Bipolar Transistor Technology: Past and Future Directions

IT IS now more than 50 years since the invention of the bipolar transistor. The emergence of the transistor from Bell Laboratories in late 1947 and early 1948 was the first step in the development of today's semiconductor electronics industry. Currently transistor production is on the order of 10^{17}/year. Although CMOS has acquired an ever-increasing role, the bipolar transistor retains its position as a premier technology for high speed circuits, power amplifiers, mixed-signal and precision analog components, and in other applications. In the intervening years, bipolar technology went through many changes, some evolutionary and some revolutionary. It was the topic of a great deal of energetic and insightful research. It continues today to be a topic of great excitement.

This Special Issue provides an unusual mix of papers. It contains the following.

1) *Historical papers* that give insight into the personal and organizational side of past developments. These are issues that seldom are evident in the standard technical papers of T-ED, but we believe provide a singular perspective on the excitement associated with bipolar research.
2) *Current research articles* that describe issues important to various aspects of state-of-the-art bipolar transistor technology.
3) *Overview articles on new concepts* which summarize recent research in areas that may provide breakthroughs in performance in the years to come.

The retrospective flavor of this issue is particularly timely in light of the fact that two contributors of many key ideas for bipolar transistor technology development were recognized with the Nobel prize in Physics in 2000. The concept of the integrated circuit from Jack Kilby was key to the widespread application of transistors. And although the Nobel citation for Herbert Kroemer focuses on his contributions to the double heterostructure laser, Dr. Kroemer also was the originator of many ideas that propelled bipolar transistor developments (as described in one of the papers in this issue).

The issue is organized according to a roughly historical outline. The first papers describe developments in the early days of the transistor, with emphasis on people and places where key contributions were made. Subsequently, innovations in bipolar transistors with polysilicon emitter technology are described, both in historical review, and as descriptions of current research. Later in the issue, the history and recent developments in SiGe bipolar transistor technology are given. Finally, III–V HBT work is described. In this category, there are several overview articles that provide a valuable summary of exciting research results that may propel the technology for decades to come.

The wide diversity of papers makes clear that many different areas of physics and technology are associated with bipolar transistors. It is also clear how research contributions to bipolar technology come from all across the globe.

The editors would particularly like to draw attention to a series of interesting and insightful invited papers in this issue. Articles by Warner, Early, Ning, and Harame are primarily historical, and describe the evolution of the technology based on Ge, Si, and more recently, SiGe, along with fascinating glimpses of the personalities of the developers and the organizations they worked for. Articles by Rodwell and Ishibashi provide overviews of new physics concepts, implemented principally in III–V semiconductors.

The editors are grateful to all the authors for their contributions. The editors are also grateful to them for their patience through the prolonged period of assembling this issue. The editors are additionally grateful to the reviewers that helped hone the articles to their present state, and to the staff at our various organizations and the IEEE that contributed to putting this issue together.

PETER M. ASBECK, *Guest Editor*
University of California, San Diego
Department of Electrical and Computer Engineering
La Jolla, CA 92093 USA
asbeck@ece.ucsd.edu

TOHRU NAKAMURA, *Guest Editor*
Hosei University
Department of Electronics and Electrical Engineering
Tokyo, 184-8584 Japan
t.nakamura@ieee.org

Publisher Item Identifier S 0018-9383(01)09093-1.

0018–9383/01$10.00 © 2001 IEEE

Peter M. Asbeck received the B.S. and Ph.D. degrees in electrical engineering from the Massachusetts Institute of Technology, Cambridge, in 1969 and in 1975, respectively.

He worked at the Sarnoff Research Center, Princeton, NJ, and at Philips Laboratory, Briarcliff Manor, NY, in the areas of quantum electronics and GaAlAs/GaAs lasers. In 1978, he joined Rockwell International Science Center, where he was involved in the development of high speed devices and circuits using III–V compounds and heterojunctions. He pioneered the effort to develop heterojunction bipolar transistors based on GaAlAs/GaAs and InAlAs/InGaAs materials, and has contributed widely in the areas of physics, fabrication, and applications of these devices. In 1991, he joined the University of California at San Diego, La Jola, as Professor in the Department of Electrical and Computer Engineering. His research interests are in development of high speed heterojunction transistors and optoelectronic devices, and their circuit applications.

Dr. Asbeck is a Distinguished Lecturer of the IEEE Electron Devices Society and the IEEE Microwave Theory and Techniques Society. He was the General Chairman of the 1996 Device Research Conference, and the founding Chairman of the IEEE Topical Workshop on Power Amplifiers for Wireless Communications.

Tohru Nakamura (M'79–SM'90–F'99) received the M.S. and Ph.D. degrees in electrical engineering from Waseda University, Tokyo, Japan, in 1971 and 1979, respectively.

He joined the Central Research Laboratory, Hitachi Ltd., Tokyo, in 1975. He worked initially in the areas of IIL circuits and high-speed silicon bipolar device and integrated circuit technologies. His key emphasis was directed to the development of a new self-aligned bipolar device, SICOS (Sidewall Base Contact Structure), and associated technologies and their application for high speed bipolar memory LSI's. He also worked in the area of high speed HEMT's and HBT's for use in telecommunication and mobile communication from 1993, as a Chief Researcher in the Central Research Laboratory, Hitachi Ltd., Tokyo Japan. During 1992–1993 he was a Visiting Professor at University of California, San Diego. He has been working at Department of Electronics and Electrical Engineering, Hosei University in Japan since 1998.

Dr. Nakamura has served as an IEDM subcommittee member in the IC area from 1989 to 1991, and as a BCTM subcommittee member of process/technology from 1994 to 1998. He has also served as an Editor for IEEE TRANSACTIONS ON ELECTRON DEVICES during 1993–1999.

Submicron Scaling of HBTs

Mark J. W. Rodwell, *Senior Member, IEEE*, Miguel Urteaga, Thomas Mathew, Dennis Scott, Dino Mensa, Q. Lee, James Guthrie, Y. Betser, Suzanne C. Martin, R. P. Smith, S. Jaganathan, Sundararajan Krishnan, Stephen I. Long, R. Pullela, Bipul Agarwal, *Member, IEEE*, Uddalak Bhattacharya, Lorene Samoska, and Mattias Dahlstrom

***Abstract*—The variation of heterojunction bipolar transistor (HBT) bandwidth with scaling is reviewed. High bandwidths are obtained by thinning the base and collector layers, increasing emitter current density, decreasing emitter contact resistivity, and reducing the emitter and collector junction widths. In mesa HBTs, minimum dimensions required for the base contact impose a minimum width for the collector junction, frustrating device scaling. Narrow collector junctions can be obtained by using substrate transfer or collector-undercut processes or, if contact resistivity is greatly reduced, by reducing the width of the base ohmic contacts in a mesa structure. HBTs with submicron collector junctions exhibit extremely high $f_{\max}$ and high gains in mm-wave ICs. Transferred-substrate HBTs have obtained 21 dB unilateral power gain at 100 GHz. If extrapolated at −20 dB/decade, the power gain cutoff frequency $f_{\max}$ is 1.1 THz. $f_{\max}$ will be less than 1 THz if unmodeled electron transport physics produce a >20 dB/decade variation in power gain at frequencies above 110 GHz. Transferred-substrate HBTs have obtained 295 GHz f_{τ}. The substrate transfer process provides microstrip interconnects on a low-ϵ_r polymer dielectric with a electroplated gold ground plane. Important wiring parasitics, including wiring capacitance, and ground via inductance are substantially reduced. Demonstrated ICs include lumped and distributed amplifiers with bandwidths to 85 GHz and per-stage gain-bandwidth products over 400 GHz, and master–slave latches operating at 75 GHz.**

***Index Terms*—Heterojunction bipolar transistors, integrated circuits (ICs).**

Manuscript received August 23, 1999; revised March 22, 2001. This work was supported in part by the University of California, Santa Barbara, the ONR under Grants N0014-99-1-0041, N00014-01-1-0065, N00014-01-1-0066, N00014-01-1-0024, N00014-98-1-0750, and N00014-98-1-0830, the AFOSR under Grant F4962096-1-0019, the ARO under the Quasi-Optical MURI PC249806 Grant, the JPL Center for Space Microelectronics Technology, Pasadena, CA, and the NASA Office of Space Science. The review of this paper was arranged by Editors P. Asbeck and T. Nakamura.

M. J. W. Rodwell, M. Urteaga, T. Mathew, D. Scott, S. Krishnan, S. I. Long, and M. Dahlstrom are with the Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA 93106 USA.

D. Mensa, S. Jaganathan, and R. Pullela were with the University of California, Santa Barbara, CA 93106 USA. They are now with Gtran, Inc., Thousand Oaks, CA 91319 USA.

Q. Lee was with the University of California, Santa Barbara, CA 93106 USA. He is now with Big Bear Networks, Milpitas, CA 95101 USA.

J. Guthrie was with the University of California, Santa Barbara, CA 93106 USA. He is now with Nortel Networks, Ottawa, ON, Canada.

Y. Betser was with the University of California, Santa Barbara, CA 93106 USA. He is now with Anadigics, Inc., Haifa, Israel.

S. C. Martin is with the Jet Propulsion Laboratory, Pasadena, CA 91109 USA.

R. P. Smith was with the Jet Propulsion Laboratory, Caltech, Pasadena, CA, 91101 USA. He is now with Cree Research, Durham, NC 27701 USA.

B. Agarwal was with the University of California, Santa Barbara. He is now with Conexant Corporation, Newport Beach, CA 92658 USA.

U. Bhattacharya was with the University of California, Santa Barbara, CA 93106 USA. He is now with Intel Corporation, Beaverton, OR 97005 USA.

L. Samoska was with the University of California, Santa Barbara, CA 93106 USA. He is now with the Jet Propulsion Laboratory, Pasadena, CA 91109 USA.

Publisher Item Identifier S 0018-9383(01)09072-4.

I. Introduction

RESEARCH in wide bandwidth heterojunction bipolar transistors (HBTs) [1], [2] is driven by applications in high-frequency communications and radar. In optical fiber communications, integrated circuits for 40 Gb/s transmission are now in development [5], [6]. Emergence of 160 Gb/s transmission equipment in the near future must rely on a timely and substantial improvement in the bandwidth of semiconductor electronics. 160 Gb/s fiber transmission will require amplifiers with flat gain and linear phase over a ∼DC-110 GHz bandwidth and master–slave latches [3] (used in decision circuits, multiplexers, and phase-lock loops) operable at 80 GHz or 160 GHz clock frequency.

A second set of driving applications are wideband, high-resolution analog–digital converters, digital–analog converters, and direct digital frequency synthesizers [8]. Increased bandwidths of these mixed-signal ICs will increase the bandwidth and frequency agility of military radar and communications systems [4]. In ADCs and DACs, very high resolution is obtained using oversampling techniques [7], [9], with clock frequencies $\sim 100 \times$ the signal bandwidths. In high resolution ADCs, to avoid metastability errors in latched comparators driven by small input signals, the circuit time constants must be much smaller than the periods of the clock signals employed. Similar design constraints apply to high-resolution DACs. High resolution ADCs and DACs consequently require transistor bandwidths $10^2:1$ to $10^4:1$ larger than the signal frequencies involved. Transistors with several hundred GHz f_τ and $f_{\max}$ would enable high-resolution microwave mixed-signal ICs.

A third driving application is in monolithic millimeter-wave integrated circuits (MIMICs). In microwave and millimeter-wave receivers, the low-noise RF preamplifier, several stages of amplification, and frequency conversion (a mixer) are typically implemented as small-scale monolithic circuits. Similar MIMICs are used in the transmitter. The operating frequency is set by the application, but progressive improvements in transistor bandwidths permit the evolution of radar and communications ICs to progressively higher frequencies. A transistor with a 1 THz power-gain cutoff frequency would provide useful gain over the full 30–300 GHz millimeter-wave band. This would permit e.g., digital radio links with millimeter-wave carrier frequencies and 1–10 Gb/s channel capacities. Until recently, III–V high-electron-mobility field-effect-transistors (HEMTs) have shown $f_{\max}$ superior to that of HBTs, and have dominated in MIMICs. With recent work on scaling of HBTs to submicron dimensions [45], HBT power-gain cutoff frequencies now exceed those of HEMTs, and HBTs can compete for application in MIMICs.

0018–9383/01$10.00 © 2001 IEEE

In high-speed digital and mixed-signal applications, III–V HBTs must compete with their silicon counterparts. The primary advantage of III–V HBTs is superior bandwidth, and the primary disadvantage is the relative immaturity of the technology, with consequently higher cost and lower scales of integration. There are several factors contributing to the superior bandwidth of III–V HBTs. For HBTs grown on GaAs or InP substrates, available lattice-matched materials allow use of an emitter whose bandgap energy is much larger than that of the base [1]. This allows the base doping to be increased to the limits of incorporation in growth $\sim 10^{20}/\text{cm}^3$ and results in very low base sheet resistance. 600 Ω□ sheet resistance and 0.15 ps base transit time is readily obtained in a Be-doped InGaAs base of 400 Å thickness. In contrast, constraints of allowable lattice mismatch in Si/SiGe HBTs limit the allowable Ge : Si alloy ratio. The emitter–base bandgap energy difference is then much smaller than in III–V HBTs, and base dopings are consequently lower. 4–8 kΩ□ base sheet resistivity is typical of SiGe HBTs [13]. High electron velocities are a second significant advantage of III–V HBTs. In InAlAs/InGaAs HBTs with 0.2–0.3 μm collector thickness, effective collector electron velocities exceed 4×10^7 cm/s, approximately 4 : 1 higher than observed in Si. This high electron velocity results in high current-gain cutoff frequencies.

Best reported results of InP-based HBTs include 300 GHz f_τ [49]. Si/SiGe HBTs [10], [11] have obtained 156 GHz f_τ. Thus, despite the advantages of III–V HBTs provided by superior materials properties, Si bipolar junction transistors (BJTs) and Si/SiGe HBTs remain highly competitive. The high bandwidths of Si/SiGe HBTs arise in part from aggressive submicron scaling. In devices with 0.14 μm emitter–base junction widths, 92 GHz f_τ and 108 GHz $f_{\max}$ have been reported [12]. Self-aligned polysilicon contacts reduce both the parasitic collector–base capacitance and the base resistance. In marked contrast to the aggressive submicron scaling and aggressive parasitic reduction employed in Si/SiGe HBTs, III–V HBTs are typically fabricated with 1–2 μm emitter junction widths and 3–5 μm collector–base junction widths. This is remarkable in an era when commodity microprocessors are available with tens of millions of transistors at 0.13 μm gate lengths. Deep submicron scaling will improve the bandwidth of III–V heterojunction bipolar transistors and is critical to their continued success.

To obtain improved HBT bandwidths by scaling, transit times are reduced by decreasing the thicknesses of the base and collector epitaxial layers. Important RC charging times are reduced by laterally scaling the base and collector junction widths. Most significant among several limits to HBT submicron scaling is the extrinsic (parasitic) collector–base junction lying under the base ohmic contacts. The required minimum size for the base ohmic contacts places a lower limit on the size of the collector–base junction, preventing submicron junction scaling. We have developed a substrate transfer process that allows fabrication of HBTs with submicron emitter–base and collector–base junctions lying on opposing sides of the base epitaxial layer. With this device, $f_{\max}$ increases rapidly with scaling. With transferred-substrate HBTs, 1.1 THz *extrapolated* power-gain cutoff frequencies and 295 GHz current-gain cutoff frequencies have been obtained. Further improvements in f_τ require further epitaxial scaling, together with increased operating current density and greatly improved emitter parasitic resistance.

II. HBT SCALING

In HBTs, thinning the base and collector epitaxial layers reduces the carrier transit times but increases the base resistance and the collector–base capacitance. These can be subsequently reduced by reducing the lithographically-defined widths of the emitter–base and collector–base junctions. To simultaneously obtain both high f_τ and high $f_{\max}$, device epitaxial and lithographic dimensions must be concurrently scaled. Below we examine the limits to HBT scaling.

Fig. 1 shows a simplified cross-section of a mesa HBT. To form the transistor, the emitter, base, and collector layers first grown by molecular-beam epitaxy (MBE) or metal–organic chemical vapor deposition (MOCVD) on a semi-insulating substrate. The HBT junctions are formed by a series of patterned etches, and contacts formed by depositing metal. This results in a device structure where the collector–base junction must lie under the full area of the base ohmic contacts. There is also a parasitic collector–base junction lying under the area of the base contact pad. In this device structure, the collector–base junction must be substantially larger than the emitter dimensions. At the sides of the emitter stripe, the base ohmic contact must be at least one ohmic contract transfer length L_{contact} in order to obtain low contact resistance. In an InGaAs-base HBT with 400 Å base thickness and $5 \times 10^{19}/\text{cm}^3$ doping, $L_{\text{contact}} \simeq 0.4$ μm. Lithographic alignment tolerances between emitter and collector also constrain the minimum collector–base junction dimensions. Dependent upon the process minimum feature size and the length of the emitter stripe, the base contact pad area can contribute as much as 50% of the total collector–base capacitance.

A. Factors Determining f_τ

Before examining scaling for high cutoff frequencies, relevant HBT parameters must first be calculated. The current-gain cutoff frequency is

$$\frac{1}{2\pi f_\tau} = \tau_b + \tau_c + \frac{kT}{qI_c}(C_{je} + C_{cb}) + (R_{ex} + R_c)C_{cb} \quad (1)$$

where

R_{ex} and R_c parasitic emitter and collector resistances;
C_{cb} collector junction capacitance;
I_c collector current.

First examine the base transit time τ_b. If a linear grading of the base semiconductor bandgap energy with position is used to reduce τ_b, then [15]

$$\tau_b = \frac{T_b^2}{D_n}\left(\frac{kT}{\Delta E}\right) - \frac{T_b^2}{D_n}\left(\frac{kT}{\Delta E}\right)^2\left(1 - e^{-\Delta E/kT}\right) + \frac{T_b}{v_{exit}}\left(\frac{kT}{\Delta E}\right)\left(1 - e^{-\Delta E/kT}\right) \quad (2)$$

where ΔE is the grading in the base bandgap energy, and T_b is the base thickness. The base exit velocity v_{exit} is of the order of $(kT/m^*)^{1/2}$ for an ungraded base and is somewhat larger

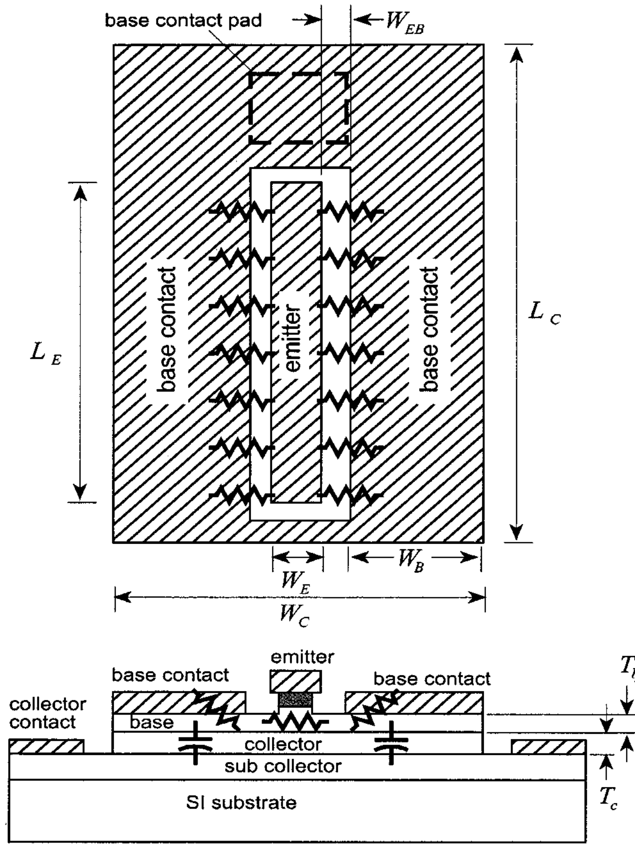


Fig. 1. Plan and cross-section of a typical mesa HBT. The emitter–base junction has width W_e, length L_e, and area $A_e = L_e W_e$, while the collector–base junction has width W_c, length L_c, and area $A_c = L_c W_c$

with base bandgap grading. D_n is the base minority carrier diffusivity and m^* the electron effective mass. Equation (2) is derived from the drift-diffusion relationship and is accurate only if the predicted τ_b is large in comparison with the momentum relaxation time $\tau_m = D_n m^*/kT$ [16]. Using the parameters of an InGaAs base at 5 × 10^{19}/cm^3 doping (D_n = 40 cm^2/sec, v_{exit} ∼ 3 × 10^7 cm/s, τ_m = 35 fs), we note that 52 meV bandgap grading is sufficient to reduce τ_b by ∼2 : 1. For a thick base layer or a large v_{exit}, $\tau_b \propto T_b^2$, with InGaAs base layers below ∼400 Å thickness, the exit velocity term in (2) adds a significant correction.

The collector transit time τ_c is the mean delay of the collector displacement current, and is given by [17], [18]

$$\tau_c = \int_0^{T_c} \frac{(1 - x/T_c)}{v(x)}\, dx \equiv \frac{T_c}{2v_{\text{eff}}} \tag{3}$$

where $v(x)$ is the position-dependent electron velocity in the collector drift region and v_{eff} an effective electron velocity. τ_c is most strongly dependent upon the electron velocity in the proximity of the base and becomes progressively less sensitive to the electron velocity as the electron passes through the collector [18]. At low collector–base bias voltages, electrons must traverse a significant fraction of the collector drift region before acquiring sufficient kinetic energy (0.55 eV for InGaAs [19], 0.6eV for InP [20]) to undergo Γ-L scattering [17], [18], and $v(x)$ is fortuitously highest near the base. In thin InGaAs or InP layers, v_{eff} = 3–5 × 10^7 cm/s. For scaling analysis, we will take $\tau_c \propto T_c$.

In InAlAs/InGaAs HBTs with $T_b \cong 400$ Å and $T_c \cong 0.2$ μm, $f_\tau \simeq 250$ GHz, and the RC charging terms in (1) comprise 35% of the total forward delay. These terms must be considered in detail.

First consider the charging time $[kT/qI_c]C_{cb}$. This term has a major impact upon digital circuit delay (Section II-F) and is reduced by increasing the collector current density to limits set by collector space-charge screening (the Kirk effect [21]). If the collector doping N_d is chosen so as to obtain a fully-depleted collector at zero bias current and the applied V_{cb}, we must have

$$V_{cb} + \phi = qN_d T_c^2/2\epsilon \tag{4}$$

while base pushout occurs at a current density $J_{\max}$ satisfying

$$V_{cb} + \phi = (J_{\max}/v_{sat} - qN_d)\, T_c^2/2\epsilon. \tag{5}$$

Hence, the maximum collector current before base pushout is

$$I_{c,\max} = A_e(V_{cb} + \phi) 4\epsilon v_{sat}/T_c^2 \propto A_e/T_c^2 \tag{6}$$

where v_{sat} is a (assumed) uniform electron velocity within the collector. With undoped collectors, $I_{c,\max}$ is 2 : 1 smaller than in (6). The collector capacitance is $C_{cb} = \epsilon A_c/T_c$. With the HBT biased at $I_{c,\max} \propto 1/T_c^2$, $(kT/qI_C)C_{cb} \propto T_c(A_c/A_e)$. This delay term is thus minimized by scaling (reducing T_c), but bias current densities must increase in proportion to the square of the desired fractional improvement in f_τ.

The emitter charging time [$C_{je}[kT/qI_c]$ in (1)] is a significant determinant of f_τ and also plays a major role in ECL logic delay (Section II-F). If we were to assume that C_{je} were simply a depletion capacitance, it would be reasonable to expect that this charging time could be minimized simply by making the emitter–base depletion region very thick, by use of very low emitter doping, combined with a thick bandgap grading region in the base–emitter heterojunction. Clearly, this approach must fail somehow in the limit of very large depletion thicknesses. We must examine design of the emitter–base junction in detail to determine the limits to the emitter–base depletion thickness, and to understand how the junction design must be modified as the transistor is scaled for increased device bandwidth.

In order to support a high emitter current density without a substantial potential drop in the emitter–base depletion layer, a high electron density $n(x)$ must be present within the emitter–base junction. In high-speed HBTs, the thickness T_{eb} of the emitter–base depletion layer must then be small if significant charge storage effects are to be avoided. Fig. 2 shows a band diagram of the base–emitter depletion region. $n(x) = N_c \exp[-q(E_c(x) - E_{f,n}(x))/kT]$, where N_c is the conduction band effective density of states, $E_c(x)$ is the conduction-band energy, and $E_{f,n}(x)$ is the electron quasi-Fermi level. An arbitrary conduction-band profile $E_c(x)$ can be obtained through combined bandgap grading and doping. Under modulation of V_{be}, $\partial n(x)/\partial V_{be} = n(x)(q/kT)(x/T_{e,b})$. Here, $x = 0$ is defined at the emitter edge of the depletion region, as shown in Fig. 2. The ideality factor N is defined by

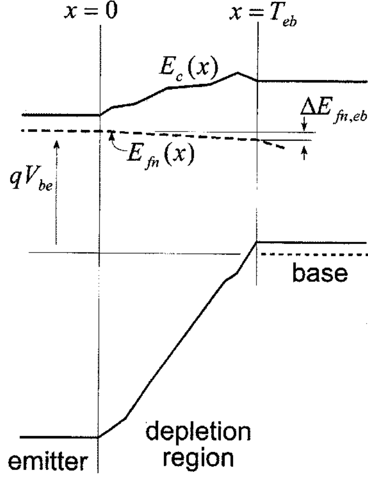


Fig. 2. Band diagram of the HBT emitter–base junction. If the base–emitter junction thickness T_{eb} is excessive, HBT performance will be degraded by either stored charge or by excessive potential drops in the depletion layer.

the relationship $I_c \propto e^{qV_{be}/NkT}$, and gradients in E_{fn} in the emitter–base depletion region result in N greater than unity, with

$$N = 1 + \frac{1}{q}\frac{\partial(\Delta E_{fn,eb})}{\partial V_{be}}. \quad (7)$$

In the base–emitter depletion region, $dE_{fn}/dx = -J/\mu_{n,eb}n(x)$, while in the base $J_n = qn(T_{eb})D_n/T_b\Gamma$. Here, $\mu_{n,eb}$ is the electron mobility in the junction (due to the low doping in the grade, this mobility is significantly larger than that of the base), and $\Gamma = kT/\Delta E - (kT/\Delta E - D_n/v_{exit}T_b)e^{-\Delta E/kT}$ is a factor involving the base bandgap grading ($\Gamma \simeq 1$ for an ungraded base). Combining these relationships, the ideality factor is

$$N = 1 + \frac{T_{eb}}{T_b}\frac{\mu_n}{\Gamma\mu_{n,eb}}\int_0^1 \frac{n(T_{eb})}{n(\zeta T_{eb})}(1-\zeta)\,d\zeta \quad (8)$$

where $\zeta = x/T_{eb}$ is a normalized position variable, and μ_n is the electron mobility in the base. To obtain a low ideality factor, T_{eb}/T_b must not be large, and the electron density $n(x)$ in the junction must be kept high. Unless T_{eb}/T_b is kept small, the high $n(x)$ will result in significant charge storage. Using methods similar to those used to derive the collector transit time [17], [18] (3)

$$C_{je}/A_e = \epsilon/T_{eb} + \frac{\partial}{\partial V_{be}}\left[\int_0^{T_{eb}} (x/T_{eb})\,qn(x)\,dx\right]. \quad (9)$$

The term $(kT/qI_c)C_{je}$ in (1) can be then written as

$$(kT/qI_c)C_{je} = \left(\frac{\epsilon A_e}{T_{eb}}\right)\left(\frac{kT}{qI_c}\right) + \frac{\Gamma T_{eb}T_b}{D_n}\int_0^1 \frac{n(\zeta T_{eb})}{n(T_{eb})}\zeta^2\,d\zeta. \quad (10)$$

The first term in (10) results from the depletion-layer capacitance, and is minimized using high bias current densities $J_e = I_e/A_e$; the second term reflects storage of mobile electron charge within the depletion layer, and is minimized by reducing $T_{eb}T_b$.

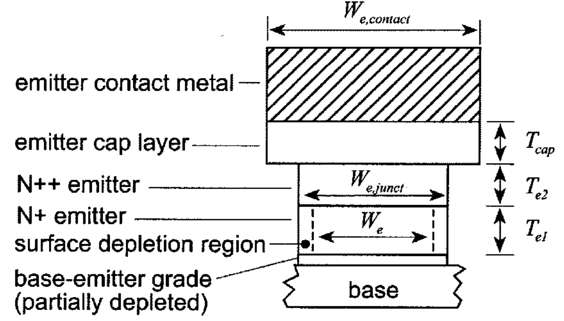


Fig. 3. Cross section of the emitter layers within a typical HBT, comprising a heavily doped semiconductor contact ("cap") layer, a low-resistance N++ emitter layer, and the N+ emitter. Lateral depletion of the N++ emitter can be significant in submicron devices.

In (1), the delay term $R_{ex}C_{cb}$ is a major limit to HBT scaling for high f_τ. Further, R_{ex} contributes significantly to ECL logic delay. Because of the relative sizes of the emitter and collector ohmic contacts, in a *well-designed* submicron HBT, R_c is 4 : 1 to 10 : 1 smaller than R_{ex} and R_cC_{cb} can be neglected in a first analysis. R_{ex} must first be calculated. The emitter layer structure of a typical HBT (Fig. 3) contains a heavily doped and narrow-bandgap contact ("cap") layer, and a heavily-doped N++ wide-bandgap emitter layer. A portion of the emitter layer may be more lightly (N+) doped for reduced junction capacitance, and may be of several hundred Å thickness to avoid dopant diffusion from the N++ layer into the emitter–base junction. If heterointerfaces are properly graded to avoid conduction-band barriers between layers, the parasitic emitter resistance is

$$R_{ex} = \rho_{c,e}/L_eW_{e,contact} + \rho_{cap}T_{cap}/L_eW_{e,contact} + \rho_{e2}T_{e2}/L_eW_{e,junct} + \rho_{e1}T_{e1}/L_eW_e \quad (11)$$

where $\rho_{c,e}$ is the emitter specific ohmic contact resistivity, and ρ_{cap}, ρ_{e2}, and ρ_{e1} are the bulk resistivities of the cap, N++, and N+ emitter layers. For submicron emitters, the junction width $W_{e,junct}$ is significantly smaller than the contact width $W_{e,contact}$ due to lateral undercutting of the emitter during etching of the emitter–base junction, and the electrically active emitter width W_e can be significantly smaller than $W_{e,junct}$ because of the presence of surface (edge) depletion regions of width $(2\epsilon\phi/qN_{e1})^{1/2}$, where N_{e1} is the N+ layer doping, and ϕ is the bandbending due to pinning of the Fermi energy at the surface. For simplicity in scaling analysis, we will approximate

$$R_{ex} \simeq \rho_e/A_e \quad (12)$$

where ρ_e is a fitted parameter, approximately 50 Ω-μm^2 for submicron InAlAs/InGaAs HBTs fabricated to date at the University of California, Santa Barbara. In the InAlAs/InGaAs HBTs we have fabricated, $\rho_{c,e} = 20$ Ω-μm^2 when InGaAs contacts at 10^{19}/cm^3 doping are employed, and $\rho_{c,e} = 4$ Ω-μ m^2 for contacts to InAs layers at 2×10^{19}/cm^3 doping. The $\rho_{e1}T_{e1} = 5.5$ Ω-μm^2 resistance of the N+ InAlAs layer (8×10^{17}/cm^3 doping, 700 Å thickness) is significant in submicron devices for which W_e is 2 : 1 to 4 : 1 smaller than $W_{e,contact}$.

To avoid such emitter size effects, deep submicron HBTs should use $\gg 10^{18}$/cm^3 emitter doping.

The $R_{ex}C_{cb}$ charging time can now be examined. Since $C_{cb} = \epsilon A_c/T_c$

$$R_{ex}C_{cb} = \left(\frac{\epsilon \rho_e}{T_c}\right)\left(\frac{A_c}{A_e}\right) = 28 \text{ fs} \times \left(\frac{A_c}{A_e}\right) \tag{13}$$

if $\rho_e = 50\ \Omega$-μm^2 and $T_c = 0.2\ \mu$m. This a significant delay. In HBTs, we have fabricated with 275 GHz peak f_τ and the substrate transfer process allows A_c/A_e to be kept small at 2.3 : 1, yet $R_{ex}C_{cb}$ still constitutes 11% of the total $1/2\pi f_\tau = 0.58$ ps forward delay. In mesa HBTs (Fig. 1) A_c/A_e is often larger than 2.3 : 1 and hence, $R_{ex}C_{cb}$ will contribute a larger delay. Because $R_{ex}C_{cb} \propto 1/T_c$, thinning the collector to reduce τ_c also increases $R_{ex}C_{cb}$.

To increase HBT current gain cutoff frequencies, the base and collector layers must be thinned and the bias current density increased. Thinning the collector increases $R_{ex}C_{cb}$, imposing a limit to scaling. Limits to bias current density imposed by device reliability and loss in breakdown voltage with reduced collector thickness are two further potential limits to scaling. Finally, unless the device structure of Fig. 1 is laterally scaled, vertical HBT scaling for increased f_τ will result in *reduced* power-gain cutoff frequencies $f_{\max}$.

B. Lithographic Scaling for High $f_{\max}$

Regardless of the value of f_τ, transistors cannot provide power gain at frequencies above $f_{\max}$. Independent of f_τ, $f_{\max}$ defines the maximum usable frequency of a transistor in either narrowband reactively-tuned or broadband distributed circuits [22]. In more general analog and digital circuits (Section II-F), all transistor parasitics play a significant role. The f_τ and $f_{\max}$ of a transistor are then cited to give a first-order summary of the device transit delays and of the magnitude of its dominant parasitics.

In an HBT with base resistance R_{bb} and collector capacitance C_{cb}, the power-gain cutoff frequency is approximately $f_{\max} \simeq (f_\tau/8\pi R_{bb}C_{cbi})^{1/2}$. The base–collector junction is a distributed network, and $R_{bb}C_{cbi}$ represents an effective, weighted time constant.

The base resistance (Fig. 1) R_{bb} is composed of the sum of contact resistance R_c, base–emitter gap resistance R_{gap}, and spreading resistance under the emitter R_{spread}. With base sheet resistance ρ_s, and specific (vertical) contact access resistance ρ_c, we have

$$\begin{aligned} R_{bb} &= R_{b,\,cont} + R_{gap} + R_{spread} \\ R_{b,\,cont} &= \sqrt{\rho_s \rho_c}/2L_e \\ R_{gap} &= \rho_s W_{eb}/2L_e \\ R_{spread} &= \rho_s W_e/12L_e. \end{aligned} \tag{14}$$

To compute $f_{\max}$, we must find C_{cbi}. Because the base–collector junction parasitics are distributed, calculation of $R_{bb}C_{cbi}$ is complex and will be deferred until Section II-C. As a first (and very rough) approximation, we will first compute $R_{bb}C_{cb}$, e.g., the product of the base resistance and the full capacitance $C_{cb} = \epsilon A_c/T_c$ of the collector–base junction

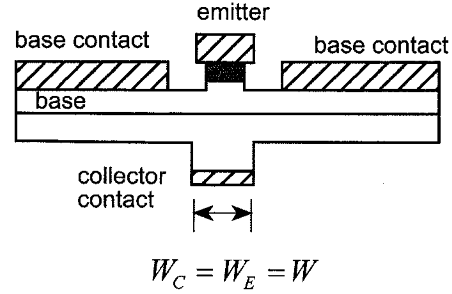


Fig. 4. Cross section of an idealized HBT with the collector–base junction lying only under the emitter. Such device structures can be formed using substrate transfer processes.

$$R_{bb}C_{cb} = \left[\left(\sqrt{\rho_s\rho_c} + \rho_s W_{eb}\right)\left(\frac{\epsilon}{2}\right)\left(\frac{L_c}{L_e}\right)\right]\left[\frac{W_c}{T_c}\right] + \left[\left(\frac{\rho_s \epsilon}{12}\right)\left(\frac{L_c}{L_e}\right)\right]\left[\frac{W_c W_e}{T_c}\right]. \tag{15}$$

Consider the influence of device scaling on the time constant $R_{bb}C_{cb}$. Decreasing the base thickness to reduce τ_b increases the base sheet resistivity ρ_c, increasing $R_{bb}C_{cb}$. Decreasing the collector thickness T_c to reduce τ_c directly increases $R_{bb}C_{cb}$, as is shown explicitly in (15).

Low $R_{bb}C_{cb}$, and consequently high $f_{\max}$, is obtained by scaling the emitter and collector junction widths W_e and W_c to submicron dimensions. Reducing the emitter width W_e alone reduces toward zero the component of $R_{bb}C_{cb}$ associated with the base-spreading resistance [the second term in (15)]. In the normal triple-mesa HBT (Fig. 1), the base ohmic contacts must be at least one contact transfer length ($L_{\text{contact}} = (\rho_c/\rho_s)^{1/2}$), setting a minimum collector junction width W_c. The component of $R_{bb}C_{cb}$ associated with the base contact resistance [the first term in (15)] has a minimum value, independent of lithographic limits. Consequently, $f_{\max}$ does not increase rapidly with scaling. Given this minimum $R_{bb}C_{cb}$, attempts to obtain high f_τ by thinning the collector have resulted in decreased $f_{\max}$, frustrating efforts to improve HBT bandwidths.

If the parasitic collector–base junction is eliminated, $f_{\max}$ will instead increase rapidly with scaling. The collector–base junction need only be present where current flows, e.g., under the emitter. We have fabricated such a device (Fig. 4) using substrate transfer processes. The emitter and collector junctions can be of equal width, hence $W_c = W_e$. The base–collector time constant becomes

$$R_{bb}C_{cb} = \left[\left(\sqrt{\rho_s\rho_c} + \rho_s W_{eb}\right)\left(\frac{\epsilon}{2}\right)\left(\frac{L_c}{L_e}\right)\right]\left[\frac{W_e}{T_c}\right] + \left[\left(\frac{\rho_s \epsilon}{12}\right)\left(\frac{L_c}{L_e}\right)\right]\left[\frac{W_e^2}{T_c}\right]. \tag{16}$$

With submicron scaling of the emitter and collector junction widths, the first term in (16) dominates, and $f_{\max}$ increases as the inverse square root of the process minimum feature size.

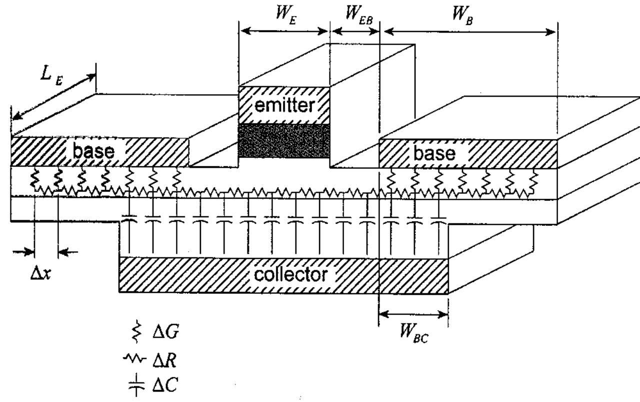


Fig. 5. Distributed model of the HBT base-collector junction for accurate calculation of $R_{bb}C_{cbi}$. With mesh spacing Δx, $\Delta G = L_e \Delta x/\rho_c$, $\Delta R = \rho_s \Delta x/L_e$, and $\Delta C = \epsilon L_e \Delta x/T_c$.

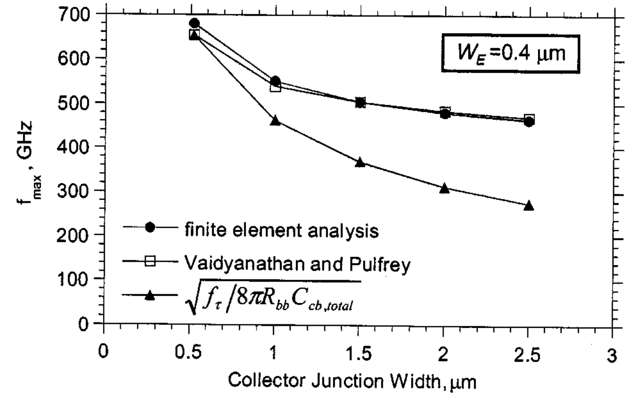


Fig. 6. Comparison of $f_{\max}$ computed from a finite-element model with Vaidyanathan and Pulfrey's model (17) and a model using the total collector junction capacitance (15). Except for W_c, the modeled HBT is that of Fig. 14 and has $W_e = 0.4$ μm.

C. Secondary Effects in $f_{\max}$

The formulas developed previously are highly simplified and significantly underestimate the HBT $f_{\max}$. Two significant corrections must be applied. First, the simple lumped RC model of the base–collector junction must be re-examined. Secondly, differential space-charge effects substantially reduce the collector–base capacitance under high-current conditions.

The HBT base-collector network is distributed, and is represented by the model of Fig. 5. Using a small grid spacing, we have entered the resulting network into a microwave circuit simulator (HP-EESOF [23]) to calculate, without approximation, the HBT $f_{\max}$. Alternatively, analytic expressions for $f_{\max}$ can be developed from hand analysis of the distributed network of Fig. 5. Among these is the model of Vaidyanathan and Pulfrey [24], which provides good physical insight. The model of reference [24] is derived for a triple-mesa HBT. The authors of [25] have recently generalized the model to the case of transferred-substrate and lateral-etched-undercut collector [30] HBTs. We describe the Vaidyanathan/Pulfrey model below, and examine its predicted performance for HBTs with submicron emitter and collector junction widths.

Referring to Fig. 5, define three capacitances. $C_{cb,\,e} = \epsilon L_e W_e/T_c$ is the capacitance of the collector junction lying under the emitter. $C_{cb,\,gap} = 2\epsilon L_e W_{eb}/T_c$ is the capacitance of the collector junction lying under the gap between the emitter and the base contact. $C_{cb,\,ext} = 2\epsilon L_e W_{cb}/T_c$ is the capacitance of the collector lying under the base ohmic contacts. Components of the base resistance are as defined in (14).

The collector–base capacitance under the emitter stripe $C_{cb,\,e}$ is charged through a resistance $(R_{b,\,cont}+R_{gap}+R_{spread})$. The collector–base capacitance under the gap between the emitter and the base ohmic contacts is charged through a resistance $(R_{b,\,cont}+R_{gap}/2)$.

The charging time constant associated with the collector–base junction capacitance $C_{cb,\,ext}$ lying under the base ohmics requires more detailed scrutiny. $C_{cb,\,ext}$ can be charged by currents passing vertically through the base ohmic contact above it. This path has a resistance $R_{b,\,cont,\,1} = \rho_c/2L_e W_{cb}$. Alternatively, $C_{cb,\,ext}$ can be charged by currents passing laterally from the base contact region lying outside the perimeter of the collector contact. This path has a resistance $R_{b,\,cont,\,0} = (\rho_s\rho_c)^{1/2}\coth((W_b - W_{bc})/L_{\text{contact}})$, where $L_{\text{contact}} = (\rho_c/\rho_s)^{1/2}$ is the base ohmic contact transfer length.

In the limit of zero collector series resistance, Vaidyanathan and Pulfrey's model [24], [25] reduces to

$$f_{\max} = \sqrt{\frac{f'_\tau}{8\pi\tau_{cb}}} \tag{17}$$

where

$$\frac{1}{2\pi f'_\tau} = \tau_b + \tau_c + \frac{kT}{qI_c}(C_{je} + C_{cb}) \tag{18}$$

and

$$\begin{aligned}\tau_{cb} =& C_{cb,\,e}\,(R_{b,\,cont} + R_{gap} + R_{spread}) \\ &+ C_{cb,\,gap}\,(R_{b,\,cont} + R_{gap}/2) \\ &+ (R_{b,\,cont,\,0} \| R_{b,\,cont,\,1})\,C_{cb,\,ext}.\end{aligned} \tag{19}$$

Examining Fig. 5, the external collector capacitance $C_{cb,\,ext}$ is not charged through the resistances R_{gap} and R_{spread}. It is pessimistic to calculate $f_{\max}$ as $(f_\tau/8\pi R_{bb}C_{cb})^{1/2}$, in which the collector–base time constant includes the full collector–base capacitance. As indicated by Vaidyanathan and Pulfrey's model (17), the external collector capacitance $C_{cb,\,ext}$ is in fact charged through a smaller associated resistance $(R_{b,\,cont,\,0}\|R_{b,\,cont,\,1})$. This model shows extremely good agreement with finite-element analysis (Fig. 6).

Fig. 7 compares the $f_{\max}$ of mesa and transferred-substrate HBTs, computed using the finite-element model. For the transferred-substrate device, $f_{\max}$ increases rapidly with deep submicron scaling. Experimentally, we observe a more rapid variation of $f_{\max}$ with collector width than is shown in Figs. 6 and 7 predicts a higher $f_{\max}$ than is experimentally observed for mesa HBTs. Series resistance in the base metallization and collector series resistance [24] (not modeled previously, and not present in Schottky-collector transferred-substrate HBTs) are possible explanations for the discrepancy.

At high collector current densities, differential space-charge effects in the collector space-charge region result in C_{cb} smaller than $\epsilon A_c/T_c$ and increase the HBT $f_{\max}$. The effect was predicted by Camnitz and Moll [27] and first experimentally ob-

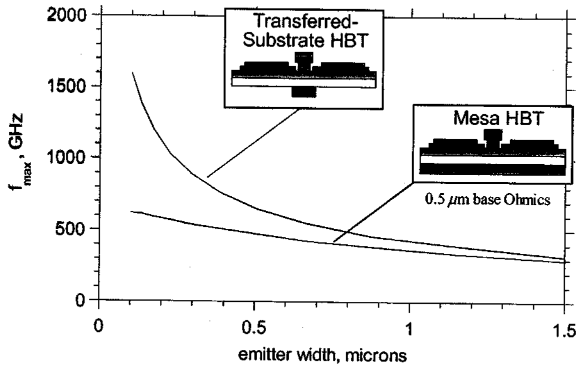


Fig. 7. Lithographic scaling of transferred-substrate and mesa HBTs. $f_{\max}$ is calculated using Fig. 5's finite-element model of the collector–base junction. Except for W_c and W_e, the HBT parameters are taken from the device of Fig. 14. Current density and epitaxial layer thicknesses are held constant, resulting in constant f_τ.

served by Betser and Ritter [26]. Similar effects have been observed in MESFETs [28]. In III–V materials at high fields, electron velocity $v(\mathcal{E})$ decreases with increasing electric field. To a first approximation, $1/v(\mathcal{E}) \simeq \kappa_0 + \kappa_1\mathcal{E}$. Modulating the collector voltage V_{cb} modulates the collector transit time τ_c (3) and partially modulates the space-charge in the collector drift region. This modulated space-charge partially screens the base from modulations in the collector applied field, and $C_{cb,\,e}$ is reduced to

$$C_{cb,\,e} = \epsilon A_e/T_c - I_c \frac{d\tau_c}{dV_{cb}} = \frac{\epsilon A_e}{T_c} - \frac{\kappa_1 J_c A_e}{2}\left[1 - \frac{\kappa_1 J_c T_c}{6\epsilon}\right]. \quad (20)$$

The quadratic dependence upon J_c results from internal collector field redistribution in the presence of the collector space-charge [27]. Current spreads laterally during transport through the collector, flowing through a region of width $\sim (W_e + T_c)$. The differential space charge effect strongly reduces the collector junction capacitance in regions below and adjacent to the emitter stripe. It thus has the strongest impact upon $f_{\max}$ in devices with minimal excess collector capacitance. Experimental data confirming C_{cb} cancellation will be shown in Section III-B. Capacitance cancellation is not instantaneous, but instead arises after a delay proportional to τ_c. HBT power gain must therefore decrease at -40 dB/decade for frequencies above $\sim 1/2\pi\tau_c$. This effect can produce a $\sim 2:1$ increase in $f_{\max}$ and hence, a large increase in the attainable gain of tuned millimeter-wave amplifiers. In contrast, in digital circuits, many delay terms are significant, and a $2:1$ reduction in C_{cbi} would produce only a $\sim$12% decrease in gate delay.

D. HBT Equivalent Circuit Model

The HBT base–collector network is distributed, and accurate expressions for $f_{\max}$ are complex. Computer simulation of complex circuits requires a compact device model. Under small-signal operation, the Gummel–Poon model used in SPICE reduces to the simple hybrid-π model of Fig. 8. For this model, $f_{\max} = (f_\tau/8\pi R_{bb} C_{cbi})^{1/2}$. It should be emphasized that C_{cbi}

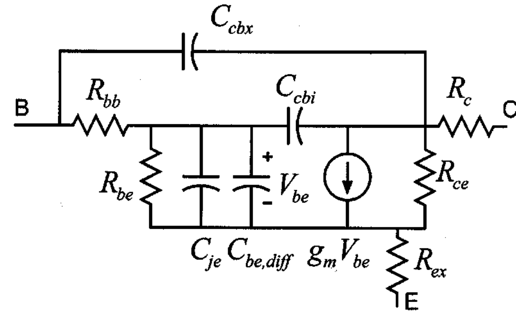


Fig. 8. Hybrid-π small-signal HBT equivalent circuit; $C_{be,\,\text{diff}} = g_m(\tau_b + \tau_c)$. The element C_{cbi} does not represent capacitance of that fraction of the collector junction lying under the emitter but is instead a parameter adjusted to obtain the correct $f_{\max}$.

corresponds to no particular physical area in the collector–base junction. Specifically, C_{cbi} is not equal to $C_{cb,\,e}$, the capacitance of that fraction of the collector junction which lies under the emitter. Instead, in this model, R_{bb} is given by (14), $(C_{cbx} + C_{cbi}) = \epsilon A_c/T_c$, and the intrinsic collector–base capacitance is set to $C_{cbi} = \tau_{cb}/R_{bb}$, where τ_{cb} is given by (19). Thus, C_{cbi} is defined so that the simplified model predicts the correct device $f_{\max}$. To correctly model common-base and emitter–follower input impedance at $f \simeq f_\tau$, the transconductance element must have an associated delay of $\sim(\tau_c + \zeta\tau_b)$, where the factor $\zeta \simeq$ 0.1–0.2 is dependent upon the degree of base bandgap grading.

E. High $f_{\max}$ HBT Designs

To obtain simultaneous high values of f_τ and $f_{\max}$, the emitter and collector stripe widths must both be scaled. The substrate transfer process is an extremely aggressive method of reducing the parasitic extrinsic collector–base junctions and requires a substantial departure from typical fabrication processes. There are alternatives requiring less radical processing. With GaAs/AlGaAs HBTs [29] deep proton implantation can reduce the extrinsic collector capacitance. The extrinsic collector junction can be undercut using selective wet chemical etches [30], [31]. Collector capacitance under the base contact pad can be reduced using dielectric spacer layers [32]. Alternatively, R_{bb} can be reduced by regrowing, prior to base contact deposition, thick extrinsic p+ contact regions on the exposed base surface [33], [34]. Finally, low $R_{bb}C_{cbi}$ can be obtained in mesa HBTs by reducing the size of the base ohmic contacts. Using a CBr_4 doping source, we have grown by MBE InGaAs base layers with $>10^{20}/\text{cm}^3$ carbon (p-type) doping. At such doping levels, ρ_c and hence the transfer length $L_{\text{contact}} = (\rho_c/\rho_s)^{1/2}$ are greatly reduced. The width of the base ohmic contacts can be accordingly reduced.

F. General HBT Scaling Laws for High Speed Circuits

As examined in Sections II-B and II-C, lithographic scaling of the emitter and collector junction widths progressively increases $f_{\max}$ if the parasitic collector–base junction is eliminated. If the lithographic dimensions are scaled while holding the base and collector epitaxial layer thicknesses constant, $f_{\max}$ increases rapidly, while f_τ remains relatively constant. While

TABLE I
APPROXIMATE DELAY COEFFICIENTS a_{ij}, FOR AN ECL MASTER–SLAVE LATCH, FOUND BY HAND ANLAYSIS. GATE DELAY IS OF THE FORM $T_{gate} = 1/2f_{clock} = \Sigma a_{ij} r_i c_j$. THE MINIMUM ALLOWABLE LOGIC VOLTAGE SWING IS $\Delta V_L \simeq 6kT/q + J\rho_e$, WHERE J IS THE EMITTER CURRENT DENSITY

..	c_{je}	c_{cbx}	c_{cbi}	$\tau_f J/\Delta V_L$
$\Delta V_L/J$	1	6	6	1
kT/qJ	0.5	1	1	0.5
ρ_e	-0.25	0.5	0.5	0.5
r_{bb}	0.5	0	1	0.5

such a device will produce gain at very high frequencies in reactively-tuned MIMICs, broadband analog circuits require simultaneous high values of f_τ and $f_{\max}$.

Digital circuits demand that all relevant HBT parasitics be small. Approximate expressions for logic gate delay can be found through hand analysis by the charge control method. By this method, the maximum clock frequency of a typical benchmark emitter-coupled-logic (ECL) circuit, a master–slave latch (Fig. 25) is found to be approximately $T_{gate} = 1/2f_{clock} = \Sigma a_{ij} r_i c_j$, where the delay coefficients a_{ij} are given in Table I. It is found that ~10 equivalent RC delay terms are significant.

In order to improve logic speed, all significant HBT capacitances and transit delays must be reduced. We now examine the scaling of HBT parameters required to increase bandwidth by a factor of $\gamma : 1$, using simplified expressions for HBT parameters in order to more clearly show the dominant trends. To ensure that bandwidth increases by $\gamma : 1$ for *all* circuits, digital and analog, using the scaled HBT, all transit times and all capacitances in Fig. 8 must be reduced by $\gamma : 1$, while maintaining constant all resistances, the transconductance, and the collector bias current I_c. Explicitly, $I_c \propto \gamma^0$ and $g_m \propto \gamma^0$.

The base–emitter diffusion capacitance is

$$C_{be,\,\text{diff}} = g_m(\tau_b + \tau_c) = (qI_c/kT)(\kappa_2 T_b^2 + \kappa_3 T_c). \quad (21)$$

Here the terms κ_i represent parameters that do not change with scaling. To obtain $C_{be,\,\text{diff}} \propto \gamma^{-1}$ with fixed I_c, we must set $\tau_b \propto \gamma^{-1}$ and $\tau_c \propto \gamma^{-1}$. This requires $T_b \propto \gamma^{-1/2}$ and $T_c \propto \gamma^{-1}$.

An immediately apparent limit to collector scaling is loss of collector breakdown voltage. An AlInAs/GaInAs HBT with a 0.2 μm InGaAs collector thickness exhibits $V_{br,\,ceo} = 1.5$ V at 10^5 A/cm^2 bias. Semiconductors with higher products ($\mathcal{E}_{\max} v_{sat}$) of breakdown field and electron velocity mitigate this limit. HBTs with InP collectors [35] exhibit τ_c comparable to devices with InGaAs collectors, but have ~5 : 1 increased breakdown. Regardless of the collector thickness, for V_{ce} less than the bandgap of the collector semiconductor, most electrons transiting the layer will not obtain sufficient energy for electron-hole pair generation. Therefore, for thin collectors, the impact ionization breakdown voltage tends to reduce to a value close to the collector bandgap energy. Further, unless the collector bandgap is small or the collector much thinner than 1000 Å, Zener tunneling currents will also be small for bias voltages below the collector bandgap energy. Even with 1000-Å collector layers, an InP/GaInAs/InP DHBT will exhibit $V_{br,\,ceo} > 1.2$ V, sufficient for current-mode logic. While important in power amplifiers and in mixed-signal (medium-voltage) ICs, loss of breakdown voltage may not pose a serious limit to the scaling of InP-collector DHBTs for low-voltage, high-speed logic.

The capacitance C_{je} is given by

$$C_{je} = C_{je1} + C_{je2} = \kappa_4 L_e W_e / T_{eb} + \kappa_5 T_{eb} T_b I_c. \quad (22)$$

To obtain $C_{je2} \propto \gamma^{-1}$, we must set $T_{eb} \propto \gamma^{-1/2}$. This results in $C_{je1} \propto \gamma^{-3/2}$, improving more rapidly than required for a $\gamma : 1$ scaling in transistor bandwidth.

Analysis of the partitioning of C_{cb} between $C_{cb,\,x}$ and C_{cbi} is complex (Section II-E), and in this section, we therefore restrict the analysis to HBTs in which $C_{cb,\,x}$ is zero ($L_c \simeq L_e$ and $W_c \simeq W_e$) and $C_{cbi} = C_{cb}$. Such HBTs include transferred-substrate (Fig. 4) and undercut-mesa devices and mesa devices having very high base doping and hence requiring only a very small base ohmic contact width. C_{cb} then scales as

$$C_{cb} = \epsilon W_c L_c / T_c \simeq \epsilon W_e L_e / T_c. \quad (23)$$

Because $T_c \propto \gamma^{-1}$, to obtain $C_{cb} \propto \gamma^{-1}$ we must set $W_c L_c \propto \gamma^{-2}$ and hence $W_e L_e \propto \gamma^{-2}$.

The base resistance R_{bb} is the sum of the terms (14) $R_{b,\,cont}$, R_{gap}, and R_{spread}. Correct scaling of C_{cb} requires that $W_e L_e \propto \gamma^{-2}$. It is desired that R_{bb} vary negligibly with scaling. We show here that this is obtained by setting $W_e \propto W_c \propto \gamma^{-2}$ and $L_e \simeq L_c \propto \gamma^0$. The base contact resistance term $R_{b,\,cont} = \kappa_6 \rho_c^{1/2} / L_e T_e$ is proportional to $\gamma^{1/4}$, while $R_{spread} = \kappa_7 W_e / L_e T_{eb} \propto \gamma^{-3/2}$. If we scale $W_{eb} \propto \gamma^{-1}$, then $R_{gap} = \kappa_8 W_{eb} / L_e T_b \propto \gamma^{-1/2}$. While the contact resistance term $R_{b,\,cont}$, the dominant term in R_{bb} for submicron devices increases ($\propto \gamma^{1/4}$) slowly with scaling, and the rapid decrease in R_{gap} and R_{spread} results in a total R_{bb} showing only a very slow increase with scaling.

The collector series resistance R_c is zero in transferred-substrate HBTs using Schottky collector contacts. In undercut-mesa devices, R_c has a similar geometric dependence as R_{bb}, and also varies only minimally with scaling.

Scaling thus requires that the emitter and collector stripe widths W_e and W_c be proportional to γ^{-2}, and that the emitter and collector stripe lengths L_e and L_c be independent of scaling. Because the collector current is constant ($I_c \propto \gamma^0$), the emitter current density increases quadratically with the desired improvement in transistor bandwidth ($J_e \propto \gamma^2$), as does the transistor's operating power density ($P/A_e = J_e V_{ce} \propto \gamma^2$). Limits to bias current density imposed by reliability concerns and dissipated power density are thus major impediments to scaling for high bandwidth.

The emitter resistance $R_{ex} = \rho_e / W_e L_e$ presents a major impediment to scaling. With $W_e L_e \propto \gamma^{-2}$, in order to maintain the desired constant R_{ex} the aggregate emitter resistivity $\rho_e \propto \gamma^{-2}$ must improve in proportion to the square of the intended improvement in HBT bandwidth. This will require substantial increases in emitter doping over those now typically used in HBTs, and use of low-resistivity (e.g., InAs) semiconductor contact layers.

The collector–emitter resistance is $R_{ce} = V_A / I_c$, where the Early voltage is $V_A = qN_a T_b T_c / \epsilon$ and N_a is the base doping. From these relationships $R_{ce} \propto \gamma^{-3/2}$, and does not scale as desired. Fortunately, for an HBT with $T_b = 300$ Å, $T_c = 0.2$ μm,

and $N_A = 5 \cdot 10^{19}/\text{cm}^3$ (a device with 275 GHz f_τ), $V_A \sim 500$ V. A $\gamma = 10:1$ scaling for a target 2750 GHz f_τ would still result in $V_A = 16$ Volts, which is acceptably large. In HBTs, degradation of R_{ce} through base-width modulation is not a significant impediment to scaling.

In scaling the device, we have set $W_e \propto \gamma^2$ and $L_e \propto \gamma^0$. If all other widths and lengths in the device layout are scaled in the same proportions, then the HBT area, and the area of a given circuit, are proportional to γ^{-2}. The average wire length within the circuit is proportional to the square root of the IC area, and hence is proportional to γ^{-1}. Wiring delays, whether transmission-line delays or $C_{wire}\Delta V/\Delta I$ charging times, thus also scale correctly. Because of the fixed bulk metal resistivity, interconnect parasitic series resistance does not scale correctly, increasing as γ^2.

In scaled HBTs, base current is dominated by surface recombination and by currents conducted on the surface between the base–emitter junction and the base ohmic contact. Consequently, $I_b \propto n(T_{eb})L_e$, where $n(T_{eb})$ is the minority carrier density in the base at the emitter–base depletion region edge. Because $I_c \propto L_e W_e n(T_{eb})/T_b$, $\beta \propto W_e/T_b$. With the scaling laws mentioned earlier, $\beta \propto \gamma^{-3/2}$. Current gain decreases rapidly with scaling, and reduction of surface recombination and surface conduction is critical in deep submicron devices.

Finally, we reconsider scaling of the mesa HBT. For mesa HBTs, base and collector thickness, emitter and collector junction widths, emitter contact resistivity, and current density must all scale as discussed previously for undercut-mesa and transferred-substrate HBTs. In particular, the base–collector junction width must still scale as γ^{-2}. For a normal triple-mesa device, this then requires that the widths W_b of the base ohmic contacts (Fig. 1) scale as γ^{-2} while maintaining a fixed $R_{b,cont} = (\rho_s\rho_c)^{1/2}(1/2L_e)\coth(W_b/L_{\text{contact}})$. This can be accomplished by a combined reduction of both ρ_s and ρ_c and hence, a general analysis is exceedingly complex. As a limiting case with a highly scaled HBT, W_c must be very small, and hence, W_b will be much less than L_{contact}. In this case $R_{b,cont} \simeq \rho_c/2L_eW_b$, and hence constant $R_{b,cont}$ requires that the base ohmic contact resistivity scale as $\rho_c \propto \gamma^{-2}$. Transferred-substrate and undercut-mesa HBTs do not require this improvement of base contact resistivity with scaling.

To simultaneously increase HBT bandwidth in general circuits by $\gamma:1$, emitter and collector junction widths must vary as γ^{-2}, while maintaining constant junction lengths. Base thickness must vary as $\gamma^{-1/2}$ and collector thickness as γ^{-1}. Emitter current density and transistor and IC power density all increase in proportion to γ^2. The emitter contact structure must improve in proportion to γ^2. Power dissipation, reliability under high-current operation, required improvements in surface recombination velocity, and the required quality of the emitter ohmic contact are the most significant impediments to scaling. These relationships are summarized in Table II.

TABLE II
SCALING LAWS FOR HBTS: REQUIRED PROPORTIONAL CHANGE IN KEY RELEVANT HBT PHYSICAL PARAMETERS IN ORDER TO OBTAIN A $\gamma:1$ INCREASE IN BANDWIDTH IN AN ARBITRARY CIRCUIT. ADDITIONALLY, FOR MESA HBTS, BUT NOT TRANSFERRED-SUBSTRATE OR UNDERCUT-MESA DEVICES, THE BASE CONTACT RESISTIVITY ρ_v MUST SCALE AS γ^{-2}

parameter	symbol	scaling law
collector depletion thickness	T_c	γ^{-1}
base thickness	T_b	$\gamma^{-1/2}$
emitter-base junction width	W_e	γ^{-2}
collector-base junction width	W_c	γ^{-2}
emitter depletion thickness	T_{eb}	$\gamma^{-1/2}$
emitter parasitic resistivity	ρ_e	γ^{-2}
emitter junction area	A_e	γ^{-2}
emitter current	I_e	γ^0
emitter current density	J_e	γ^2
bias and signal voltages	V_{CE}, v_{ce}	γ^0
average interconnect length	L_{wire}	γ^{-1}
circuit area	–	γ^{-2}
device power density	–	γ^2
circuit power density	–	γ^2

III. TRANSFERRED-SUBSTRATE HBTS

Wide HBT bandwidths are obtained by scaling. In scaling for high f_τ, significant limits include high power density and high current density, demands for very low emitter parasitic resistance, and the collapse of $f_{\max}$ due to the extrinsic collector–base junction. Using the substrate transfer processes, this extrinsic junction can be reduced in size or eliminated. This permits either aggressive lithographic scaling *without* epitaxial scaling for greatly increased $f_{\max}$ at constant f_τ. Alternatively, if high values of both f_τ and $f_{\max}$ are sought, simultaneous lithographic and epitaxial scaling is required. With the extrinsic C_{cb} eliminated, operation at high current density and reduction of the emitter resistance are the key requirements for further scaling.

A. Growth and Fabrication

We first describe the epitaxial layer structure. The InGaAs base is typically 300–400 Å thick, has $2kT$ bandgap grading, and is Be-doped at $5 \cdot 10^{19}/\text{cm}^3$. The InGaAs collector is 2000–3000 Å thickness. A collector N^+ pulse-doped layer placed 400 Å from the base delays the onset of base push-out at high collector current densities. Although such pulse-doped layers have been used as electron launchers [41] in GaAs-based HBTs, our experimental data shows no significant effect of the launcher upon τ_c for InGaAs-collector HBTs.

Devices typically use Schottky collector contacts [42], although HBTs with N+ subcollector layers (ohmic-collector devices) have also been fabricated. While ohmic-collector devices have nonzero collector series resistance and hence, lower $f_{\max}$ [24], the 0.2 V barrier present in the Schottky-collector device increases the V_{ce} required to suppress base push-out at high current densities. Ohmic-collector devices thus show higher $f_{\max}$ under the low-V_{ce} conditions associated with current-mode-logic (CML). Schottky-collector devices are used for emitter-coupled-logic (ECL), where the operating V_{ce} is higher.

Fig. 9 shows the process flow. Standard fabrication processes [44] define the emitter–base junction, the base mesa, polyimide planarization, and the emitter contacts. The substrate transfer

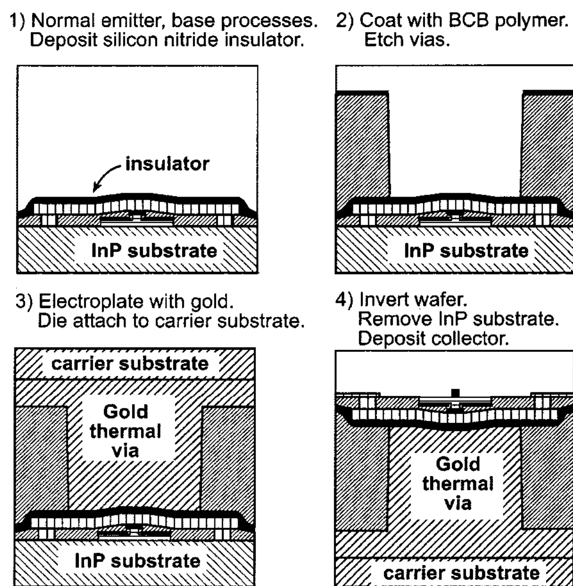


Fig. 9. Transferred-substrate HBT process flow.

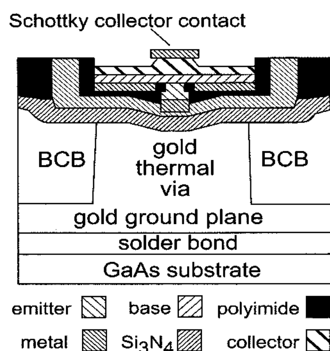


Fig. 10. Schematic cross section of a transferred-substrate HBT.

process commences with deposition of the PECVD Si_3N_4 insulator layer and the benzocyclobutene (BCB) transmission-line dielectric (5 μm thickness). Thermal and electrical vias are etched in the BCB. The wafer is electroplated to metallize the vias and to form the ground plane. The wafer is then solder-bonded to a GaAs carrier substrate. The InP substrate is removed in HCl and Schottky collectors are deposited, completing the process. Fig. 10 shows a detailed device cross section.

For the emitter–base junction, deep submicron scaling requires tight control of lateral undercutting during the base contact recess etch. To form the emitter, reactive-ion etching in $CH_4/H_2/Ar$, monitored with a HeNe laser, first removes the N^+ GaInAs emitter contact layer. A HCl/HBr/Acetic selective wet etch then removes the AlInAs emitter, stopping on the AlInAs/GaInAs emitter–base grade. By etching at 10 °C, the etch rate is slowed, and a controlled emitter undercut is formed. The undercut both narrows the emitter and serves (as normal) to define the liftoff edge in the self-aligned base contact deposition. A timed nonselective wet Citric/H_3PO_4/H_2O_2 etch then removes the base–emitter grade. Etch selectivity in both the RIE and HCl/HBr/Acetic etches aids in etch-depth control, and we are able to reproducibly etch ~100 Å into the base without use of surface contact resistance probing as a process monitor.

In defining submicron collector–base junctions, use of the Schottky-collector contact eliminates the need for an etch of similar precision through an N^+ collector ohmic contact layer. The collector junction is defined by the stripe width of the deposited metal. Subsequent to collector deposition, a self-aligned wet etch of ~1000 Å depth removes the collector junction sidewalls (eliminating fringing fields) and reduces the collector junction width by ~2000 Å. The step, intended to reduce C_{cb}, generally provides a greater increase $f_{\max}$ than would be expected from the observed reduction in collector junction width.

Given the unusual features of the substrate transfer process, IC yield is a significant concern. The transistors and ICs reported here have all been developed by a team whose average size, over time, is approximately 12 Ph.D. students working in a university cleanroom, who are responsible for all aspects of technology, including crystal growth, processing, IC design, and testing. It is therefore difficult to separate yield difficulties inherent to the substrate transfer process with yield difficulties associated with limited manpower available to address process control and the limited quality of university cleanroom equipment. Process failures do result from failure of the substrate transfer steps (failure of solder adhesion, failure, for unknown causes, of the substrate removal selective wet etch), but equally, process failures arise in HBT fabrication steps unrelated to that of substrate transfer. Significant among these are excessive undercut in the emitter–base junction etch, failure of the emitter–base RIE or selective wet etches, emitter–base short circuits forming during base contact liftoff, liftoff failures in interconnect metals, poor adhesion of resistor metal, and variation of resistor sheet resistivity. Given the resources available to a larger industrial group, various process difficulties, whether associated with or independent of substrate transfer, could be addressed. We believe the most serious fundamental difficulties are with the solder bonding and with the small wafer expansion after bonding (below), which most probably results from mechanical creep of the solder under exposure to stress and temperature cycles. Solder bonding also is presently limited to small wafer sizes (quarters of 50 mm wafers). More dimensionally stable alternatives, possibly spin-on glasses, should be found for both the solder and the BCB dielectric.

Presently, the largest working ICs fabricated in the process are 150-HBT ADCs and 250-HBT binary adders. The most significant process difficulty is dimensional change of the wafer during substrate transfer. Presently, wafers show 3×10^{-4} fractional expansion after transfer, resulting in ±0.5 μm misregistration (during collector lithography) at the edges of the stepper exposure field if a 3 mm reticle is employed. We presently adjust the dimensions of the collector mask as a correction. At the expense of increased effort during collector lithography, a smaller exposure reticle size can be used for the collector lithography than for the steps preceding substrate transfer. The relative sizes of the emitter and collector junctions are determined by lithographic alignment tolerances, and the collector stripe width must exceed the emitter stripe width by twice the lithographic alignment tolerance. Our electron-beam lithography system can align

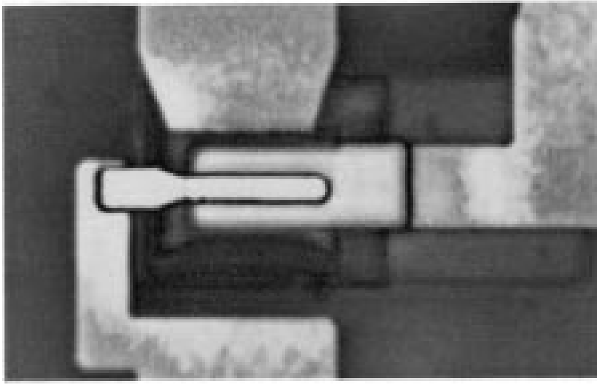


Fig. 11. Transferred-substrate HBT defined by optical projection lithography.

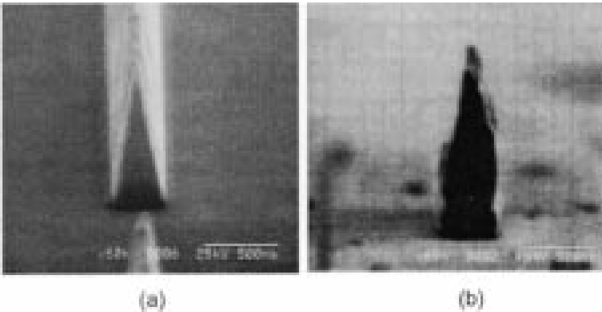


Fig. 12. E-beam HBT: (a) 0.3 μm width emitter contact metal prior to the junction etch and (b) $\sim$0.3 μm emitter–base junction subsequent to the junction etch.

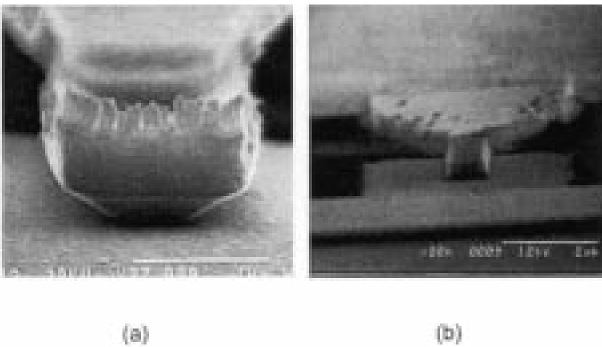


Fig. 13. E-beam HBT: (a) completed devices, viewed from the collector surface, showing 0.4 μm and (b) 0.8 μm width Schottky collector contacts.

to 0.1 μm registration, and our projection lithography system aligns to 0.1–0.3 μm registration, depending on the time since maintenance. Modern projection lithography systems are *much better* 0.35-μm-resolution steppers have $\sim$300 Å registration tolerance.

B. Device Results

Transferred-substrate HBTs have been fabricated using contact lithography at 1–2 μm resolution using a 0.5 μm stepper and using electron-beam lithography. Fig. 11 shows a device defined by optical projection lithography. Figs. 12 and 13 show HBT emitter–base and collector–base junctions defined by electron-beam lithography.

Fig. 14 shows microwave gains for a deep submicron device fabricated using electron-beam lithography, reported by Lee *et al.* [45]. The base and collector layers are 400 Å and 3000 Å thick, while the emitter and collector junction dimensions are 0.4 μm $\times$ 6 μm and 0.7 μm $\times$ 10 μm. Biased at $V_{ce} = 1.2$ V and $I_c = 6$ mA ($J_e = 2.5 \times 10^5$ A/cm^2), the device exhibits 204 GHz f_τ. If extrapolated at -20 dB/decade, a 1080 GHz $f_{\max}$ is determined. We note however, that such a 10 : 1 extrapolation must be treated with considerable caution.

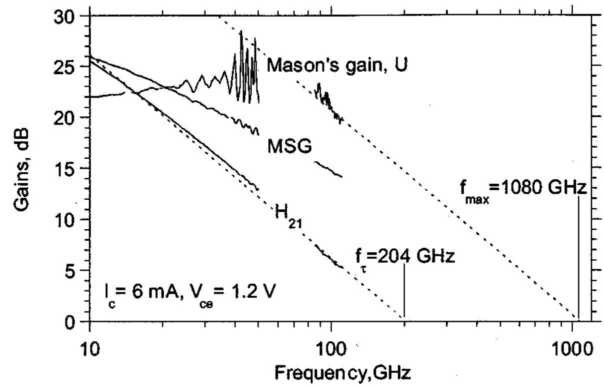


Fig. 14. Gains of a 0.4 μm $\times$ 6 μm emitter and 0.7 μm $\times$ 10 μm collector HBT fabricated using electron-beam lithography. Theoretical -20 dB/decade (H_{21}, U) gain slopes are indicated. The device exhibits an *extrapolated* 1.08 THz $f_{\max}$.

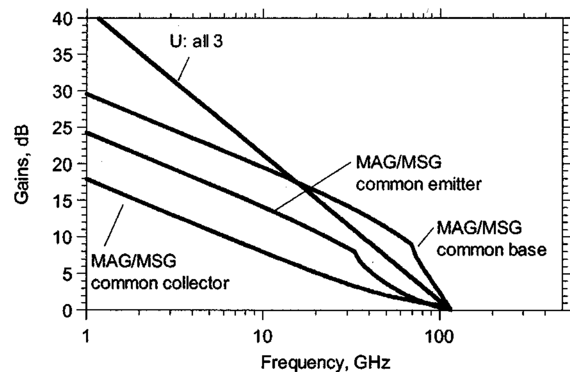


Fig. 15. Variation of transistor gains with frequency, computed from a hybrid-π HBT model. Shown are the maximum available/maximum stable gains (MAG/MSG) in common-emitter, common-base, and common collector mode, and Mason's invariant (U), the unilateral gain.

We have extrapolated Mason's invariant (unilateral) gain at -20 dB/decade to determine the extrapolated $f_{\max}$. Mason's gain [48] is invariant with respect to embedding the device in a lossless reciprocal network, and consequently, is independent of pad inductive or capacitive parasitics and independent of the transistor configuration (common–emitter versus common–base). For HBTs well-modeled by a hybrid-π equivalent circuit, Mason's gain conforms closely to a -20 dB/decade variation with frequency (Fig. 15). In marked contrast, the maximum available/maximum stable gain is a function of the transistor configuration and shows no fixed variation with frequency. $f_{\max}$ is unique. At $f = f_{\max}$, the MAG/MSG and U are both 0 dB.

Device gains were measured over 45 MHz–50 GHz and 75–110 GHz using a microwave network analyzer and microwave wafer probes. To avoid uncorrectable measurement errors (in S_{12}, hence U) arising from variable probe–probe

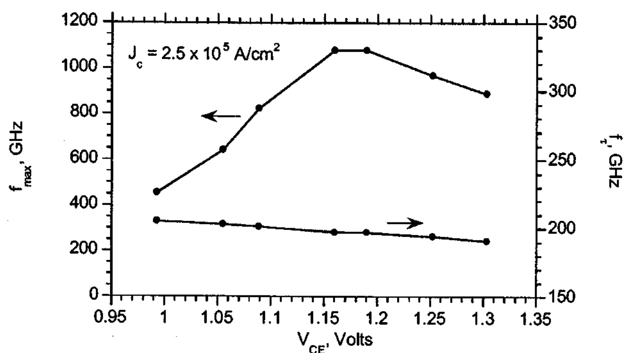


Fig. 16. Variation of f_τ and $f_{\max}$ with collector–emitter voltage.

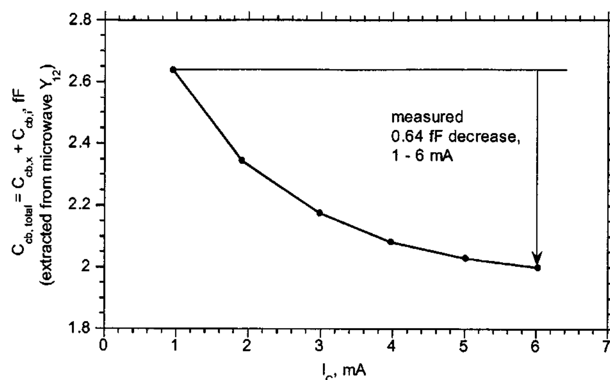


Fig. 17. Collector–base capacitance extracted from Y_{12} versus emitter current.

electromagnetic coupling, the HBTs are separated from their probe pads by long on-wafer 50 Ω microstrip lines. On-wafer line-reflect-line calibration standards are used to de-embed the transistor S-parameters [46]. Before extracting HBT power gains to extrapolate f_τ and $f_{\max}$, it is essential to verify the on-wafer calibration through measurement of known standards to verify that the probe–probe parasitic coupling (as measured from the S_{12} of an on-wafer open-circuit standard) is at least 15–20 dB smaller than the measured transistor S_{12} and to ensure that the transistor's measured S-parameters have a variation with frequency, which conforms closely to that of a hybrid-π model. In the 75–110 GHz band, with high-$f_{\max}$ (hence, very low S_{12}) HBTs, we have found that these requirements cannot be met using commercially-provided calibration substrates or with probe pads immediately adjacent to the transistor under test. The on-wafer LRM method is required, and the probe–probe separation must be at least 500 μm for all calibration test structures and for the device under test. In addition to the 10 : 1 extrapolation to 1.08 THz $f_{\max}$, the very high power gain at 110 GHz also results in significant measurement variability, with repeated calibrations at the same bias point giving extrapolated $f_{\max}$ varying from 1.0 to 1.3 THz.

We have recently acquired a 140–220 GHz network analyzer with on-wafer probes, and are now developing methods to obtain precision HBT measurements in this band. Preliminary HBT measurements on a recently-processed submicron HBT wafer indicate (Fig. 19) 10 dB maximum stable gain at 200 GHz (the device is potentially unstable even at this high frequency) [36]. Our calibration accuracy in this band is not yet sufficient for measurement of U. We have also recently demonstrated single-transistor tuned HBT amplifiers at 178 GHz [38] with as high as 6.0 dB circuit gain [37]. This indicates substantial transistor available power gain at 200 GHz. Given current measurement data, the 1.1 THz extrapolated $f_{\max}$ is presently best viewed simply as an extremely high measured power gain at 100 GHz.

C_{cb} cancellation contributes substantially to the $f_{\max}$ obtained. At zero current, $C_{cb,\,e} = \epsilon A_e/T_c$ =0.9 fF. The measured variation of f_τ versus V_{ce} (Fig. 16) indicates $\partial\tau_c/\partial V_{ce} \sim 0.18$ ps/V, predicting ∼0.9 fF reduction in $C_{cb,\,e}$ from $I_c = 1$ mA to $I_c = 6$ mA. The *total* collector–base capacitance C_{cb} is determined from the measured variation with frequency of the imaginary part of the admittance parameter $\mathrm{Im}[Y_{12}] = j\omega C_{cb}$. The total C_{cb} determined from Y_{12} (Fig. 17) shows a 0.64 fF

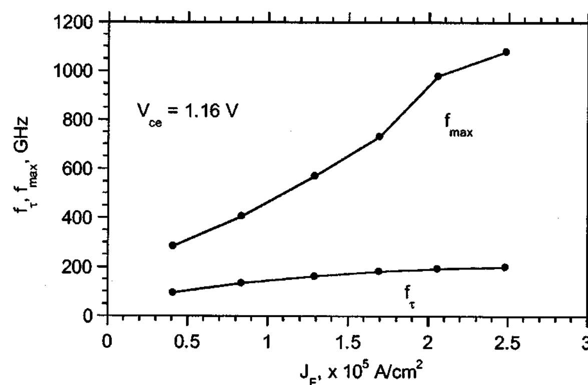


Fig. 18. Variation of f_τ and $f_{\max}$ with emitter current density.

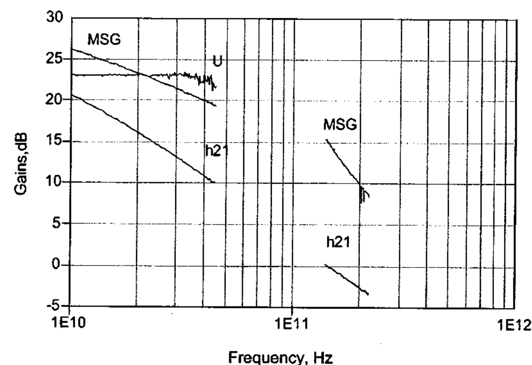


Fig. 19. Gains in the 10–45 GHz and 140–220 GHz bands of a 0.5 μm × 6 μm emitter, 0.7 μm × 6 μm collector HBT with a 300 nm collector thickness, biased at 3.6 mA I_c and 1.2 Volts V_{ce}. The device is potentially unstable at all tested frequencies.

decrease between 1 mA and 6 mA I_c. The measured variation in the total C_{cb} primarily reflects variation in the capacitance $C_{cb,\,e}$. The reduction $C_{cb,\,e}$ with bias current results in a rapid increase in $f_{\max}$ with bias (Fig. 18).

Fig. 20 shows the small-signal hybrid-π model. The measured S-parameters (Fig. 21), h_{21}, and U show good correlation with the hybrid-π model, and the model parameters are consistent with measured bulk and sheet resistivities and junction capacitances. The HBT output conductance is dominated by R_{cb}, which represents variation of collector–base leakage with

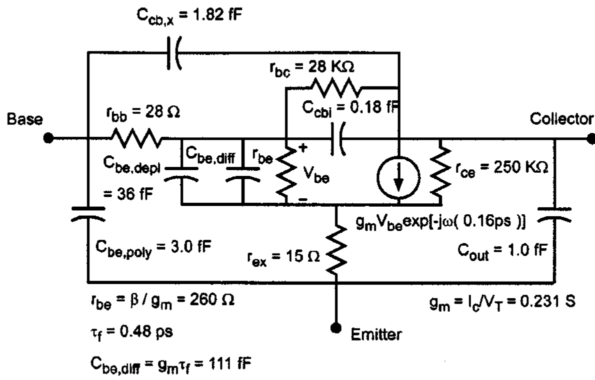


Fig. 20. Device equivalent circuit model at $V_{ce} = 1.2$ V and $I_c = 6$ mA.

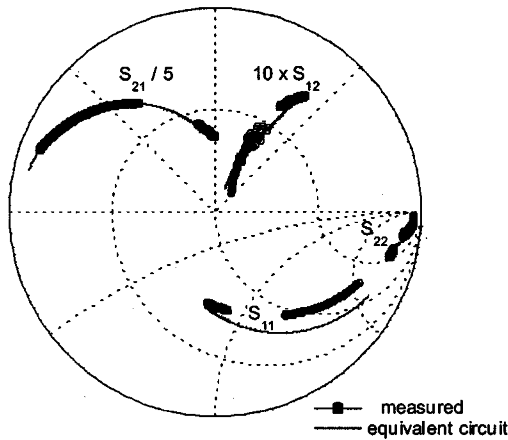


Fig. 21. Measured 45 MHz–50 GHz and 75–110 GHz device S-parameters at $V_{ce} = 1.2$ V and $I_c = 6$ mA. The solid line represents S-parameters of the equivalent circuit model (Fig. 20).

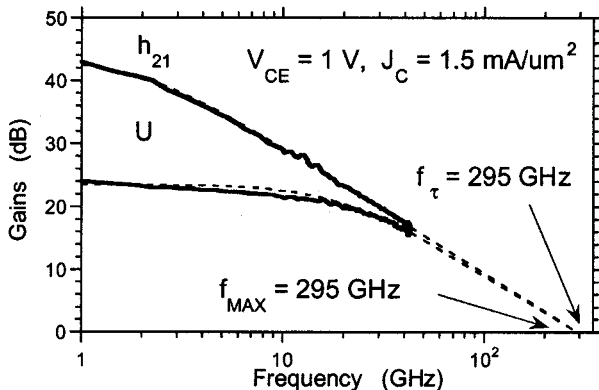


Fig. 22. Measured RF gains for an HBT with a 300 Å base with 52 meV grading and a 2000 Å collector, measured at $V_{ce} = 1$ V and $J_e = 1.5 \cdot 10^5$ A/cm^2. The emitter and collector junctions are 1 μm × 8 μm and 2 μm × 8.5 μm.

bias. This is likely due to impact ionization. Base-width modulation in HBTs is negligible, hence, R_{ce} is very large. $C_{be,poly}$ is a metal–polyimide–metal overlap capacitance between the emitter and base contacts (Fig. 10), which contributes an additional $C_{be,poly}(R_{ex} + kT/qI_c) = 60$ fs to the transistor forward delay.

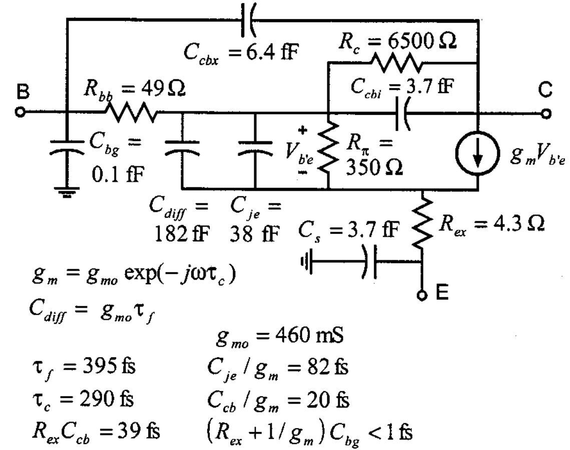


Fig. 23. Equivalent circuit model and extracted components of τ_{ec} for the HBT of Fig. 22.

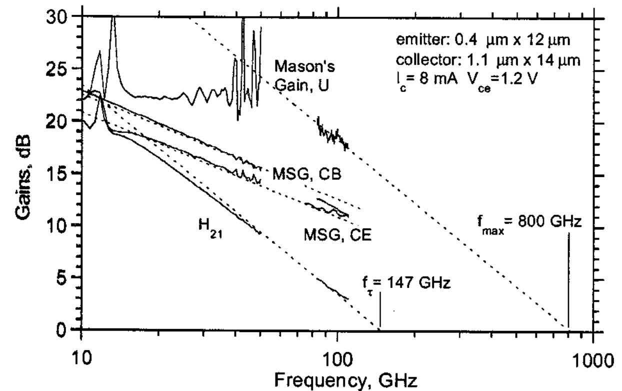


Fig. 24. Measured 10–40 GHz and 80–110 GHz gains of a submicron HBT fabricated by optical projection lithography, showing the current gain H_{21}, the unilateral power gain U, and the maximum stable gain MSG (note that $k < 1$ at all tested frequencies for common-emitter and common-base). The *extrapolated* 800 GHz $f_{\max}$ has significant experimental uncertainty.

Neither contact lithography nor electron-beam lithography is suitable for fabrication of large ICs. We have used optical projection lithography to form devices with 0.4 μm emitters and have obtained high measured power gains (Fig. 24), leading to an extrapolated 800 GHz $f_{\max}$. As with the electron-beam devices, $f_{\max}$ of the device of Fig. 24 will be less than 800 GHz if unmodeled electron transport physics produce a >20 dB/decade variation in power gain at frequencies above 110 GHz.

With the exception of reactively-tuned circuits, for which $f_{\max}$ is the sole determinant of circuit bandwidth, circuit design generally requires high values for both f_τ and $f_{\max}$. Fig. 22 shows RF gains for an HBT with 0.6 μm × 8 μm emitter and 2 μm × 12 μm collector junctions, a 300 Å thick base with 52 meV bandgap grading, and a 2000 Å thick collector [49]. The device exhibits simultaneous 295 GHz f_τ and $f_{\max}$ [49]. Examining components of $\tau_{ec} = 1/2\pi f_\tau$ Fig. 23, the emitter and base transit times comprise 73% of the total forward delay. The emitter parasitic resistance is nevertheless a significant impediment to further scaling for high f_τ, as a 2 : 1 thinning of the collector to reduce τ_c by 150 fs would increase $R_{ex}C_{cb}$ by 39 fs. To obtain further increases in f_τ, the collector must

be thinned, current density further increased, and the emitter parasitic resistance improved. Note that the transistor was characterized using the on-wafer LRL calibration method with extended reference planes. By this method, ambiguity in stripping the ~20 fF pad capacitance is eliminated. This is of significance in characterizing a transistor with ~300 GHz f_τ, hence, ~500 fs τ_{ec}. A 10 fF error in stripping pad capacitance would result in a (10 fF) $\cdot R_{ex}$ =43 fs error in determination of τ_{ec}; almost a 10% error in f_τ.

Device scaling also reduces DC current gain. Base current in narrow-emitter InAlAs/InGaAs HBTs is predominantly due to conduction on the exposed InGaAs base surface between the emitter mesa and the base ohmic contact. β decreases with emitter width but increases as the base is thinned, as base bandgap grading is increased, and (at the expense of $f_{\max}$) as the emitter–base spacing is increased. β >50 has been obtained with 0.2 μm emitters. High current gain can be obtained with submicron devices through suppression of surface conduction by a self-aligned emitter–base heterojunction ledge.

C. Interconnects and Thermal Management

In developing an integrated circuit technology for microwave mixed-signal ICs, ~100 GHz digital logic, and 100–300 GHz monolithic transmitters and receivers, significant issues in interconnects, packaging, and thermal management must also be addressed. Wiring parasitics, including line capacitance per unit length, line delay per unit length, ground via inductance, and parasitic ground return inductance must all be minimized. Ground via inductance (~12 pH, or j7.5 Ω at 100 GHz) in standard 100-μm-substrate microstrip MIMICs makes low-impedance source/emitter grounding difficult in >100 GHz ICs. The interconnects must have low capacitance and low delay per unit length and the wire lengths, hence, transistor spacings must be small. Given that fast HBTs operate at ~10^5 A/cm^2 current density, efficient heat sinking is then essential. To provide predictable performance, interconnects of more than a few ps length must have a controlled characteristic impedance. To prevent circuit–circuit interaction through ground-circuit common-lead inductance ("ground loops"), the IC technology must provide an integral low inductance (unbroken) ground plane for ground-return connections.

Ground-return inductance between the IC and package results in "ground bounce" and interaction between the ICs input and output lines. For ICs with top-surface (coplanar-wave-guide) ground connections and multiple input/output connections, ground bounce between IC and package will prevent 100 GHz operation. For an IC with N_{signal} signal lines of impedance Z_0, risetime ΔT, and voltage swing V_{signal} and N_{ground} grounding bond wires of inductance $L_{\text{bond}} \simeq 0.6$ pH/μm $\cdot$ 300 μm, the package-IC ground bounce is $V_{\text{bounce}} = V_{\text{signal}} N_{\text{signal}} L_{\text{bond}} / N_{\text{ground}} Z_0 \Delta T$. For ground bounce equal to 10% of the signal amplitudes, a 100-GHz clock rate IC must have $N_{\text{ground}}/N_{\text{signal}} = 5$–10, and 80%–90% of the IC bond-pads must be devoted to IC grounding. Reported 10 GHz clock rate ICs devote ~50% of IC pads for grounding. For mixed-signal and communications ICs, signal coupling through ground bounce must be much smaller than 10% of the digital I/O interface levels. Consequently, common-lead inductance between the IC and package ground systems must be made vanishingly small.

In addition to wide bandwidth transistors, the substrate transfer process provides thermal bias for HBT heatsinking, and microstrip transmission-line interconnects on a low dielectric constant substrate ($\epsilon_r = 2.7$) with bias, ground plane, and three levels of interconnects. At 5 μm length, the grounding vias are 20 : 1 shorter than in typical 100-μm-substrate microstrip MIMICs, reducing ground via inductance by over an order of magnitude. The process also incorporates NiCr resistors and Si_3N_4 MIM capacitors.

Presently, thermal resistance is dominated by temperature gradients internal to the transistor itself, arising from the low thermal conductivity of the InAlAs emitter and InGaAs base and collector layers. Thus, allowable power per unit HBT emitter area remains comparable to mesa HBTs. There is also a small temperature gradient (~15 C for an HBT operating a 1 V and 10^5 A/cm^2) across the SiN insulator. For power transferred-substrate HBTs, the use of high-thermal-conductivity InP emitter and collector epitaxial layers will greatly increase allowable power per unit HBT junction area. This is being pursued. To tolerate high power densities, the NiCr resistors must have thermal vias, which results in significant parasitic capacitance. Pull-up resistors in ECL do not require the thermal via.

IV. Integrated Circuit Results

A number of ICs have been fabricated in the transferred-substrate process. Here we show significant results. Master–slave latches [51] configured as 2 : 1 static frequency dividers were fabricated using optical projection lithography. These designs employed HBTs with 0.6 μm emitter and 1.4 μm collector junctions widths, with the devices operating at 1.8×10^5 A/cm^2 current density. Critical interconnects between stages are implemented as short doubly-terminated 100 Ω transmission lines at the center of the IC. The terminations use a *small* amount of series inductive peaking (Fig. 25). Emitter–follower buffers increase logic speed but can induce strong ringing, and L–R networks provide shunt loading of emitter–follower outputs and damp the emitter–follower pulse response. The overall chip area is 1.0 × 0.4 mm (Fig. 26). The latch dissipates 880 mW from a −3.9 V supply. Circuit simulations, which included all significant device and interconnect parasitics, predicted a 95 GHz maximum clock frequency when the latch is configured as a 2 : 1 static frequency divider. In testing, the IC functions correctly at all frequencies in the 5–75 GHz range [52] (Fig. 27).

A number of high speed analog ICs have been fabricated in the transferred-substrate HBT process. Among these are 80 GHz distributed amplifiers [39] (Fig. 28), 50 GHz broadband differential amplifiers for optical fiber receivers [54], and broadband Darlington and f_τ-doubler resistive feedback amplifiers (Fig. 29). Fig. 30 shows the measured gain versus frequency of a Darlington resistive feedback amplifier [55], [40]. Greater than 400 GHz gain-bandwidth product is obtain from a single

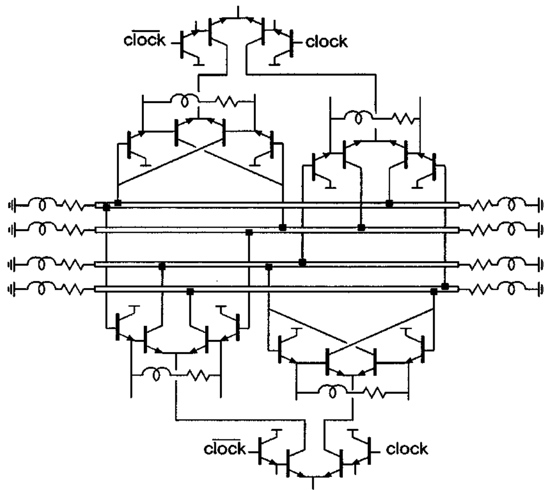


Fig. 25. ECL master–slave latch configured as a 2 : 1 static frequency divider.

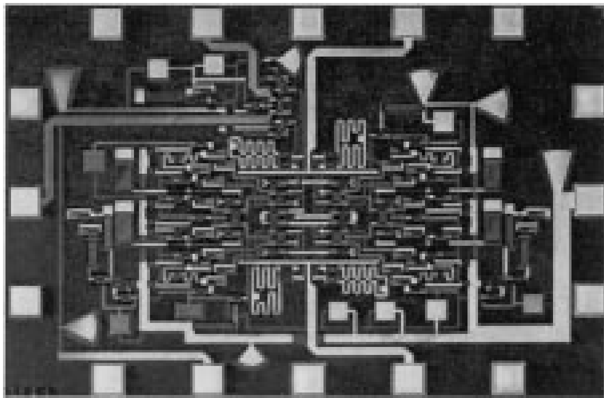


Fig. 26. The 75 GHz master–slave latch. The IC contains 70 HBTs.

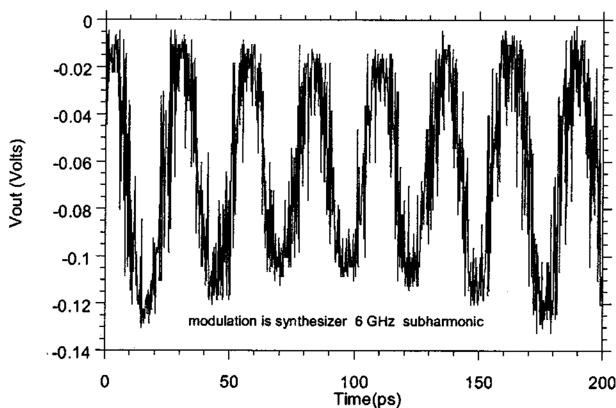


Fig. 27. The 37.5 GHz output waveform for the static frequency divider for a 75 GHz input.

Darlington stage. Tuned mm-wave amplifiers have also been demonstrated in the transferred-substrate process, including a 75 GHz amplifier [56] (Fig. 31) and recently, a 180-GHz tuned amplifier [38].

Larger digital and mixed-signal ICs have also been fabricated in the transferred-substrate process. We have recently fabricated

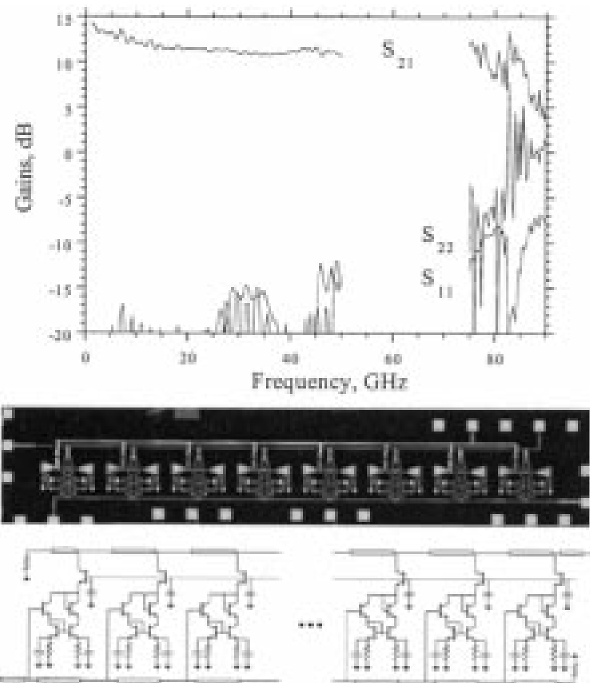
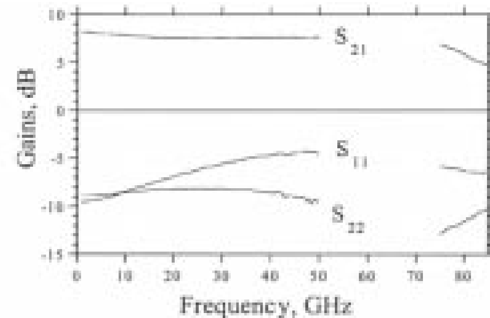


Fig. 28. Distributed amplifier in the transferred-substrate process. The amplifier exhibits 11.5 dB gain and approximately 80 GHz bandwidth.



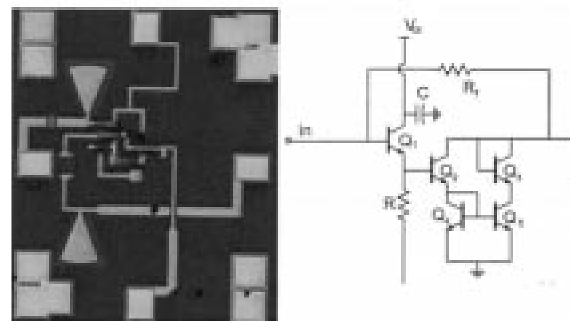


Fig. 29. f_τ-doubler resistive feedback amplifier with 8.2 dB low-frequency gain and a DC-80 GHz 3-dB-bandwidth.

Δ–Σ modulators in the technology (Fig. 32) [57]. These ICs have operated at an 18 GHz clock rate.

Larger digital circuits in development include sum and carry generation circuits for pipelined adder-accumulators. These circuits use four-level series-gated current-steering logic and merged logic-latch circuits to obtain the equivalent of two AND, two OR, and two latching operations in a 50 ps clock period [58].

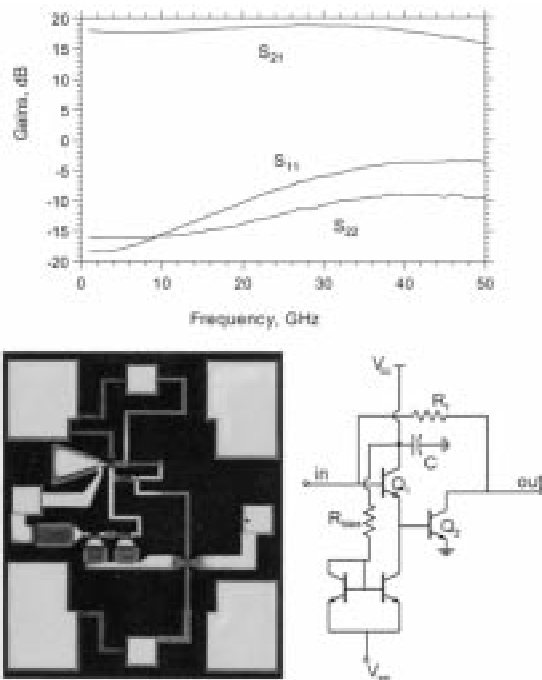


Fig. 30. Measured S-parameters of a single-stage Darlington feedback amplifier. The amplifier exhibits 18 dB baseband gain, a 3-dB bandwidth greater than 50 GHz, and greater than 400 GHz gain-bandwidth product.

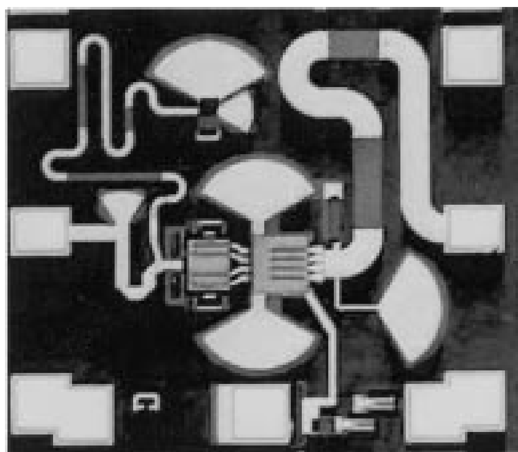


Fig. 31. W-band cascode medium-power amplifier. The amplifier has 7.5 dB gain and produces 10 dBm saturated output power at 78 GHz.

V. Conclusions

Bipolar IC bandwidths have increased tremendously since the first demonstration of (bipolar) integrated circuits 40 years ago. Device, IC, and application bandwidths will continue to increase. With MOS transistors and III–V HEMTs (FETs), improved device bandwidths are obtained by lateral scaling (shorter gate lengths) combined with vertical scaling (thinner gate-channel insulating barriers) and progressive improvements in source/drain ohmic contacts. With bipolar transistors, improved bandwidths are obtained by vertical scaling (thinner base and collector layers), combined with lateral scaling (narrower collector and emitter junctions), increased current density, and progressive improvements in emitter ohmic contacts. While III–V HBTs benefit from strong heterojunctions, high mobilities, and high electron velocities, Si/SiGe bipolar transistors have been much more aggressively scaled, both in lithographic dimensions and emitter current density. Essential to the future success of III–V HBTs is submicron junction scaling and greatly increased current densities.

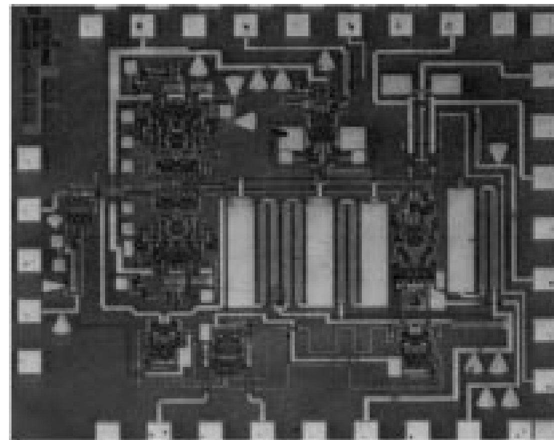


Fig. 32. Δ–Σ ADC fabricated in the transferred-substrate process. The IC contains approximately 150 HBTs and operates at 18 GHz clock rate.

While bipolar ICs are much smaller than CMOS VLSI ICs, clock frequencies are much higher. In both technologies, thermal management and signal integrity are major limits to performance. As bipolar technologies evolve toward complex ICs operating at a 100 GHz clock, an increasing fraction of the total circuit connections will be terminated transmission lines of controlled characteristic impedance and minimal dielectric loading.

References

[1] H. Kroemer, "Heterostructure bipolar transistors and integrated circuits," *Proc. IEEE*, vol. 70, pp. 13–25, Jan. 1982.

[2] P. Asbeck, F. Chang, K.-C. Wang, G. Sullivan, and D. Cheung, "GaAs-based heterojunction bipolar transistors for very high performance electronic circuits," *Proc. IEEE*, vol. 81, pp. 1709–1726, Dec. 1993.

[3] M. Sokolich, D. P. Docter, Y. K. Brown, A. R. Kamer, J. F. Jensen, W. E. Stanchina, S. Thomas, III, C. H. Fields, D. A. Ahmari, M. Lui, R. Martinez, and J. Duvall, "A low power 52.9 GHz static frequency divider in a manufacturable 180 GHz AlInAs/InGaAs HBT IC technology," in *Tech. Dig., IEEE GaAs IC Symp.*, Atlanta, GA, Nov. 1–4, 1998, pp. 117–120.

[4] P. K. Hughes, J. Y. Choe, and J. Zolper, "Advanced multifunctional RF system (AMRFS)," in *Tech. Dig., Government Microcircuits Application Conf. (GOMAC)*, vol. 25, Anaheim, CA, Mar. 2000, pp. 194–197.

[5] H. Suzuki, K. Watanabe, K. Ishikawa, H. Masuda, K. Ouchi, T. Tanoue, and R. Takeyari, "InP/InGaAs HBT ICs for 40 Gbit/s optical transmission systems," in *Tech. Dig., IEEE GaAs IC Symp.*, Anaheim, CA, 1997, pp. 215–218.

[6] H. M. Rein, E. Gottwald, and T. F. Meister, "Si-bipolar—A potential candidate for high-speed electronics in 20 and 40 Gb/s TDM systems?," in *Tech. Dig., Ultrafast Electronics and Optoelectronics Conf.*, Incline Village, NV, 1997, pp. 118–120.

[7] J. C. Candy and G. C. Temes, Eds., *Oversampling Delta–Sigma Data Converters*. Piscataway, NJ: IEEE Press, 1992.

[8] D. C. Larson, "High speed direct digital synthesis techniques and applications," in *Tech. Dig., IEEE GaAs IC Symp.*, 1998, pp. 209–212.

[9] J. Jensen, G. Raghavan, A. Cosand, and R. Walden, "A 3.2 GHz second order sigma–delta modulator implemented in the InP HBT technology," *IEEE J. Solid-State Circuits*, vol. 30, pp. 119–127, Oct. 1995.

[10] S. Subbanna, J. Johnson, G. Freeman, R. Volant, R. Groves, D. Herman, and B. Meyerson, "Prospects for silicon germanium based technology for very high speed circuits," in *IEEE MTT-S Dig.*, Boston, MA, June 2000.

[11] E. F. Crabbe, B. S. Meyerson, D. L. Harame, J. M. C. Stork, A. Megdanis, J. Cotte, J. Chu, M. Gilbert, C. Stanis, J. H. Comfort, G. L. Patton, and S. Subbanna,, "113-GHz f_τ graded-base SiGe HBTs," in *51st Device Research Conf., 1993; Abstract in IEEE Trans. Electron Devices*, vol. 40, 1993, p. 2100.

[12] K. Ohhata, T. Masuda, E. Ohue, and K. Washio, "Design of a 32.7-GHz bandwidth AGC amplifier IC with wide dynamic range implemented with SiGe HBT," *IEEE J. Solid-State Circuits*, vol. 34, pp. 1291–1297, Sept. 1999.

[13] E. F. Crabbe, J. H. Comfort, J. D. Cressler, J. Y.-C. Sun, and J. M. C. Stork, "High-low polysilicon-emitter SiGe-base bipolar transistors," *IEEE Electron Device Lett.*, vol. 4, pp. 478–480, Oct. 1993.

[14] S. Yamahata, K. Kurishima, H. Ito, and Y. Matsuoka, "Over-220-GHz-f_τ-and-$f_{\max}$ InP/InGaAs double-heterojunction bipolar transistors with a new hexagonal-shaped emitter," in *IEEE GaAs IC Symp. Tech. Dig.*, New York, 1995, pp. 163–166.

[15] H. Kroemer, "Two integral relations pertaining to the electron transport through a bipolar transistor with a nonuniform energy gap in the base region," *Solid State Electron.*, vol. 28, pp. 1101–1103, 1985.

[16] B. G. Streetman, *Solid State Electronic Devices*. Englewood Cliffs, NJ: Prentice-Hall, 1990.

[17] S. Laux and W. Lee, "Collector signal delay in the presence of velocity overshoot," *IEEE Electron Device Lett.*, vol. 11, pp. 174–176, Apr. 1990.

[18] T. Ishibashi, "Influence of electron velocity overshoot on collector transit times of HBTs," *IEEE Trans. Electron Devices*, vol. 37, pp. 2103–2105, Sept. 1990.

[19] M. Littlejohn, K. W. Kim, and H. Tian, "High-field transport in InGaAs and related heterostructures," in *Properties of Lattice-Matched and Strained Indium Gallium Arsenide*, P. Bhattacharya, Ed. London, U.K.: INSPEC, 1993.

[20] E. P. O'Reilly, "Band structure of InP: Overview," in *Properties of Indium Phosphide*. London, U.K.: INSPEC, 1991.

[21] C. T. Kirk, "A theory of transistor cutoff frequency (f_τ) fall-off at high current density," *IEEE Trans. Electron Devices*, vol. ED-9, p. 164, 1962.

[22] M. J. W. Rodwell, S. T. Allen, R. Y. Yu, M. G. Case, M. Reddy, E. Carman, J. Pusl, M. Kamegawa, Y. Konishi, and R. Pullela, "Active and nonlinear wave propagation devices in ultrafast electronics and Optoelectronics," *Proc. IEEE*, vol. 82, pp. 1037–1058, July 1994.

[23] *HP-EESOF Series IV Microwave Circuit Simulation Program*. Palo Alto, CA: Hewlett-Packard.

[24] M. Vaidyanathan and D. L. Pulfrey, "Extrapolated $f_{\max}$ of heterojunction bipolar transistors," *IEEE Trans. Electron Devices*, vol. 46, pp. 301–309, Feb. 1999.

[25] ——, private communication.

[26] Y. Betser and D. Ritter, "Reduction of the base collector capacitance in InP/GaInAs heterojunction bipolar transistors due to electron velocity modulation," *IEEE Trans. Electron Devices*, vol. 46, pp. 628–633, Apr. 1999.

[27] L. H. Camnitz and N. Moll, "An analysis of the cutoff-frequency behavior of microwave heterojunction bipolar transistors," in *Compound Semiconductor Transistors*, S. Tiwari, Ed. Piscataway: IEEE Press, 1992, pp. 21–45.

[28] R. W. H. Engelmann and C. A. Liechti, "Bias dependence of GaAs and InP MESFET parameters," *IEEE Trans. Electron Devices*, vol. ED-24, pp. 1288–1296, Nov. 1977.

[29] M.-C Ho, R. A. Johnson, W. J. Ho, M. F. Chang, and P. M. Asbeck, "High-performance low-base–collector capacitance AlGaAs/GaAs heterojunction bipolar transistors fabricated by deep ion implantation," *IEEE Electron Device Lett.*, vol. 16, pp. 512–514, Nov. 1995.

[30] W. Liu, D. Hill, H. F. Chau, J. Sweder, T. Nagle, and J. Delany, "Laterally etched undercut (LEU) technique to reduce base–collector capacitance in heterojunction bipolar transistors," in *Tech. Dig., IEEE GaAs IC Symp.*, San Diego, CA, 1995, pp. 167–170.

[31] A. Gutierrez-Aitken, E. Kaneshiro, J. Matsiu, J. Matsiu, D. Sandai, J. Notthoff, P. Chin, and A. Oki, "Cantilever base DHBT for high-speed digital applications," *Int. J. High-Speed Electron. Syst.*, vol. 11, no. 1, 2001.

[32] T. Oka, K. Hirata, K. Ouchi, H. Uchiyama, K. Mochizuki, and T. Nakamura, "Small-scaled InGaP/GaAs HBTs with WSi/Ti base electrode and buried SiO_2," *IEEE Trans. Electron Devices*, vol. 45, pp. 2276–2282, Nov. 1998.

[33] H. Shimawaki, Y. Amamiya, N. Furuhata, and K. Honjo, "High $f_{\max}$ AlGaAs/InGaAs and AlGaAs/GaAs HBTs with p^+/p regrown base contacts," *IEEE Trans. Electron Devices*, vol. 42, pp. 1735–1744, Oct. 1995.

[34] T. Oka, K. Hirata, K. Ouchi, H. Uchiyama, T. Taniguchi, K. Mochizuki, and T. Nakamura, "Advanced performance of small-scaled InGaP/GaAs HBTs with f_τ over 150 GHz and $f_{\max}$ over 250 GHz," in *Proc. 1998 IEEE Int. Electron Device Meeting*, San Francisco, CA, Dec. 6–9, pp. 653–656.

[35] Y. Matsuoka, S. Yamahata, K. Kurishima, and H. Ito, "Ultrahigh-speed InP/InGaAs double-heterostructure bipolar transistors and analysis of their operation," *Jpn. J. Appl. Phys.*, vol. 35, pp. 5646–5654, 1996.

[36] M. Urteaga, D. Scott, T. Mathew, S. Krishnan, Y. Wei, M. Dahlstrom, and M. J. W. Rodwell, "Characteristics of submicron HBTs in the 140–220 GHz band," in *2001 IEEE Device Research Conf.*. South Bend, IN, June 2001.

[37] M. Urteaga, D. Scott, T. Mathew, S. Krishnan, Y. Wei, and M. J. W. Rodwell, "Single-stage G-band HBT amplifier with 6.3 dB gain at 175 GHz," in *Proc. 2001 IEEE GaAsIC Symp.*, Baltimore, MD, Oct. 2001.

[38] ——, "185 GHz monolithic amplifier in InGaAs/InAlAs transferred-substrate HBT technology," in *2001 Microwave Theory and Techniques Int. Microwave Symp.*, May 2001.

[39] S. Krishnan, S. Jaganathan, T. Mathew,, Y. Wei, and M. J. W. Rodwell, "Broadband HBT amplifiers," in *2000 IEEE Cornell Conf. High Speed Electronics*. Ithaca, NY.

[40] S. Krishnan, D. Mensa, J. Guthrie, S. Jaganathan, T. Mathew, R. Girish, Y. Wei, and M. J. W. Rodwell, "Broadband lumped HBT amplifiers," *Electron. Lett.*, vol. 36, pp. 466–467, May, 2000.

[41] S. Yamahata, Y. Matsuoka, and T. Ishibashi, "Ultrahigh-speed AlGaAs/GaAs ballistic collection transistors using carbon as a p-type dopant," *Electron. Lett.*, vol. 29, pp. 1996–1997, Oct. 28, 1993.

[42] R. P. Smith, S. T. Allen, M. Reddy, S. C. Martin, J. Liu, R. E. Muller, and M. J. W. Rodwell, "0.1 μm Schottky-collector AlAs/GaAs resonant tunneling diodes," *IEEE Electron Device Lett.*, vol. 15, pp. 295–297, Aug. 1994.

[43] Q. Lee, B. Agarwal, R. Pullela, D. Mensa, J. Guthrie, L. Samoska, and M. Rodwell, "A $>$400 GHz $f_{\max}$ transferred-substrate heterojunction bipolar transistor IC technology," *IEEE Electron Device Lett.*, vol. 19, pp. 77–79, Feb. 1998.

[44] W. E. Stanchina *et al.*, "An InP-based HBT fab for high-speed digital, analog, mixed-signal, and optoelectronic ICs," in *Tech. Dig., GaAs IC Symp.*, 1995, pp. 31–34.

[45] Q. Lee, S. C. Martin, D. Mensa, R. P. Smith, J. Guthrie, S. Jaganathan, Y. Betser, T. Mathew, S. Krishnan, L. Samoska, and M. J. W. Rodwell, "Submicron transferred-substrate heterojunction bipolar transistors with greater than 1 THz $f_{\max}$," in *1999 IEEE Device Research Conf.*, Santa Barbara, CA, June.

[46] Q. Lee, S. C. Martin, D. Mensa, R. P. Smith, J. Guthrie, and M. J. W. Rodwell, "Submicron transferred-substrate heterojunction bipolar transistors," *IEEE Electron Device Lett.*, vol. 20, pp. 396–398, Aug. 1999.

[47] D. Mensa, Q. Lee, J. Guthrie, S. Jaganathan, and M. J. W. Rodwell, "Transferred-substrate HBTs with 250 GHz current-gain cutoff frequency," in *Proc. 1998 Int. Electron Device Meeting*, San Francisco, CA, Dec., 1998.

[48] S. J. Mason, "Power gain in feedback amplifier," *IRE Trans. Circuit Theory*, vol. CT-1, pp. 20–25, 1954.

[49] Y. Betser, D. Mensa, S. Jaganathan, T. Mathew, and M. Rodwell, "InAlAs/InGaAs HBTs with simultaneously high values of Ft and Fmax for mixed analog/digital applications," *IEEE Electron Device Lett.*, vol. 22, pp. 56–58, Feb. 2001.

[50] J. Guthrie, D. Mensa, T. Mathew, Q. Lee, S. Krishnan, S. Jaganathan, S. Cerhan, Y. Betser, and M. J. W. Rodwell, "A 50 mm copper/polymer substrate HBT technology for $>$100 GHz MIMICs," in *1999 IEEE Conf. InP and Related Materials*, Davos, Switzerland, May 1999.

[51] Q. Lee, D. Mensa, J. Guthrie, S. Jaganathan, T. Mathew, S. Krishnan, S. Cerhan, and M. J. W. Rodwell, "66 GHz static frequency divider in transferred-substrate HBT technology," in *1999 IEEE RF/Microwave Monolithic Circuits Symp.*, Anaheim, CA, June 1999.

[52] T. Mathew, H. J. Kim, S. Jaganathan, S. Krishnan, Y. Wei, M. Urteaga, S. Long, and M. J. W. Rodwell,, "75 GHz static frequency divider in InAlAs/InGaAs transferred-substrate HBT technology," in *2001 IEEE Conf. Indium Phosphide and Related Materials*, Nara, Japan, May 2001.

[53] B. Agarwal, R. Pullela, Q. Lee, D. Mensa, J. Guthrie, and M. J. W. Rodwell, "80 GHz distributed amplifiers with transferred-substrate heterojunction bipolar transistors," in *1998 IEEE Microwave Theory and Techniques Microwave Symp.*, Baltimore, MD, June 1998.

[54] B. Agarwal, Q. Lee, R. Pullela, D. Mensa, J. Guthrie, and M. J. W. Rodwell, "A transferred-substrate HBT wideband differential Amplifier to 50 GHz," *IEEE Microwave Guided Wave Lett.*, vol. 8, pp. 263–265, July 1998.

[55] D. Mensa, R. Pullela, Q. Lee, B. Agarwal, J. Guthrie, S. Jaganathan, and M. J. W. Rodwell, "Baseband amplifiers in the transferred-substrate HBT technology," in *1998 IEEE GaAs IC Symp.*, Atlanta, GA, Nov. 1–4.
[56] J. R. Guthrie, M. Urteaga, D. Scott, D. Mensa, T. Mathew, Q. Lee, S. Krishnan, S. Jaganathan, Y. Betser, and M. Rodwell, "MMIC 75 GHz power amplifiers," in *2000 IEEE Conf. Indium Phosphide and Related Materials*, Williamsburg, VA, May.
[57] S. Jaganathan, D. Mensa, T. Mathew, Y. Betser, S. Krishnan, Y. Wei, D. Scott, M. Urteaga, and M. Rodwell, "An 18 GHz clock rate continuous-time Δ–Σ modulator implemented in InP transferred-substrate HBT technology," in *2000 IEEE GaAs IC Symp.*, Seattle, WA, Nov..
[58] T. Mathew, S. Jaganathan, D. Scott, S. Krishnan, Y. Wei, M. Urteaga, M. J. W. Rodwell, and S. Long, "2 bit adder carry and sum logic circuits at 19 GHz clock frequency in Transferred Substrate HBT technology," in *2001 IEEE Conf. Indium Phoshide and Related Materials*, Nara, Japan, May 2001.

Mark J. W. Rodwell (M'89–SM'99) received the B.S. degree from University of Tennessee, Chattanooga, in 1980, the M.S. and Ph.D. degrees from Stanford University, Stanford, CA, in 1982 and 1988, respectively.

He is currently a Professor and the Director of the Compound Semiconductor Research Laboratories, University of California, Santa Barbara. He was with AT&T Bell Laboratories from 1982 to 1984. His research focuses on very high bandwidth bipolar transistors, high-speed bipolar IC design, and GHz mixed-signal ICs. His group has worked extensively in the area of GaAs Schottky-diode ICs for subpicosecond/mm-wave instrumentation.

Dr. Rodwell is the Recipient of a 1989 National Science Foundation Presidential Young Investigator award, and his work on submillimeter-wave diode ICs was awarded the 1997 IEEE Microwave Prize.

Miguel Urteaga received the B.A.Sc. degree in engineering physics from Simon Fraser University, Vancouver, BC, Canada, in 1998, and the M.S. degree in electrical engineering from the University of California, Santa Barbara (UCSB), in 2001, where he is currently pursuing the Ph.D. degree under the supervision of Prof. M. Rodwell.

His research work includes device design and fabrication of high speed InP HBTs, as well as the design of ultra high-frequency integrated circuits.

Thomas Mathew was born in Cochin, Kerala, India. He received the B.Tech degree from REC, Calcutta, India, in 1992, and the M.Tech degree from the Indian Institute of Technology (IIT), Bombay, India, in 1996. He is currently pursuing the Ph.D. degree at the University of California, Santa Barbara.

He is currently involved in digital circuit design, HBT-based circuit fabrication, and high-speed circuit measurement techniques.

Dennis Scott received the B.S. and M.S. degrees in electrical engineering from the University of Illinois, Urbana, in 1996 and 1999, respectively. He is currently pursuing the Ph.D. degree at the University of California, Santa Barbara, working on high-speed HBTs.

Dino Mensa received the B.S. degree in physics and the M.S. and PhD degrees in electrical engineering, all from University of California, Santa Barbara (UCSB), in 1995, 1997, and 1999, respectively.

His research at UCSB focused on MBE growth, high-speed device design, and high-frequency amplifier design in the transferred-substrate InP HBT process. From 1999 to 2000, he worked as a fiber-optic IC Design Engineer at Conexant Systems, Inc. He is currently a Senior Engineer, Gtran Inc., Thousand Aaks, CA. His current research interests include circuit design for high speed fiber-optic systems.

Q. Lee was born in Beijing, China. She received the B.S. degree in physics from Sichuan University, Chengdu, China, in 1986, the M.S. degree in physics from Lehigh University, Bethlehem, PA, in 1995, and the Ph.D. degree in electrical engineering from the University of California, Santa Barbara, in 1999.

From 1999 to 2000, she was Member of Technical Staff with Bell Laboratories, Lucent Technologies, Murray Hill, NJ, designing high-speed circuits for fiber optic communications. She is currently a Senior Design Engineer at Big Bear Networks, Milpitas, CA.

James Guthrie received the B.Ap.Sc. degree in engineering science and the M.S. in electrical engineering, both from the University of Toronto, Toronto, ON, Canada, in 1992 and 1994, respectively, and the Ph.D. degree in electrical engineering from the University of California, Santa Barbara (UCSB), in 2000.

He joined the HBT process development group, Nortel Networks, Ottawa, ON, Canada, in 2000. His research interests are in high speed electronics.

Y. Betser, photograph and biography not available at the time of publication.

Suzanne C. Martin received the B.S. and M.S. degrees in electrical engineering from Brown University, Providence, RI, in 1985 and 1991, respectively.

From 1985 to 1989, she was a Research Engineer at Brown University, designing and fabricating germanium photodiodes and MOSFETs. She is currently a member of the Engineering Staff at the Jet Propulsion Laboratory, Pasadena, CA, and is involved in the fabrication of mixer and varactor diodes for submillimeter wave applications along with e-beam process development for other devices including HEMTs, HBTs, and GaN FETs.

R. P. Smith, photograph and biography not available at the time of publication.

S. Jaganathan received the B.Tech. degree in electrical engineering from Indian Institute of Technology, Bombay, India, in 1993, and the M.S. and Ph.D. degrees in electrical engineering from the University of California, Santa Barbara, in 1997 and 2000, respectively.

His research at UCSB focused on design of high-speed sigma–delta ADCs using InGaAs/InP HBTs. He is currently a Senior Engineer with Gtran Inc., Newbury Park, CA. His current research interests include circuit design for high-speed fiber-optic systems.

Sundararajan Krishnan received the B.Tech degree in electrical engineering from the Indian Institute of Technology, Madras, India, in 1998. Since then, he has been with Prof. Rodwell's group at the University of California, Santa Barbara, where he is involved in the design of high-speed mixed-signal circuits.

Stephen I. Long received the B.S. degree in engineering physics from the University of California, Berkeley, in 1967, and the M.S. and Ph.D. degrees in electrical engineering from Cornell University, Ithaca, NY, in 1969 and 1974.

From 1974 to 1977, he was a Senior Engineer and Manager of Semiconductor Engineering, Varian Associates, Palo Alto, CA. From 1978 to 1981, he was a Member of the Technical Staff, Rockwell International Science Center, Thousand Oaks, CA. In 1981, he joined the Electrical and Computer Engineering Department, University of California, Santa Barbara, where he is currently a Professor. His research interests include the design of low power, high-speed digital and analog circuits, high-performance devices and fabrication technologies, and microwave analog integrated circuits for personal communications. In 1988, he was a Research Visitor at GEC Hirst Research Centre, U.K. In 1994, he was the Fulbright Research Visitor at the Signal Processing Laboratory, Tampere University of Technology, Tampere, Finland, and a Visiting Professor at the Electromagnetics Institute, Technical University of Denmark, in 1999, he was a Visitor at Hewlett-Packard HP/EEsof Division, Santa Rosa, CA.

Dr. Long received the IEEE Microwave Applications Award in 1978 for development of InP millimeter wave devices.

R. Pullela received the B. Tech. degree in electronics and communication engineering from the Indian Institute of Technology, Madras, India, in 1993, and the M.S. and Ph.D. degrees in electrical engineering from the University of California, Santa Barbara, in 1995 and 1998, respectively.

From June 1998 to May 2000, he was a Member of Technical Staff, Bell Laboratories, Lucent Technologies, Murray Hill, NJ. Since May 2000, he has been a Senior Engineer with Gtran, Inc., Thousand Oaks, CA. His current interests include high-speed fiber optic transceivers and indium phosphide HBT technology design.

Bipul Agarwal (S'97–M'99) was born in Cuttack, India, in 1970. He received the B.Tech. in electronics and communications engineering and the M.S. and Ph.D. degrees from the Indian Institute of Technology (IIT), Madras, in 1992, 1995, and 1998, respectively.

From 1992 to 1993, he was a Research Assistant with IIT. He joined the Electrical Engineering Department, University of California, Santa Barbara, as a Graduate Student Researcher in the Fall of 1993. His dissertation was on ultrafast "transferred-substrate" InP HBTs and high-speed analog integrated circuits for fiber-optic communication. He is currently with the RFIC Design Group, Conexant Systems, Newport Beach, CA. His work involves design of RF circuits for wireless applications.

Uddalak Bhattacharya received the B.Tech degree in electronics and electrical communication engineering from the Indian Institute of Technology, Kharagpur, India, in 1991, and the M.S. and Ph.D. degrees in electrical engineering from the University of California, Santa Barbara, in 1993 and 1996, respectively.

Since then, he has been a Senior Design Engineer, Technology Development Division, Intel Corporation, Portland, OR. His interests are in high-speed digital circuit design, test, measurement, and yield analysis.

Lorene Samoska received the B.S. degree in engineering physics from the University of Illinois, Urbana, in 1989, and the Ph.D. degree in materials engineering from the University of California, Santa Barbara, in 1995.

She was an Associate Research Engineer with the Electrical and Computer Engineering Department, University of California, Santa Barbara, where she was engaged in the design and fabrication of state-of-the-art microwave digital circuits based on InP heterojunction bipolar transistors (HBTs). In 1998, she joined the Jet Propulsion Laboratory, Pasadena, CA, where she is currently a Member of the Engineering Staff of the Submillimeter-Wave Advanced Technology (SWAT) Team. Her current interests include the design of 70–200 GHz HEMT power amplifiers for providing local oscillator sources to space missions.

Mattias Dahlstrom is currently pursuing the Ph.D. degree at the Laboratory of Photonics, KTH, Kista, Sweden, where he has been working on monolithic integration of InP-based optoelectronic devices. He is currently working the University of California, Santa Barbara, on fast InP-based HBTs