87 GHz Static Frequency Divider in an InP-based Mesa DHBT Technology

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Abstract

We report a static frequency divider with a maximum clock frequency of 87 GHz in a mesa InP/InGaAs/InP DHBT Technology. The divider is operational at all tested frequencies between 4 and 87 GHz and dissipated 700 mW of power from a –4.5V supply.

Keywords

Static Frequency Dividers, HBT

INTRODUCTION

Fully static frequency dividers are typically used as benchmarks to evaluate the speed of a digital technology. The performance of such a circuit is a recognized figure of merit because it uses the same basic flip-flop elements found in more complex sequential circuits—these include retiming latches and selectors in fiber optic integrated circuits. Impressive results, measured by the maximum clock frequency of the divider, have been demonstrated in SiGe [1] and InAlAs/InGaAs HBT technologies. Sokolich et al have reported a 72.8 GHz maximum clock frequency in an InAlAs/InGaAs mesa SHBT process [2], while we have previously reported a 75 GHz clock rate static frequency divider in an InAlAs/InGaAs transferred-substrate SHBT technology [3]. We report here a static frequency divider with a maximum clock frequency of 87 GHz, fabricated in a more manufacturable InP/InGaAs/InP DHBT technology

TECHNOLOGY

The reported circuit uses an MBE epitaxial layer structure with a 400 Å graded $In_{0.53}GaAs$ highly doped base layer (Be: $4.0 \cdot 10^{19} cm^{-3}$), a 100 Å InGaAs setback layer, a 240 Å CSL base-collector grade and a 1630 Å InP collector layer, resulting in a total collector depletion layer thickness of 2kÅ. The circuit devices are fabricated in a triple-mesa process with both active junctions defined by selective wet-etch chemistry [4]. The active junctions are then passivated by polyimide. The polyimide is planarized and patterned using a dry etch to expose the electrical contacts to the three terminals of the transistor. Following this, thin-film NiCr resistors are deposited with a sheet resistance of 40 Ω/square. The ensuing level of metal deposition is used for circuit interconnects—making electrical contacts to the transistors and resistors. A 4000 Å thick SiN layer is then deposited and acts as the dielectric for the MIM capacitors.

To realize complex mixed-signal ICs, a wiring environment that maintains control of signal integrity and has predictable characteristics to enable robust computer-aided design (CAD) is required. Thin-film-dielectric microstrip-wiring provides controlled-impedance interconnects within dense mixed-signal ICs. The associated ground plane also eliminates signal coupling through on-wafer ground-return inductance.

Such a wiring environment is added to this process using a dielectric layer and ground-plane above the IC top-surface. We implement this by spin-casting a 5-μm thick benzocyclobutene (BCB) polymer film onto the wafer, vias through BCB are etched where required, and the top ground-plane is then formed by electroplating. A cross-sectional view of this wiring environment is shown in Fig. 1. In such a wiring environment, 8-μm and 3-μm width conductors have controlled 50Ω and 80Ω microstrip impedances respectively. Since the dielectric is thin, ground-vias can be closely packed—a necessity for complex IC's, and the ground-via-inductance is quite small. In addition, interconnects are not significantly coupled for line spacing greater than 10 μm.

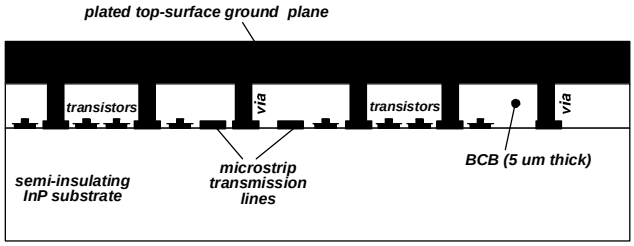

Fig. 1: Cross-sectional view of the microstrip-wiring environment

Disadvantages of using thin dielectric microstrip wiring include the increased skin-loss compared to a conventional microstrip environment of similar impedance, and the charging time associated with unterminated nodes in a circuit are increased due to the increased capacitance per unit length of interconnect.

RF measurements were done on devices with 0.7 X 8 μm^2 emitter and 1.7 X 12 μm^2 collector mask dimensions. The f_τ and f_{max} were found to be 205 and 210 GHz respectively at a current density $J_c = 2.5. 10^5$ A/cm^2 and at a bias voltage $V_{ce} = 1.2$ V.

CIRCUIT DESIGN

The circuit schematic of the master-slave flip-flop is shown in Fig. 2 and is similar to the static divider reported in [3]. The output of the master-slave flip-flop drives a simple ECL differential-pair that serves as an output buffer. The output buffer drives a 50 Ω load. To minimize the number of active devices, we do not use a current-mirror based biasing scheme. Instead, the bias currents are established using pull-down resistors. The current-switching pair and the emitter-followers are designed to operate at current densities of 2.5 mA/μm^2 and 2 mA/μm^2, respectively.

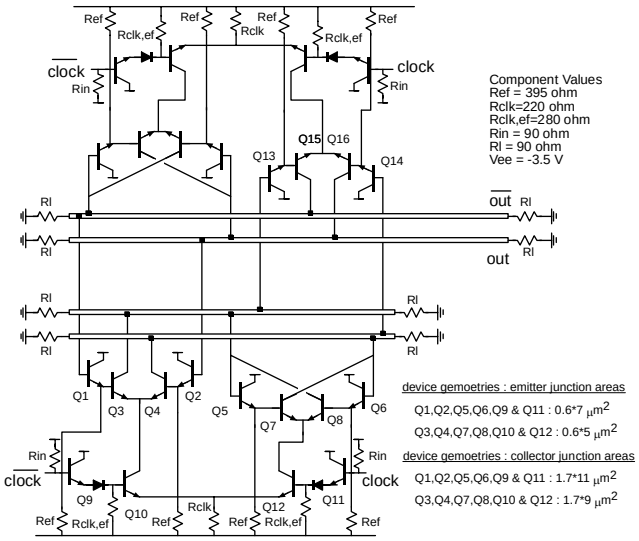

Fig. 2: Circuit schematic of the static frequency divider

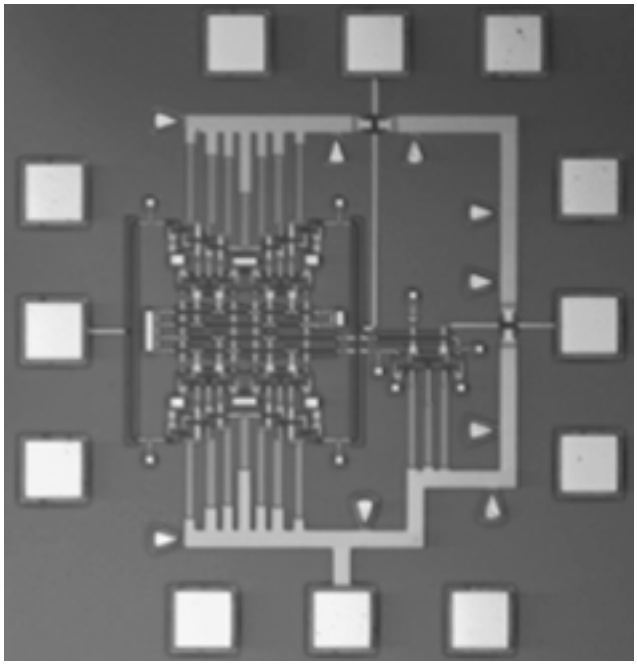

Fig. 3: IC Micrograph of the static frequency divider

To minimize the interconnect delays, the switching signal path is a short, doubly-terminated in a 90 Ω transmission-line bus, located at the center of the IC. The IC micrograph of the divider is shown in Fig. 3. The die-area is 0.7 X 0.7 mm^2 and contains 28 transistors.

MEASUREMENTS AND RESULTS

We performed divider measurements for clock frequencies ranging from 4 to 87 GHz. At low frequencies, a 10 MHz-40 GHz frequency synthesizer output directly drives the clock input. A low frequency measurement was performed to establish the fully static nature of the divider and is shown in Fig. 4. An input clock driver is not employed in this circuit. For this reason, and considering that we used a sine-wave generator, a dependence of the output waveform on the slew-rate of the incoming clock signal is observed.

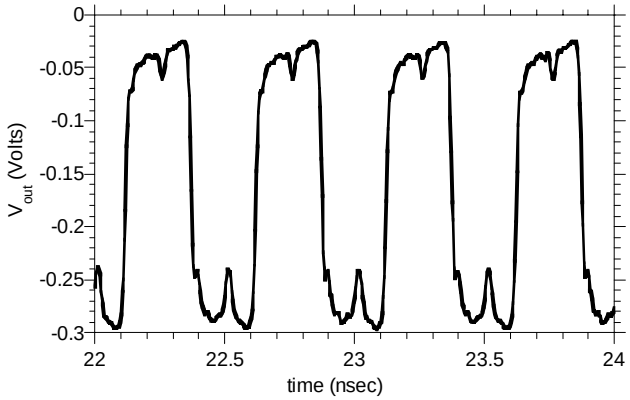

Fig. 4: Output Voltage @ 2 GHz; f_{clk} = 4 GHz
This measurement establishes that the divider is fully static.

For 50-75 GHz (V-band) measurements, the 10 MHz-40 GHz synthesizer drives a frequency tripler (with output frequency range of 50 to 75 GHz) whose output is delivered on-wafer with a V-band waveguide-couple micro-coaxial probe. Fig. 5 shows the output waveform for a clock input of 75 GHz.

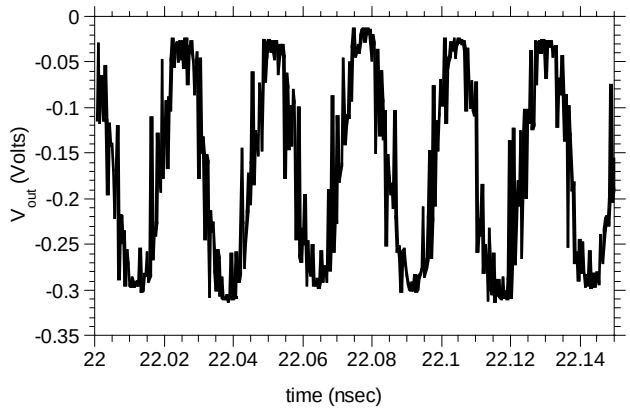

Fig. 5: Output Voltage @ 37.5 GHz; f_{clk} = 75 GHz

For 75-87 GHz (W-band) measurements, the synthesizer drives a 20-40 GHz amplifier, whose output drives a frequency tripler (with output frequency range of 75 to 110 GHz). This output signal is then amplified and delivered through a waveguide-coupled W-band wafer probe. The output waveform for a clock input of 87 GHz is shown in Fig. 6, and drive power at the clock input (probe tip) was measured to be 9.7 dBm at this frequency.

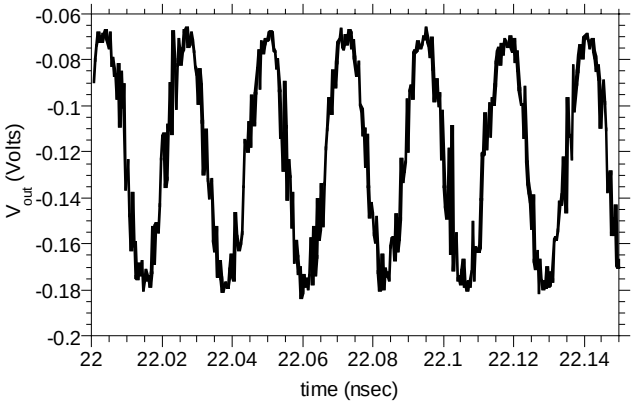

Fig. 6: Output waveform @ 43.5 GHz; f_{clk} = 87 GHz

ACKNOWLEDGEMENTS

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