Multi-stage G-band (140-220 GHz) InP HBT Amplifiers

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***Abstract* — We report three-stage monolithic amplifiers for the 140-220 GHz frequency band. Two designs have been fabricated in an InAlAs/InGaAs transferred-substrate HBT technology. The first design exhibited a small-signal gain of 12.0 dB at 170 GHz, and the second design exhibited a gain of 8.5 dB at 195 GHz.**

I. INTRODUCTION

Electronics in the 140-220 GHz frequency band have applications in wideband communication systems, remote atmospheric sensing, and planetary exploration. Extending transistor bandwidths to provide high available gain in this frequency range requires submicron scaling of lateral device dimensions. The gate lengths of InP-based high electron mobility transistors (HEMTs) have been scaled to deep submicron dimensions, and high gain G-band amplifiers have been reported in technologies utilizing these devices [1,2,3]. In [4], we reported a single-stage amplifier fabricated in a transferred-substrate HBT technology that exhibited 6.3 dB gain at 175 GHz. Here, we report multi-stage amplifier designs developed in the same technology.

II. TRANSFERRED-SUBSTRATE HBT TECHNOLOGY

The standard geometry of a III-V mesa-HBT frustrates efforts to simultaneously scale the emitter-base and collector-base junction areas [5]. Utilizing a substrate transfer process, we are able to lithographically pattern both sides of the device epitaxy and simultaneously scale the emitter-base and collector-base junction widths to submicron dimensions. The dramatic reduction in base-collector capacitance provided by this processing technique has yielded transistors with record values of measured power gains at W-band frequencies [6].

A. Epitaxial Growth and Fabrication

A brief overview of the transferred-substrate process and device layer structure is presented here. A more detailed review of the technology can be found in [5].

The HBT layer structure has a single InAlAs/InGaAs heterojunction and is grown by molecular beam epitaxy on a semi-insulating InP substrate. The 400 Å base layer is p+ Be-doped at 5×10^{19} cm^{-3}, and includes approximately 50 meV of compositional grading to reduce base transit time. In this work, the InGaAs collector was 3000 Å thick.

Prior to substrate transfer, the HBT fabrication process is similar to that of a traditional mesa-HBT. Technology features include: self-aligned base contacts, polyimide device passivation, two levels of metal interconnects, MIM capacitors, and NiCr resistors.

After the definition of the final interconnect layer, a spin-on-polymer, benzocyclobutene (ε_r=2.7), is spun onto the wafer and serves as the microstrip transmission line dielectric. Vias are dry-etched in the BCB, and the BCB is simultaneously etched back to a final thickness of 5 µm. A gold ground plane is electroplated on the BCB surface. The InP wafer is then mechanically bonded to a GaAs carrier wafer with the ground plane at the GaAs wafer surface. A selective HCl etch removes the InP substrate revealing the collector epitaxy. Schottky collector contacts can then be defined directly over the devices. In this work, electron-beam lithography was used to define emitter and collector stripes. A cross-section of the transferred-substrate technology is shown in Fig. 1.

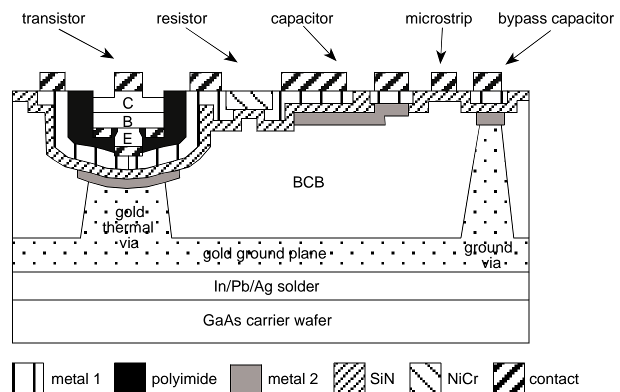

Fig. 1. Schematic cross-section of transferred-substrate HBT process.

B. Device Results

The transistor used in the amplifier design had an emitter-base junction area of 0.4 µm x 6 µm, and a collector stripe of 0.7 µm x 6.4 µm. Devices of that geometry have typical DC small signal current gains, β, of

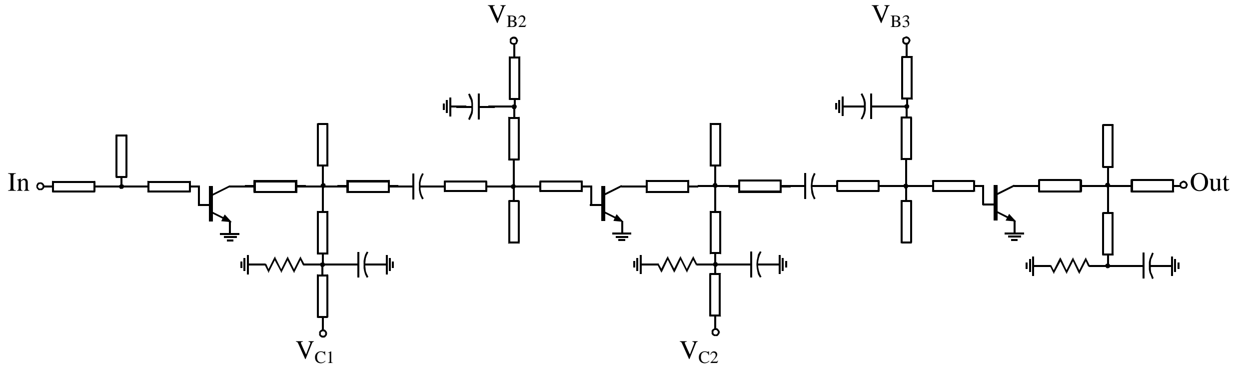

Fig. 3. Circuit schematic of multi-stage amplifier design.

20, and common-emitter breakdown voltages, BV_{CEO}, of 1.5 V at a current density of 10^5 A/cm^2.

Fig. 2 shows the maximum stable gain (MSG) and the short circuit current gain (h_{21}) for a transistor measured from 10-45 GHz, 75-110 GHz and 140-220 GHz. The device was biased at I_c = 3.2 mA, and V_{ce} = 1.25 V. The bias conditions are identical to those used in the measured amplifiers.

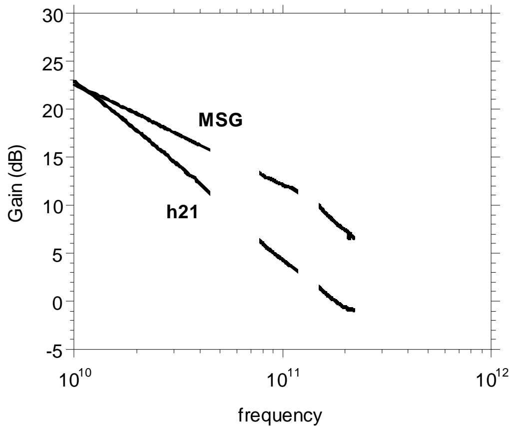

Fig. 2. HBT current gain (H21), maximum stable power gain (MSG) and unilateral power gain (U), measured in the DC-45 GHz and 140-220 GHz bands.

We note that the Rollet stability factor (*k*) is less than unity to 220 GHz and that the power gain in the 140-220 GHz band still represents the maximum stable gain of the device, and not the maximum available gain. The current gain cutoff frequency f_τ of the device was measured to be 180 GHz. Mason's unilateral power gain (U) is generally used to extrapolate the maximum power gain cutoff frequency (f_{max}) of a transistor. For an HBT well modeled by a hybrid-pi transistor model, U will exhibit a 20-dB/decade rolloff independent of transistor configuration and the reactances associated with the on-wafer embedding network.

We have observed that highly scaled InGaAs collector HBTs may exhibit a phase shift in the reverse transmission characteristics (Y12) that cannot be modeled by a hybrid-pi transistor model. Such transistors exhibit a peaking in the unilateral power gain, and under certain bias conditions, U may exhibit a singularity where it increases and becomes negative. It is believed that these effects are the result of second-order transport phenomenon in the collector space charge region. These effects would not be observed in a standard III-V mesa-HBT because the reverse transmission characteristics are dominated by the large extrinsic base-collector capacitance. A more detailed presentation of these results will be reported at a later date.

A consequence of the observation of a singularity in the unilateral power gain is that we cannot extrapolate f_{max} from transistor power gain measurements. However, our previously reported result of a single-stage amplifier with 6.3 dB gain at 175 GHz verifies the high available gain from these devices at the frequency limits of currently available VNA systems [4].

III. Amplifier Design

A circuit schematic of the multi-stage amplifier design is shown in Fig. 3. The design consists of three cascaded common-emitter stages. The input and output of each stage are matched to a 50Ω characteristic impedance using transmission line shunt-stub tuning. Inter-stage MIM capacitors, with nominal values of 75 fF, provide DC isolation between stages. Separate supply lines provide DC bias to the base and collector of each device. DC bias to the base of the first stage and collector of the final stage are provided through bias Tees in the high frequency on-wafer probes. A shunt resistor at the collector of each device is used to ensure low frequency stability, and a high

impedance quarter-wave line to a MIM capacitor bypasses the resistor at the intended design frequency. At the amplifier design frequencies, resistive losses in the transmission line matching networks are sufficient to stabilize the transistors. A chip photograph of a fabricated amplifier is shown in Fig. 4.

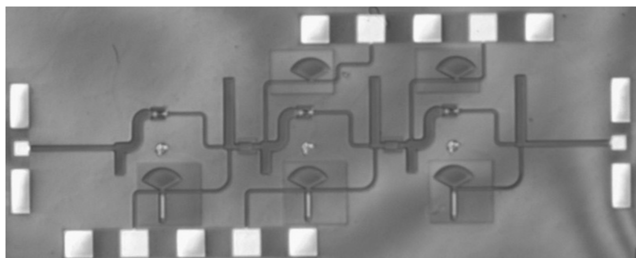

Fig. 4. Chip photograph of fabricated amplifier. Cell dimensions are 1.66 x 0.59 mm^2.

Two amplifier designs were fabricated with intended design frequencies of 175 GHz and 200 GHz. The designs were developed using measured S-parameters of transistors with identical geometries and layer structures from a previous process run [4].

The circuits were designed using Agilent Technologies Advanced Design System software [7]. A planar method-of-moments EM simulator (Momentum) was used to model the microstrip discontinuities (i.e. junctions and bends) in the circuit. Standard microstrip CAD models were used to model the remaining transmission lines in the circuit. Excellent agreement has been seen between measurement and simulation of passive structures using this design approach [4].

Simulations of the two amplifier designs predicted a peak gain of 20 dB for the 175 GHz design and a peak gain of 14.5 dB for the 200 GHz design.

IV. RESULTS

The amplifiers were measured on-wafer from 140-220 GHz. The measurements were made using an HP8510C Vector Network Analyzer (VNA) with Oleson Microwave Labs Millimeter Wave VNA Extensions. The test set extensions are connected to GGB Industries coplanar wafer probes via a short length of WR-5 waveguide. The device and amplifier measurements were calibrated on-wafer using Thru-Reflect-Line calibration standards.

Fig. 5 shows the measured gain, and input and output return loss of the 175 GHz amplifier design. Fig. 6 shows the same parameters measured for the 200 GHz amplifier design. For both amplifier designs, the transistors in the circuit were biased at $I_c = 3.2$ mA, and $V_{ce} = 1.25$ V.

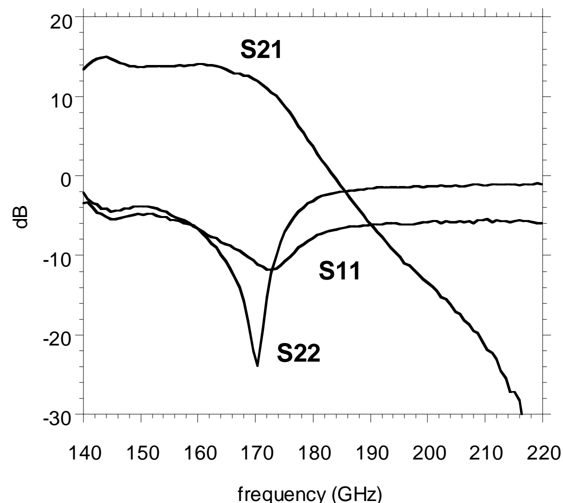

Fig. 5. Measured S-parameters of 175 GHz three-stage amplifier.

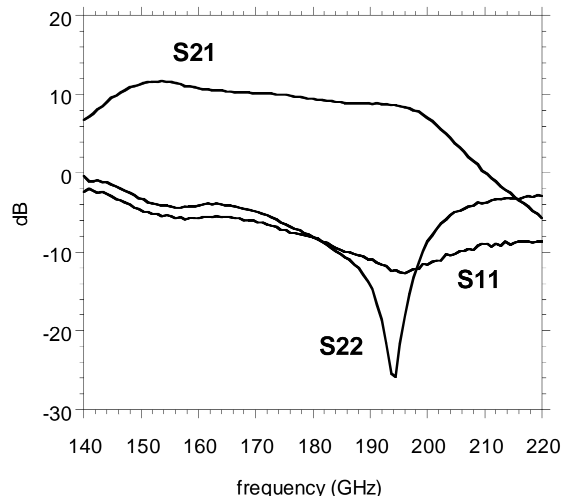

Fig. 6. Measured S-parameters of 200 GHz three-stage amplifier.

The 175 GHz amplifier design had a gain of 12.0 dB at the output match frequency of 170 GHz. A peak gain of 15.0 dB was measured at 144 GHz, and the gain was greater than 10 dB to 175 GHz. The 200 GHz amplifier design exhibited a gain of 8.5 dB at the output match frequency of 195 GHz. A peak gain of 11.7 dB was measured at 154 GHz and the gain was greater than 7.0 dB to 200 GHz.

Both amplifier designs exhibited a downward shift of ~5 GHz from their intended design frequency. The peak gains of the designs were also less than predicted from simulations. The amplifier designs were based on measured device S-parameters from a previous process run. Transistor measurements from the multi-stage

amplifier process run show higher extrinsic emitter resistance, and lower available power gain than the transistors used in the design cycle.

Fig 7. shows a circuit simulation of the 175 GHz multi-stage amplifier using measured transistor S-parameters from the amplifier process run. The close agreement with measured amplifier results indicates that device variation is responsible for the downward shift from the design frequency and verifies the amplifier matching network design.

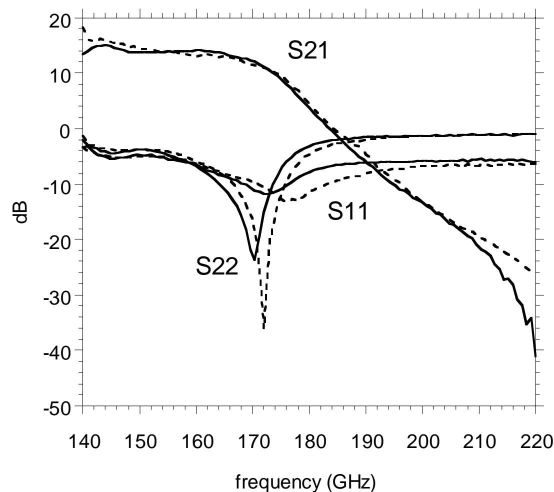

Fig. 7. S-parameters of measured 175 GHz amplifier (solid lines) and circuit simulation of amplifier using measured transistor S-parameters (dashes)

V. Conclusions

We have presented multi-stage tuned amplifier designs in a transferred-substrate HBT technology. Two designs were fabricated with gains of 12.0 dB and 8.5 dB at 170 GHz and 195 GHz, respectively. The circuits demonstrate the potential for highly scaled low-parasitic HBT technologies to compete with HEMTs in G-band millimeter-wave circuit applications.

Acknowledgement

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