InAlAs/InGaAs/InP DHBTs with Polycrystalline InAs Extrinsic Emitter Regrowth

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We report dc transistor performance in InAlAs/InGaAs/InP double heterojunction bipolar transistors (DHBT) utilizing molecular beam epitaxy (MBE) regrown base-emitter junctions. We believe this to be the first report of an HBT utilizing non-selective-area regrowth in the formation of an active heterojuction. The process produces a very low-resistivity polycrystalline InAs extrinsic emitter, with a very low-resistivity emitter contact whose area is much larger than that of the base-emitter junction, facilitating low emitter resistance. The process also eliminates the need to form the base-emitter junction by etching and self-aligned metal liftoff, as we have found such processes have very low yield at deep submicron dimensions. This work is the first step in an attempt to parallel the highly scaled, high integration, low parasitic, and high-yield aspects of silicon transistors.

The advantages of III-V HBTs over Si/SiGe include higher electron velocities and stronger heterojuctions. The primary disadvantage is the immaturity of its processing technology relative to its silicon counterpart. Despite the superior material properties of III-V HBTs, Si/SiGe HBTs remain highly competitive. The best reported InP-based HBTs include 341 GHz f_τ and 425 GHz f_{max} [1,2]. Si/SiGe HBTs have obtained a published f_τ as high as 210 GHz [3] using emitter dimensions as small as 0.22×0.8 μm^2. The high bandwidth arises from aggressive scaling and parasitic reduction. The low-resistance polysilicon emitter contact used in SiGe is much wider than the active emitter junction allowing the emitter resistance to remain low while shrinking the active junction area. Emitter regrowth in Si/SiGe HBTs allows for deep submicron emitter widths while maintaining high yield. Conventional III-V mesa HBTs would suffer from emitter contact resistance if the emitter metal were scaled to comparable dimensions. The difficulty of reliably producing deep submicron base-emitter junctions by etching in III-V HBTs also suggests low yield.

This work suggests a restructuring of the III-V HBT fabrication process to closely follow the Si/SiGe HBT. As a first step in paralleling the Si/SiGe process, we have used MBE to non-selectively grow an InAlAs emitter and InAs cap onto a patterned base-collector template. The base-collector template was grown by MBE on a 2-inch InP substrate. The template consists of a 2500Å InGaAs n+ subcollector, 1200Å n- InP collector, 300Å n- grade and undoped setback, 400Å p+ InGaAs base, 80Å InP p+ etch stop, and 520Å p+ InGaAs cap. Silicon is the n-type dopant. Carbon is the p-type dopant for the InGaAs, and beryllium is used for the InP. After growth, the template was covered with SiN_x and the emitter regrowth areas were defined by optical lithography with dimensions as small as 1×15 μm^2. The SiN_x was removed from the emitter areas by dry etching, and the underlying InGaAs base cap was removed using selective citric etchant. SiN_x sidewalls were formed, and the 80Å InP etch stop layer was removed just prior to regrowth. A schematic of the template cross-section is shown in Figure 1. MBE was then used to grow a 200Å InGaAs/InAlAs n- grade, 600Å InAlAs n- emitter, 500Å InAlAs n+ emitter, and 1000Å heavily doped InAs. Regrowth of the emitter material in the semiconductor areas is intended to be crystalline. Regrowth on the SiN_x is expected to be polycrystalline. After the regrowth, large-area contacts were etched from the cap and emitter stopping on the SiN_x. The SiN_x not protected by remaining regrowth was then removed to expose the base cap. The base stack and collector were selectively wet etched down to the subcollector, and the metal layer was patterned. Ti/Pt/Au was then simultaneously deposited on the emitter, base, and subcollector. The process is detailed in Figure 2. The result is a large-area transistor with small emitter dimensions as shown in Figure 3. A cross-section of the base-emitter junction is shown in Figure 4.

The dc characteristics of the HBT with a regrown emitter area of 0.8×15 μm^2 are shown in Figure 5. Figure 5(a) shows the common-emitter characteristics. The common-emitter current gain β is over 15, and the collector-emitter breakdown voltage BV_{CEO} is soft and above 3.5V. The offset voltage is about 0.25V. The prominent dip in the collector current is attributed to a growth error in the base-emitter grade. A 50Å InAlAs layer was unintentionally grown directly on the InGaAs base before the grade. This wide-bandgap layer in the device acts as a current blocking element. It is suspected to contribute to the low β and accounts for the large dip in the common-emitter curves. Figure 5(b) shows a Gummel plot with a base-collector bias voltage V_{BC} of 0V. Note the low base leakage current at low V_{BE}. Hall measurements were used to determine the doping and mobility of the silicon-doped InAs grown on SiN_x. The doping is 1.3×10^{19} cm^{-3} with a mobility of 290 cm^2/V·s. These numbers suggest a very low-resistance polycrystalline contact layer. TLM data from the polycrystalline regrowth on SiN_x shows a sheet resistance of 158 Ω/sq and a contact resistance of 0.5 Ω-μm^2.

[1] M. Ida, K. Kurishima, H. Nakajima, N. Watanabe, T. Enoki, Tech Dig. 2001 IEEE IEDM, p. 35.4.

[2] S. Lee, H.J. Kim, M. Urteaga, S. Krishnan, Y. Wei, M. Dahlstrom and M. Rodwell, Tech. Dig. 2001 GaAs IC Symp., p. 185.

[3] S.J. Jeng, B. Jagannathan, J.-S. Rieh, *et al.*, IEEE EDL, vol. 22, no. 11, pp. 542-544, 2001.

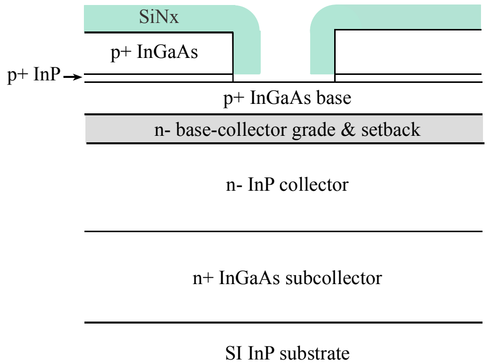

Figure 1. Base-collector template prior to regrowth.

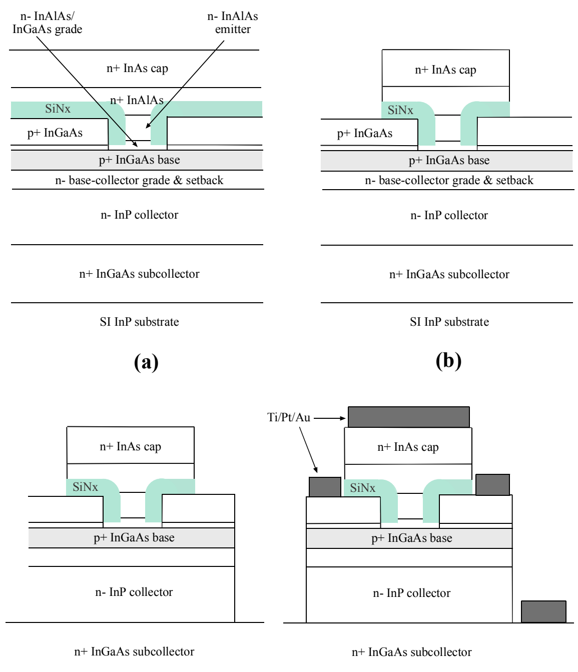

Figure 2. Process flow to fabricate large-area HBT.

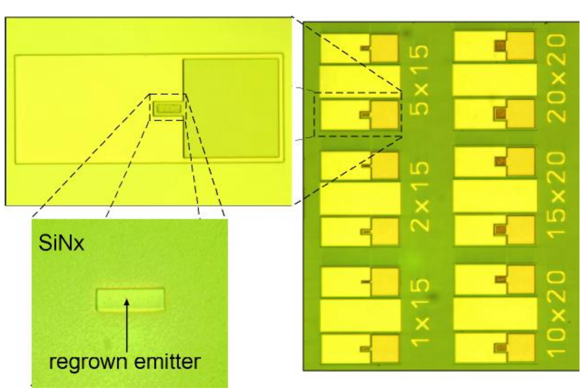

Figure 3. Large-area, small-emitter HBT.

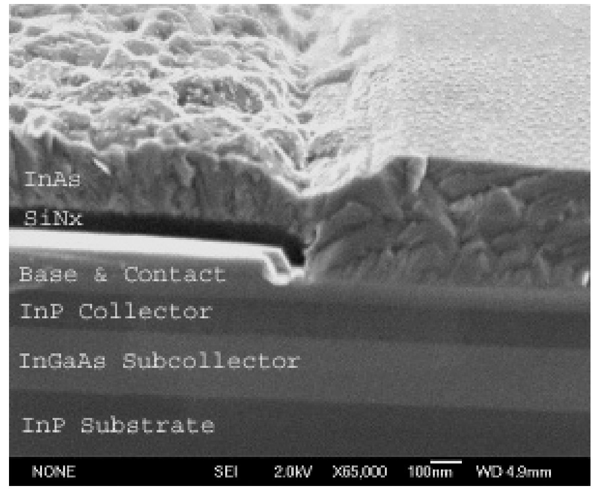

Figure 4. SEM cross-section of the regrown emitter HBT showing the polycrystalline regrowth (left) and the regrowth on crystalline material (right).

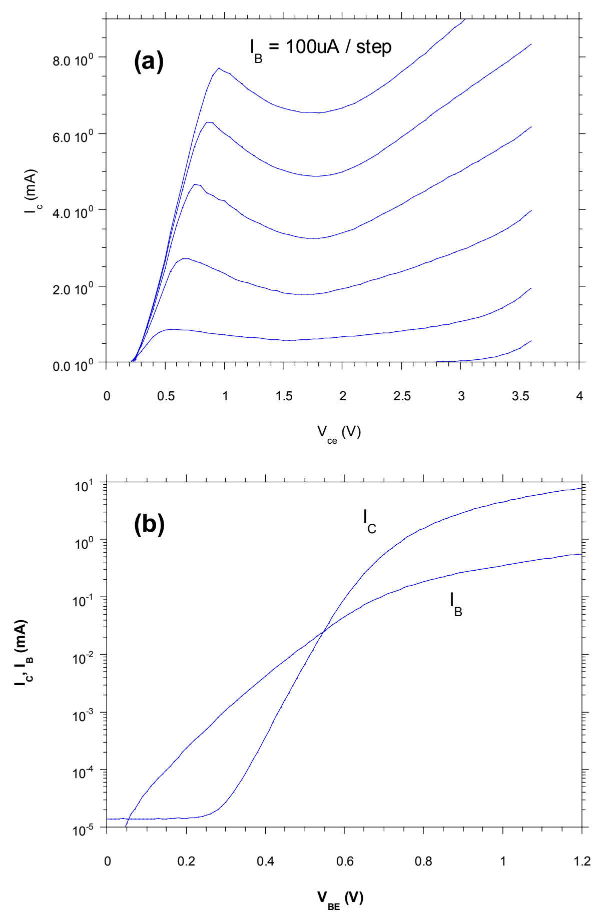

Figure 5. DC device characteristics for $0.8 \times 15\ \mu m^2$ regrown emitter HBT.