50-200 GHz InP HBT Integrated Circuits for Optical Fiber and mm-Wave Communications

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***Abstract**: We report the InP HBT scaling strategies required for 80-160 Gb/s optical fiber ICs, and a variety of recent HBT results, including 87 GHz static frequency dividers, 175 GHz amplifiers, and >450 GHz $f_{\max}$ DHBTs.*

Despite recent economic conditions, there remains rapid growth in the communications infrastructure, both in optical fiber transmission, and in wireless local-area and metropolitan area networks. In optical fiber communication, 10 Gb/s systems are now a large commercial market, with the supporting ICs quickly transitioning from III-V through SiGe to 0.13 μm CMOS. 40 Gb/s systems are one to two years from commercial release. Here the dominant contending IC technologies are InP and SiGe heterojunction bipolar transistors (HBTs). Several laboratories worldwide are investigating device technologies and IC designs for 80-160 Gb/s, with efforts focusing on InP HEMT and InP HBT integrated circuits. Most wireless applications are very cost-sensitive and hence predominantly operate in the low GHz range, where ICs are inexpensive. Nevertheless, high-frequency metropolitan area networks are being explored in the 60 GHz band, where there is sufficient bandwidth to support Gb/s transmission rates. At higher mm-wave frequencies, 100-220 GHz, there are large available bandwidths available over which (weather permitting) the atmospheric losses are low. Given the availability of 200 GHz ICs, wireless networks of 1-10 Gb/s capacity will be feasible. Through submicron scaling, InP HBT ICs will be able to serve both 160 Gb/s optical fiber transmission and 200 GHz wireless networks.

Transistor bandwidths are increased through either scaling or through improved semiconductor transport characteristics. Historically, gains in SiGe HBT and CMOS performance were obtained through aggressive scaling, while III-V (GaAs and InP) devices have relied upon superior electron transport and employ large (1-2 μm) device dimensions. For 50-200 GHz operation, III-V HBTs must also be scaled to submicron dimensions. Additionally, transistor development must be guided by IC performance, rather than by the figures of merit of current-gain (f_τ) and power gain ($f_{\max}$) cutoff frequencies. Critical factors for optical fiber ICs and logic are low emitter access resistance, moderately low base resistance, and very high ratio of current to depletion-layer capacitances. Compared to InP, Si/SiGe HBTs employ smaller junctions, operate at higher current densities, and have lower emitter resistance.

We have developed scaling laws which describe the adjustments in HBT parameters required for a balanced and proportional improvement in device bandwidth in an arbitrary circuit [1,2]. For each 2:1 improvement in bandwidth, the collector layer must be thinned 2:1, the base thinned $\sqrt{2}$:1, the operating current density increased 4:1, and the emitter resistance per unit area reduced 4:1. Emitter and collector junction widths must both decrease 4:1. If the base contacts lie above the active collector-base junction, the contact width and the contact resistivity must both also decrease 4:1; in device structures where the contacts do not lie above the collector-base junction, the contact width and contact resistivity can remain unscaled. Scaling rates can be relaxed with appropriate material or process improvements: emitter current density can be proportionally reduced if the ratio of collector to emitter junction areas is reduced, while emitter and collector junction widths can be increased if the base contact resistivity is greatly reduced. Based upon these scaling laws, Table 1 summarizes the key device parameters required for operation of InP HBT ICs at 40, 80, and 160 Gb/s rates, as determined by computing1 the maximum operating frequency of a master-slave latch, the key digital building block in the MUX, decision, DMUX, and PLL.

HBTs are more readily scaled for mm-wave amplification, as the use of inductive tuning networks allows circuit operation to $f_{\max}$, even in the presence of relatively low f_τ and moderate depletion capacitance charging times. High $f_{\max}$ can be obtained by lateral scaling, while maintaining relatively thick semiconductor layers and moderate current density. For these applications we have developed transferred-substrate HBTs (fig. 1, 3) with 0.3 μm junction dimensions and 6-11 dB power gain at 200 GHz. For optical fiber & mixed-signal ICs (ADCs and DACs), we have developed submicron-geometry mesa devices (fig. 2, 4), and have demonstrated 87 GHz digital ICs. Further submicron scaling at high yield will demand of SiGe-like fabrication processes.

References

[1]M. Rodwell *et al*, International Journal of High Speed Electronics and Systems, Vol. 11, No. 1, pp. 159-215.

[2]M Rodwell *et al*, IEEE Transactions On Electron Devices, Vol. 48, No. 11, November 2001

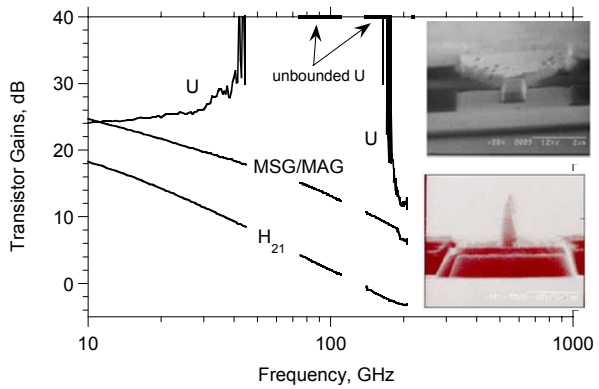

Fig. 1 : Measured mm-wave gains of a InAlAs / InGaAs / InGaAs deep submicron transferred-substrate HBT.

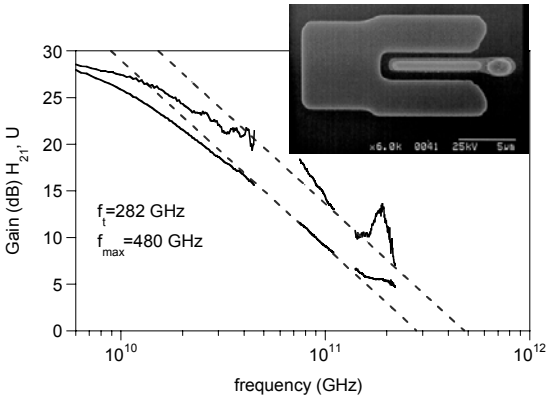

Fig. 2: Measured mm-wave gains of an InP / InGaAs / InP mesa DHBT with a carbon-doped InGaAs base.

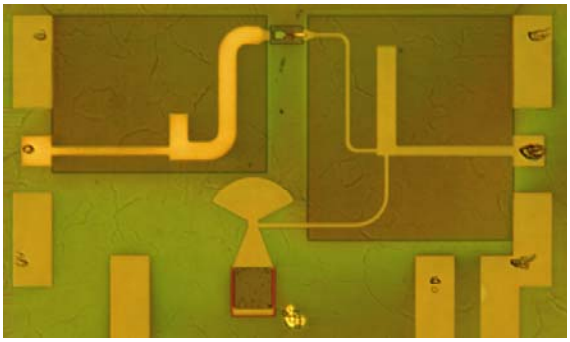

Fig. 3: One-HBT (transferred-substrate) 6.3 dB gain amplifier at 175 GHz

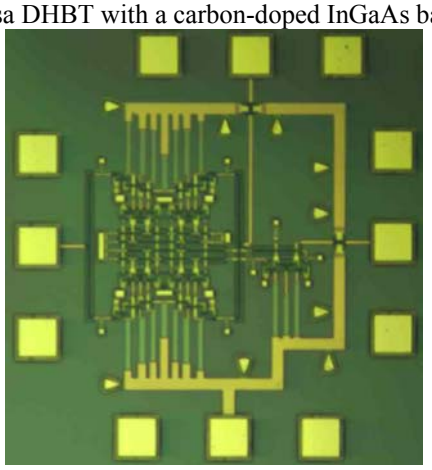

Fig.4: 87 GHz master-slave latch in the InP mesa HBT process

Parameter	Generation 1	Generation 2	Generation 3
Simulated MS-DFF speed	62 GHz	125 GHz	237 GHz
Emitter Junction Width	1 μm	0.8 μm	0.2 μm
Parasitic Resistivity	50 Ω-μm^2	20 Ω-μm^2	5 Ω-μm^2
Base Thickness	400Å	300Å	250Å
Doping	4 10^{19}/cm^2	6 10^{19}/cm^2	8 10^{19}/cm^2
Sheet resistance	750 Ω	700 Ω	700 Ω
Contact resistance	150 Ω-μm^2	20 Ω-μm^2	10 Ω-μm^2
Collector Junction Width	3 μm	1.6 μm	0.4 μm
Collector Thickness	3000 Å	2000 Å	1000 Å
Current Density	1 mA/μm^2	2.3 mA/μm^2	9.3 mA/μm^2
$A_{collector}/A_{emitter}$ (area ratio)	4.55	2.6	2.6
f_τ	170	260	500
f_{max}	170	440	1000
C_{cb}/I_c	1.7 ps/V	0.63 ps/V	0.31 ps/V
$C_{cb}\Delta V_{logic}/I_c$	0.5 ps	0.19 ps	0.093 ps
$R_{bb}/(\Delta V_{logic}/I_c)$	0.8	0.65	0.52
$C_{je}(\Delta V_{logic}/I_C)$	1.7 ps	0.72 ps	0.18 ps
$R_{ex}/(\Delta V_{logic}/I_c)$	0.1	0.15	0.15

Table 1: Technology roadmap for the migration of InP HBT technology from 40 Gb/s through 80 and 160 Gb/s operation.