An 8 GHz continuous time $\Sigma - \Delta$ analog-digital converter in an InP-based HBT Technology

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Abstract

We report an 8 GHz clock-rate, 2nd order continuous-time $\Sigma - \Delta$ analog-digital converter (ADC) that achieves 57.4dB, 51.7dB, and 40.2dB SNR at signal sampling rates of 125Msps, 250Msps, and 500Msps, respectively. The IC occupied 1.45 mm$^2$ die area, contains 76 transistors, is fabricated in an InP-based HBT technology, and dissipates \( \sim 1.8W \). We also study the effect of excess delay on modulator performance, and show that excess delay does not affect performance as long as the centroid-in-time of the DAC pulse remains stationary.

1 Introduction

High speed analog-to-digital converters (ADCs) find widespread applications in wideband communications and radar receivers. Efforts are being made to move the ADC forward in the signal chain, closer to the antenna. Such efforts depend critically on the ability to digitize wideband signals with very high resolution. This modified architecture should result in a more robust receiver implementation consisting of the ADC followed by DSP hardware and software.

A popular oversampling ADC architecture is based on $\Sigma - \Delta$ modulation. These achieve high signal/noise ratio (SNR) without requiring high precision
in component values or device matching. Moreover, the requirements on the analog anti-aliasing filter are significantly relaxed. $\Sigma - \Delta$ modulators achieve high resolution by utilizing high sampling rates; a 2$^{\text{nd}}$ order ADC achieves a 15 dB improvement in SNR for every octave increase in sampling rate.

The SNR of a $\Sigma - \Delta$ modulator depends on the order of the loop filter and the oversampling ratio [1]. While a high-order loop-filter results in a high SNR, it is difficult to design a stable modulator with order greater than two. High SNR can be obtained by using a 2$^{\text{nd}}$ order filter and as high an oversampling ratio as permitted by the technology of implementation. This is our approach. We seek as high a clock rate as is feasible in the technology in order to obtain a high resolution.

InP-based heterojunction bipolar transistors (HBTs) have achieved very high device bandwidths [2], permitting very high speed digital ICs [3]. In bipolar processes, fast, low-offset switches are difficult to implement, and the continuous-time architecture [4] is more readily implemented than the discrete-time, switched-capacitor architecture prevalent in CMOS $\Sigma-\Delta$ ADCs. Continuous-time $\Sigma - \Delta$ modulators have been reported with clock rates as high as 4 GHz [7], 5 GHz [6] and 18 GHz [13]. Here we report an 8 GHz clock-rate, second order continuous time $\Sigma - \Delta$ ADC.

In order to minimise metastability errors in the quantizer, an additional stage of regeneration is necessary. This additional stage introduces excess delay in the loop and the effect of this delay on ADC-resolution is well known [9, 10, 11] and has been studied in detail [8]. In [8], Cherry et al studied the effect of excess delay by considering the equivalence between continuous-time and discrete-time $\Sigma - \Delta$ ADCs. Using such an approach, they were able to predict SNR-degradation in the presence of excess delay and propose solutions to compensate the loss in performance. Here, we provide an alternate analysis of SNR degradation in the presence of excess delay. We compare the linear additive-white-noise model’s predictions with full-loop MATLAB simulations to show that the simple linear model cannot be used to explain the dynamics of an ADC with a 1-bit internal quantizer. We then proceed to show that the
problem can be understood using timing-diagrams, and that the loss in SNR can be recovered by monitoring the centroid-in-time of the DAC pulse, and ensuring that it remains stationary. It is further shown that this can be achieved by using a Return-to-Zero (RTZ) DAC. We conclude by comparing the measured results of two designs, one with no compensation for excess delay, and the other where an RTZ DAC is used to compensate for the excess delay.

2 Device Technology

The circuits are fabricated in a triple-mesa process; both active-junctions are defined by selective wet-etch chemistry [2]. To realise complex mixed-signal ICs, a wiring environment that maintains control of signal integrity and has predictable characteristics to enable robust computer-aided design (CAD) is required. Thin-film-dielectric microstrip-wiring provides controlled-impedance interconnects within dense mixed-signal ICs. The associated ground plane eliminates signal coupling through on-wafer ground-return inductance. Such a wiring environment is added to the process with the addition of a dielectric layer and ground-plane above the IC top-surface wiring planes. We have implemented this by spin-casting a 5\(\mu\)m thick benzocyclobutene (BCB) polymer film, etching vias in BCB and depositing the top ground-plane by electroplating.

Figs. 1 and 2 shows a cross-sectional view of the wiring environment, and an IC micrograph of a master-slave latch after ground-plane plating, respectively.

In such a wiring environment, 8-micron and 3-micron width conductors have controlled 50Ω and 80Ω impedances respectively. Since the dielectric is thin, ground-via inductance is greatly reduced. Interconnects are not significantly coupled for line spacings greater than 10\(\mu\)m. Ground-vias can be closely spaced, as is required in complex ICs. The disadvantage of using a thin dielectric is the increase in skin-loss compared to a conventional microstrip of similar impedance. In addition, the ground-plane reduces line impedances and increases capacitance, thereby increasing node-charging times on unterminated interconnects.
Figure 1: Cross-sectional view of the microstrip wiring environment

Figure 2: Top view of the microstrip wiring environment - Master-Slave latch after plating the Ground Plane
3 Choice of $\Sigma - \Delta$ Architecture: The Problem of Excess Delay

The most common design procedure for continuous-time $\Sigma - \Delta$ modulators is to start with a discrete-time transfer function that will provide maximum baseband attenuation of quantization noise. The discrete-time transfer function is then transformed to the continuous-time domain to obtain a continuous-time transfer function. For a second-order system, it can be shown that the equivalent continuous-time transfer function for the discrete-time filter is given by [8]

$$G(s) = \frac{1 + 1.5sT_s}{s^2T_s^2}$$

where $T_s = 1/f_s$ represents the sampling time. Any excess delay, $\tau$, can be represented as $e^{-j\omega \tau}$ in the frequency domain and is simply a multiplying factor in the loop transfer function (Fig. 3).

The noise transfer function in the frequency domain, $N(j\omega)$, is given by

$$N(j\omega) = \frac{1}{1 + G(j\omega) \cdot e^{-j\omega \tau}}$$

$|N(j\omega)|^2$ can be simplified to

$$|N(j\omega)|^2 = \frac{\omega^4 \cdot T_s^4}{(\omega^2 \cdot T_s^2 \cdot (1 - 1.5\tau/T_s) - 1)^2 + \omega^2 \cdot (1.5T_s - \tau)^2}$$

Consider the effect of $\tau$ on $|N(j\omega)|^2$ at low frequencies, or in other words, the effect of excess delay on the in-band noise suppression. At low frequencies,
the denominator of $|N(j\omega)|^2$ simplifies to its constant term, in this case, unity. $|N(j\omega)|^2$ hence simplifies as

$$|N(j\omega)|^2 = \omega^4 \cdot T_s^4$$  \hspace{1cm} (4)

an expression that is independent of the excess delay, $\tau$. Hence, a linearized-model based analysis predicts that excess delay has no effect on the in-band suppression of the quantization noise at low frequencies, and consequently, on the resolution of the ADC at high OSRs. Further, it is possible to show that by introducing a zero with a time constant $\tau$ in the loop, one can compensate for the excess delay over a wide range of frequencies. Based on this, one would expect that excess delay would have no effect on the SNR at high OSRs. In addition, one would also expect that the effect of SNR can be compensated at lower OSRs also by changing the location of the zero suitably. To verify this, we performed MATLAB simulations on the two circuits i.e. an ADC with a M-S latch based quantizer, and an ADC with a M-S-S latch based quantizer. The circuit block-diagram is shown in Fig. 4. The additional stage of regeneration introduces an extra delay of one-half clock-cycle (25 ps for a 20-GHz clock). Fig. 5 compares the results of a full-loop MATLAB simulation for the two cases. The results of the full-loop simulation are inconsistent with the linear model predictions. We observe considerable degradation in SNR in the presence of excess delay in spite of introducing a zero in the loop. For instance, at an OSR of 128, we see $> 15$ dB SNR-degradation between the two cases.

Given the inconsistency between the linear model’s prediction and the MATLAB simulation, and the fact that the additive white-noise approximation does not hold for a 1-bit quantizer, we conclude that the linear model cannot be used to explain the dynamics of a modulator with a 1-bit internal quantizer. Instead, we propose a timing-diagram based approach. Since the quantizer’s output depends on its input at the sampling instants, it should be possible to recover the loss in SNR by restoring the quantizer inputs to their original values (i.e., the case where the additional stage of regeneration is absent) at the clock transition. Further, since the quantizer inputs depend on the timing and the
Figure 4: Circuit block-diagram for simulating the effect of excess delay using MATLAB

Figure 5: Simulation result: A comparison of the FFT of the output bit-stream for a) a MATLAB simulation of a 2nd order $\Sigma - \Delta$ ADC with a MS latch-based 1-bit quantizer and b) a MATLAB simulation of a 2nd order $\Sigma - \Delta$ ADC with a MSS latch-based 1-bit quantizer. $f_{\text{clock}} = 20$ GHz, $f_{\text{signal}} = 78.125$ MHz, 1.22 MHz FFT bin (resolution)
duration of the DAC pulse, it should be possible to compensate for the loss in
SNR by ensuring that the centroid-in-time of the pulse remains stationary.

Consider the timing diagram shown in Fig. 6. We will use the falling-edge
of the clock as our reference point and compare the centroids-in-time for the
different cases relative to it. With a M-S latch based quantizer (Fig. 6a) and
a NRZ DAC, the centroid-in-time is $T_{clk}/2$ away from the clock transition.
With a M-S-S latch based quantizer (Fig. 6b) and a NRZ DAC, the centroid
is $T_{clk}$ from the clock transition. If our arguments hold, we should be able to
recover any loss in SNR between cases (a) and (b) using the DAC pulse shown
in Fig. 6c. Such a DAC pulse, though, cannot be realized with a M-S-S latch
based quantizer. With a M-S-S latch based quantizer, the DAC pulse will have
to be a delta function (at $\Delta T = T_{clk}/2$) to maintain the position of its centroid-
in-time constant. In order to obtain a reasonable compromise between excess
delay and circuit realizability, we use a RTZ-DAC (Fig. 6d) whose centroid-in-
time is $3T_{clk}/4$ away from the clock transition. We find that the excess delay
of $T_{clk}/4$ (relative to case (a)) can be neutralized by changing the location of
the zero in the transfer function. Excellent agreement is observed between the
output power spectra in the two cases (Fig. 7).

Based on these observations, two ADCs were designed in the mesa-HBT
technology. Both designs use a M-S-S latch as the internal quantizer. While
one design uses a NRZ DAC, the other uses a RTZ DAC to compensate for the
excess delay introduced by the additional stage of regeneration. The following
section discusses some of the circuit-design aspects of the ADC.

4 Circuit Design

Fig. 8 shows a simplified block diagram of the IC. The clock signal to the circuit
is available in a single-ended form from the synthesizer. Clock buffers are used
on-wafer to convert the signal to differential form. This differential clock signal
feeds the comparator and the RTZ DAC. The circuit schematic for the first
integrator is shown in Fig. 9.
Figure 6: The variation of the centroid-in-time of the DAC with choice of quantizer and the nature of the DAC
Figure 7: Simulation result: A comparison of the FFT of the output bit-stream of a) a MATLAB simulation of a 2\textsuperscript{nd} order $\Sigma - \Delta$ ADC with a MS latch and a NRZ DAC. b) a MATLAB simulation of a 2\textsuperscript{nd} order $\Sigma - \Delta$ ADC with a MSS latch and a RTZ DAC with the zero-location altered suitably. In both cases, $f_{\text{clock}} = 20$ GHz, $f_{\text{signal}} = 78.125$ MHz, 1.22 MHz FFT bin (resolution)

Transistors Q3, Q4, Q7 and Q8, in association with the degeneration resistance, $R_{\text{deg}}$, produce a negative resistance to compensate for the effect of the load resistance, $R_{\text{l}}$. As a result, the DC gain of the integrator is greatly increased.

Since it is outside the loop, the linearity of the input stage impacts the dynamic range of the $\Sigma - \Delta$ ADC. It is thus critical that the input transconductance cell be highly linear with minimal distortion. To achieve this, Jensen et al [5] use a linearized input $g_m$ stage based on the Caprio’s cell [12]. In our designs, to minimize circuit complexity, we make the bias current of the transconductance cell much larger than the current fed back by the DAC. This results in a situation where the $\Sigma - \Delta$ loop overloads before the input transconductance cell. Hence, high linearity and minimal distortion are achieved in the input stage. Fig. 10 shows the variation of the fundamental and third-harmonic tones with input power. In our design, the ADC overloads at an input power, $P_{\text{in, max}}$, of -7.5 dBm. At this input power, we observe an intermodulation suppression of
Figure 8: A simplified block diagram of a second-order continuous time $\Sigma-\Delta$ ADC
Component Values

- Cint = 3 pF
- Ra = 666 ohm
- Rb = 666 ohm
- Rdeg = 680 ohm
- Ref = 650 ohm
- Rint = 270 ohm
- Rz = 29 ohm
- Vcc = 1.6 V
- Vee = -3.5 V

Device Geometries

- Q1, Q2, Q3 and Q4 emitter junction dimensions: 0.6 * 7 um^2
- Collector junction dimensions: 2.1 * 13.4 um^2
- Q5, Q6, Q7 and Q8 emitter junction dimensions: 0.6 * 5 um^2
- Collector junction dimensions: 2.1 * 11.4 um^2

Figure 9: Circuit Schematic of the First Integrator
We observe an intermodulation suppression of 88 dBc at an input power of -7.5 dBm. In addition, the input stage contributes thermal and shotnoise, and can limit the SNR. Using a calculation similar to that shown in [13], we estimate the input-noise limited SNR to be 153dB (1Hz).

The circuit schematic of the second integrator is similar to the first integrator. The quantizer is an 87 GHz [3] master-slave-slave flip-flop. While the NRZ-DAC is a simple current-switching pair, the RTZ-DAC has two levels of switching, one for the data and one for the clock. To maintain the charge fed back by the DAC constant in the two cases, the RTZ-DAC uses a bias current four times higher than the NRZ-DAC. The error signal is generated by current summing at the output nodes of the first transconductance cell. The following section describes the measurement setup and the measured results.

5 Measurement and Results

The IC Micrograph of the RTZ-DAC-based ADC is shown in Fig. 11. The design consists of 76 transistors and dissipates 1.5W.
Fig. 12 compares the output-power-spectrum, as viewed on a spectrum analyzer, for the two circuits. We observe that, in agreement with our simulations, the RTZ-DAC-based ADC has better resolution than the NRZ-DAC-based ADC. We believe that the improved performance of the RTZ-DAC-based ADC is due to its lower loop delay. We also observe that the noise-level for the RTZ-DAC-based ADC is constant at the lower end of the spectrum. Digital acquisition of the bit-stream is necessary to ensure that we are not limited by the dynamic range of the spectrum analyzer, and to predict the performance of the RTZ-DAC-based ADC correctly. We now discuss the results of such logic analyzer-based digital acquisition measurements. For the remainder of this section, the term ADC will refer to the RTZ-DAC-based ADC unless otherwise mentioned.

We capture the digital data stream by first demultiplexing it into 16 channels of 500 Msp/s each using a commercial 10G DEMUX. The data from the 16 channels is then read into a logic analyzer and transferred to a computer. The original 8 Gbps waveform is then reconstructed in software and a MATLAB-based program is used to perform a fast-Fourier transform (FFT) on this reconstructed waveform. We perform a 131072-point FFT for both one-tone and
Figure 12: A Comparison of the Output Power Spectra of the NRZ-DAC-based ADC and the RTZ-DAC-based ADC as measured on an analog spectrum analyzer

Table 1: SNR and ENOB using noise power integrated over signal bandwidth

<table>
<thead>
<tr>
<th>Signal Frequency</th>
<th>Equivalent Sampling rate</th>
<th>SNR, dB 61 kHz</th>
<th>SNR, dB 1 Hz</th>
<th>SNR, dB Nyquist</th>
<th>ENOB</th>
</tr>
</thead>
<tbody>
<tr>
<td>62.5 MHz</td>
<td>125 Ms/s</td>
<td>87.54</td>
<td>135.39</td>
<td>57.4</td>
<td>9.25</td>
</tr>
<tr>
<td>125 MHz</td>
<td>250 Ms/s</td>
<td>84.8</td>
<td>132.65</td>
<td>51.7</td>
<td>8.29</td>
</tr>
<tr>
<td>250 MHz</td>
<td>500 Ms/s</td>
<td>76.3</td>
<td>124.15</td>
<td>40.2</td>
<td>6.38</td>
</tr>
</tbody>
</table>

two-tone measurements.

Fig. 13 plots the calculated 131072-point FFT spectrum for a 62.5-MHz input. The oversampling ratio (OSR) is 64 and the input power is 3 dBm. For single-tone measurements, the SNR and the effective number of bits (ENOB) of resolution for a Nyquist-rate ADC are related by the expression

\[
ENOBN = (SNR - 1.76)/6.02
\]

[14]. We have calculated the SNR and ENOB using the noise power integrated over the signal bandwidth. The results are presented in Table 1 at different signal frequencies.

We observe that noise-shaping is absent at frequencies lower than 100MHz.
Figure 13: Output Power Spectrum of the ADC obtained by a 131072-pt. FFT performed on digital data acquired at 8 Gbps

We also observe that the loop does not show ideal behaviour at any of the tested signal-frequencies. For example, the SNR for an ideal 2nd order Σ – Δ modulator, at an OSR of 32, is 55 dB. We observe an SNR of 48 dB. We attribute this behavior to residual metastability errors in the quantizer, and to delays associated with latch latency.

To investigate the linearity of the input transconductance stage, we performed two-tone measurements on the ADC.

Fig. 14 shows the output power spectrum for two tones at 124 and 126 MHz. We observe > 80 dBc suppression of the two-tone intermodulation products. For this measurement, the comparator was not biased for maximum speed. Due to a design oversight, we do not use separate voltage sources for the integrator, the comparator and the DAC. For this reason, the bias current in the DAC increases at a much faster rate than the bias current in the integrator, when the supply-voltage is increased. Hence, we observe only 70 dBc suppression of the two-tone intermodulation products at the best bias-point (Fig. 15).

Based on these results, we conclude that, at the cost of increased DC power, sufficient intermodulation suppression can be achieved by ensuring that the
Figure 14: Third-Order Distortion for a two-tone input at 124 and 126 MHz; The
intermodulation products are below the noise-floor and hence, are not visible

Figure 15: Third-Order Distortion for a two-tone input at 124 and 126 MHz;
the comparator is biased for maximum-speed
input stage overloads well after loop-overload occurs.

6 Conclusions

We have demonstrated an 8-GHz clock-rate, second-order, continuous-time $\Sigma - \Delta$ ADC in an InP-based mesa-HBT technology. The ADC achieves SNR of 57.4 dB, 51.7 dB and 40.2 dB, corresponding to 9.25, 8.29 and 6.38 effective bits at signal sampling rates of 125 Msps, 250 Msps and 500 Msps, respectively. The IC occupies a die area of 1.45 mm$^2$, contains 76 transistors and dissipates 1.8 W of power. In addition, we have also proposed, given the inability of a linear additive white-noise model to explain the dynamics of a 1-bit internal quantizer, a centroid-in-time based approach to neutralise the effect of excess delay on modulator performance.

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References


