Low-voltage, high-performance InAs/AlSb HEMTs with power gain above 100 GHz at 100 mV drain bias

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Ultra-low power circuits require transistors with usable RF gain at low bias voltages and currents. In the present paper, we report 100 nm gate-length InAs/AlSb HEMTs with f_τ and f_{max} both exceeding 100 GHz at a mere 100 mV of drain bias. The devices also show excellent peak value for f_τ of 235 GHz and, to the best of our knowledge, a record f_{max} of 235 GHz at a higher drain bias of 300 mV. Previous work on the low-voltage RF properties of InAs/AlSb transistors by Boos *et al*. reports an f_τ of 90 GHz for a 60 nm gate-length device, with an f_τ / f_{max} ratio of 2 [1]. From the published layer structure and RF performance reported by Boos *et al*., it appears that their devices may have suffered from short-channel effects caused by inadequate vertical scaling of the channel and the top barrier. In fact, high values for f_{max} for InAs/AlSb HEMTs are rare or non-existent in the published literature. Even the most recent work reported InAs/AlSb HEMTs with high f_τ values of 212 GHz for a 100 nm gate-length device (V_{ds} = 400 mV), while f_{max} was below 200 GHz [2]. The highest reported f_τ for an InAs-channel device is 308 GHz, which employed (relatively smaller bandgap) InAlAs barriers and produced an f_{max} of 110 GHz at a gate-length of 70 nm [3].

To realize transistors with simultaneously high f_τ and f_{max} with 100 nm long gates, we scaled our composite top barrier consisting of AlSb and $In_{0.5}Al_{0.5}As$ to a total thickness of 14 nm (typically 18-25 nm). The AlSb layer, with a 1.6 eV bandgap, provides excellent electron confinement, and the $In_{0.5}Al_{0.5}As$ layer acts as a stable low-leakage cap [1]. In addition, the InAs quantum well width was reduced to 10 nm (typically 15 nm). The resulting vertically scaled layer structure maintains a good low-field Hall mobility of 18,000 cm^2/Vs at a sheet charge of 2.1×10^{12} cm^{-2}. The electron velocity in the device remains high as evidenced by a drain current of 800 mA/mm and an RF g_m of 1500 mS/mm at 500 mV drain bias. Note that the DC values of g_m observed in these devices (> 2000 mS/mm for the present transistor) are artificially high due to the positive charge supplied by holes generated through impact ionization by hot electrons in the drain. The devices exhibit excellent gate control with a very low gate-leakage linear current density of 2 nA/μm at −200 mV gate bias.

The structures reported in the present work were grown on semi-insulating GaAs substrates in a Varian Gen II MBE machine employing valved, cracked, antimony and arsenic sources. The device fabrication used a conventional mesa-isolation process and diffused ohmic contacts with >10 MΩ device-to-device isolation and 0.06 Ω-mm contact resistance. The 100 nm gates were written with a JEOL 6000FS/E electron beam lithography machine, and the gate metal was deposited directly on the as-grown surface without the need for recess etching. Our process produces >95% device-level yield for the 100 nm gate-length transistors with a threshold voltage variation of less than 10 mV across a 50 mm-diameter wafer. Parasitic capacitances were carefully de-embedded using a combination of on-wafer calibration structures and EM simulation of the pad layouts. The accuracy of the de-embedding method was verified by measuring devices with varying gate lengths and widths.

[1] J. B. Boos *et al*., *JVST-B*, vol. 17, pp. 1022-1027, 1999.
[2] R. Tsai *et al*., *Technical Digest of 2003 GaAs IC Symposium*, pp. 294-297, 2003.
[3] Y. Royter *et al*., *Proc. Int. Electron Devices Meeting*, pp. 30.7.1-30.7.4, 2003

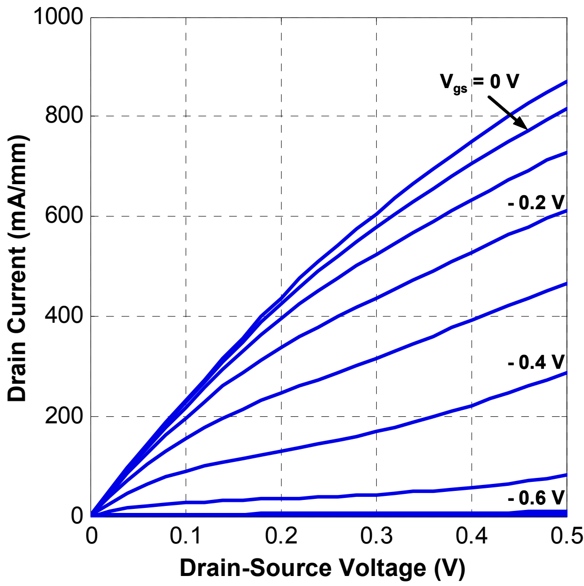

Figure 1. The DC output characteristics of the vertically scaled 100 nm gate length InAs/AlSb HEMT. Drain currents above 800 mA/mm are observed with excellent pinch-off. The gate diode leakage current (not shown) is 2 nA/µm at -200 mV gate bias

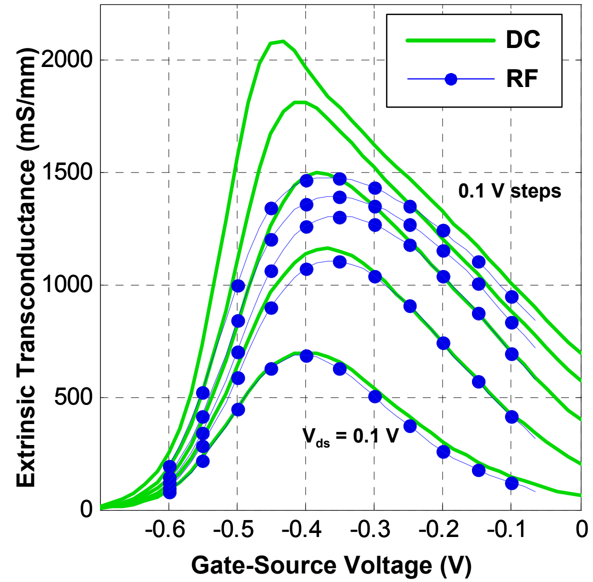

Figure 2. The RF g_m exhibits a high peak value of 1500 mS/mm at V_{ds} = 500 mV, indicative of high electron velocities in the channel. The DC transconductance peaks at over 2000 mS/mm at a drain bias of 500 mV; artificially enhanced by feedback of impact-generated holes.

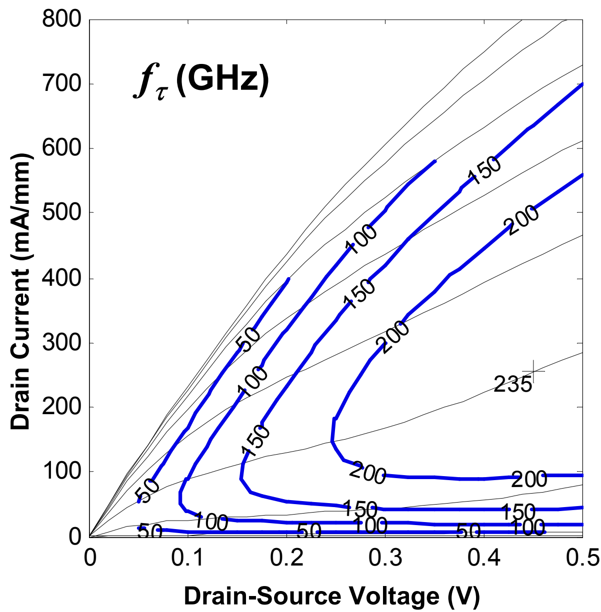

Figure 3. f_τ contours show a peak of 235 GHz at a drain bias of 450 mV, and indicate that the InAs/AlSb HEMT maintains a high f_τ at very low drain voltages.

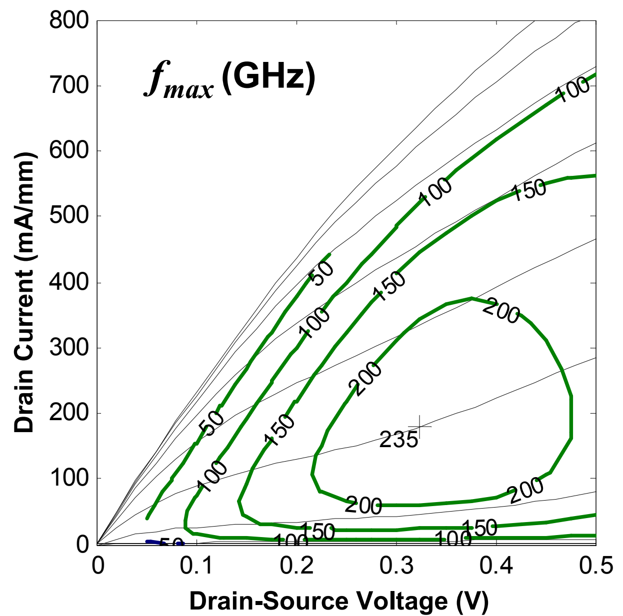

Figure 4. f_{max} contours show a peak of 235 GHz at a drain bias of 300 mV. f_{max} remains above 100 GHz at drain biases as low as 100 mV.