60nm collector InGaAs/InP Type-I DHBTs demonstrating 660 GHz f_τ, BV_{CEO} = 2.5V, and BV_{CBO} = 2.7V

Zach Griffith*, Erik Lind*, and Mark J.W. Rodwell*
*Dept. of Electrical and Computer Engineering
University of California, Santa Barbara, CA 93106-9560, USA
Phone: 805-893-5999, E-mail: griffith@ece.ucsb.edu

Xiao-Ming Fang†, Dmitri Loubychev†, Ying Wu†, Joel M. Fastenau†, and Amy W.K. Liu†
†IQE Inc., 119 Technology Drive, Bethlehem, PA 18015, USA

***Abstract*— We report InP/InGaAs/InP double heterojunction bipolar transistors (DHBT) fabricated using a conventional mesa structure. The devices employ a 14 nm highly doped InGaAs base and a 60 nm InP collector containing an InGaAs/InAlAs superlattice grade. Devices employing a 400 nm emitter exhibit a maximum f_τ = 660 GHz with a 218 GHz f_{max} – this is a record f_τ for a DHBT. The devices have been scaled vertically for reduced base and collector electron transit times, and the base-collector mesa has been further scaled to minimize the capacitance C_{cb} associated with the base contact area. The peak current gain $\beta \approx$ 95, BV_{CEO} = 2.5 V, BV_{CBO} = 2.7 V, and the devices operate in excess of 30 mW/μm^2.**

***Index Terms*— InP heterojunction bipolar transistor**

I. Introduction

Amongst InP HBT manufacturers, efforts are now under way both to obtain high circuit yield at $>$ 10,000 devices per IC and to simultaneously extend device and circuit bandwidth, where the typical emitter junction width is $\sim$ 500 nm. From geometric scaling theory [1], [2], the key HBT scaling challenges for balanced increases to f_τ, f_{max}, and digital logic speed are: making narrower emitter and collector junctions, and reducing the emitter and base Ohmic contact resistivity, while being able to operate the device at higher current densities in the limit expected by the Kirk effect $J_{max} \propto T_c^{-2}$. At the 250 nm emitter node, the scaling requisites include an emitter and base $\rho_{c,e}$ = 9 $\Omega \cdot \mu$m^2 and $\rho_{c,b}$ = 10 $\Omega \cdot \mu$m^2, a collector to emitter area ratio A_c/A_e = 2.4, and a J_{max} = 9 mA/μm^2. Recent modifications to the HBT process at UCSB have allowed these scaling requisites to be satisfied at the 250 nm node through the use of I-line lithography and results employing a 150 nm collector have been reported [3], having a simultaneous 420 GHz f_τ, 650 GHz f_{max}. The work presented here looks to investigate the challenges associated with vertical scaling for the 125 nm and 62.5 nm emitter scaling nodes – where the effects of epitaxial scaling on breakdown, current density, transit time, and thermal resistance can be measured on HBTs with larger emitter dimensions, as was done here.

Prior to this work, the highest f_τ reported for an InP DHBT was 544 GHz with an f_{max} of 347 GHz, having a 20 nm base and 75 nm collector [4], where BV_{CEO} = 3.2 V and BV_{CBO} = 3.4 V. Here we report InGaAs/InP DHBTs having a 14 nm base and 60 nm collector, exhibiting a peak 660 GHz f_τ, a record for a DHBT, simultaneous with 218 GHz f_{max} and breakdown voltages BV_{CEO} = 2.5 V, and BV_{CBO} = 2.7 V at $J_{e,c}$ = 1 kA/cm^2. In comparison, InGaAs collector InP SHBTs having a 20 nm base, 62.5 nm collector have demonstrated 604 GHz f_τ and 246 GHz f_{max} [5]. Additionally, 12.5 nm base, 55 nm collector InP SHBTs have demonstrated 710 GHz f_τ and 340 GHz f_{max} [6]. Both devices report a breakdown voltage BV_{CEO} = 1.7 V. The results reported here provide evidence that at similar base and collector thicknesses, type-I InP DHBTs (where base-collector grading is required) are continuing to demonstrate competitive bandwidths in comparison to their InP SHBT counterpart, while having significantly higher breakdown voltages and maximum operating power density before failure.

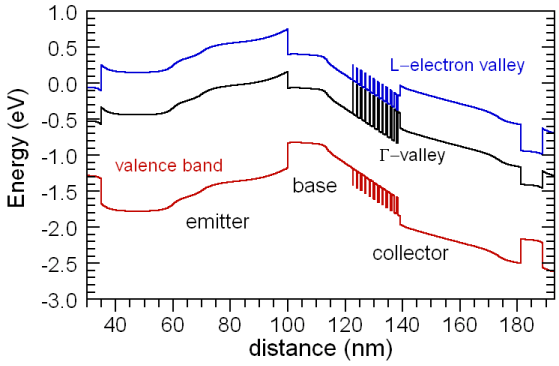
II. Design

The full Type-I InP DHBT layer structure is shown in Table I, and the associated band diagrams [7] of the device at an applied bias of V_{be} = 0.95 V, V_{cb} = 0.0 V for J_e = 0, J_{Kirk}, and 1.5·J_{Kirk} are shown in figures 1a-c.

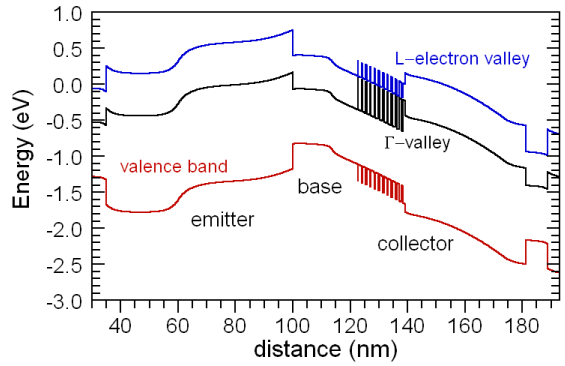
A base thickness of 14 nm was selected having a doping grade of 10-7·10^{19} cm^{-3}:C that in-turn produces $\sim$ 35-40 meV of conduction band grading to establish a quasi-field across the base. Assuming 100% carbon activation at these doping levels employed across the base, an average hole mobility $\mu_h \cong$ 36 cm^2/V·sec is extracted from the measured base sheet resistance.

Through the previous collector scaling generations of UCSB InP DHBTs (from 200 nm down to 150, 120, 100, 75 nm), the InGaAs setback and InP layers were progressively thinned – the InGaAs/InAlAs grade and InP δ-pulse doping were kept unchanged. In order to maintain higher breakdown voltages and lower device self-heating at similar bias conditions compared to InP SHBTs, both the

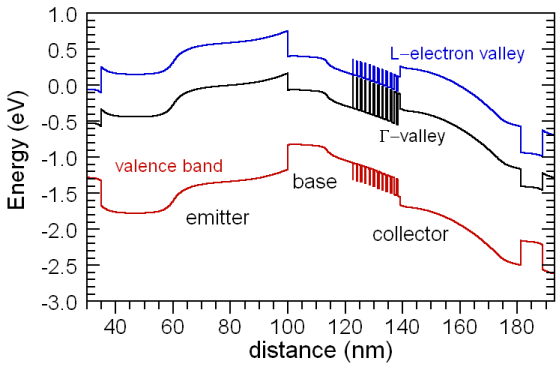
1-4244-0127-5/06/$20.00



(a) V_{be} = 0.95 V, V_{cb} = 0.0 V, J_e = 0 mA



(b) V_{be} = 0.95V, V_{cb} = 0.0V, $J_e = J_{Kirk} \sim$ 14mA/μm^2



(c) V_{be} = 0.95 V, V_{cb} = 0.0 V, $J_e \sim 1.5 \times J_{Kirk}$

Fig. 1. Simulated band-diagram: 60 nm collector, 14 nm base InP DHBT

TABLE I
INP DHBT EPITAXIAL LAYER STRUCTURE

Thickness,nm	Material	Doping, cm^{-3}	Description
10	$In_{0.85}Ga_{0.15}As$	$5 \cdot 10^{19}$: Si	Emitter cap
15	$In_xGa_{1-x}As$	$4 \cdot 10^{19}$: Si	Cap grading
10	$In_{0.53}Ga_{0.47}As$	$4 \cdot 10^{19}$: Si	Emitter cap
85	InP	$3 \cdot 10^{19}$: Si	Emitter cap
10	InP	$1.2 \cdot 10^{18}$: Si	Emitter
30	InP	$1.0 \cdot 10^{18}$: Si	Emitter
14	InGaAs	10 - $7{\cdot}10^{19}$: C	Base
7.5	InGaAs	$7.5 \cdot 10^{16}$: Si	Setback
18	InGaAs/InAlAs	$7.5 \cdot 10^{16}$: Si	B-C grade
3	InP	$3 \cdot 10^{18}$: Si	δ - doping
31.5	InP	$7.5 \cdot 10^{16}$: Si	Collector
7.5	InP	$1.0 \cdot 10^{19}$: Si	Subcollector
7.5	$In_{0.53}Ga_{0.47}As$	$2 \cdot 10^{19}$: Si	Subcollector
300	InP	$2 \cdot 10^{19}$: Si	Subcollector
—	InP	Semi-insulating	Substrate

setback *and* grade were thinned for the DHBTs reported here. The setback was thinned to 7.5 nm and the grade was thinned in the following manner: 1/4 of the superlattice periods were removed, the InGaAs/InAlAs alloy ratios adjusted for each period such that the alloy ratios of the first and last periods were consistent with the thicker 24 nm grade, and the pulse doping appropriately increased. From the Bandprof simulation of the HBT shown in figure 1b, electrons entering the collector from the base are accelerated by the $\sim$ 230 meV of potential difference across the conduction band of the setback layer before entering the grade at a simulated current density J_e = 14 mA/μm^2 and V_{cb} = 0.0 V. At higher simulated values of J_e, the potential difference across the setback changes little; however the field across the grade progressively reverses (fig. 1c) and significant reductions in the electron velocity in the collector is expected.

III. GROWTH AND FABRICATION

The epitaxial material was grown by IQE Inc. on a 3" semi-insulating InP wafer and the HBTs were fabricated in an all wet-etch, standard triple mesa process. All physical features of the DHBT were defined by I-line projection lithography. The narrowest emitter contact feature that can be realized is 400 nm. The wet-etch of the emitter semiconductor forms an undercut as small as 50 nm per side, such that 300 nm wide emitter junctions and smaller can be formed in this self-aligned base process. The devices are passivated with and the wafer is planarized in benzocyclobutene (BCB) to minimize device leakage currents associated with semiconductor surface states. BCB also provides a low-ε_r spacer (ε_r = 2.7,

1-4244-0127-5/06/$20.00 ©2006 IEEE

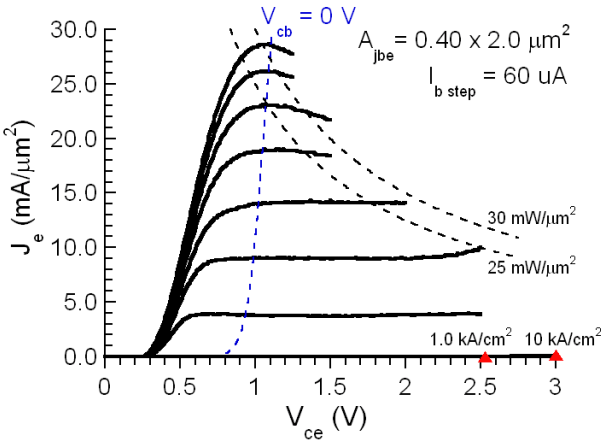


Fig. 2. Common-emitter I-V characteristics

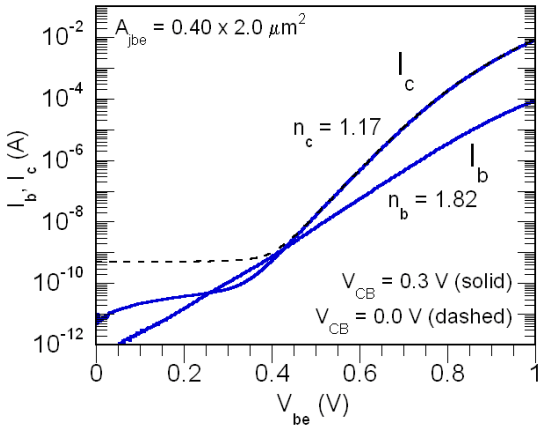


Fig. 3. Gummel characteristics

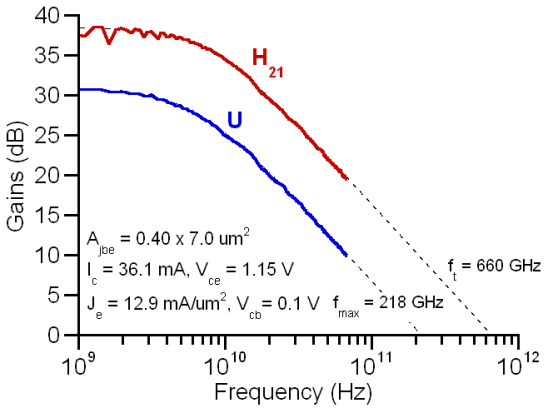


Fig. 4. Measured microwave gains associated with peak 660 GHz f_τ

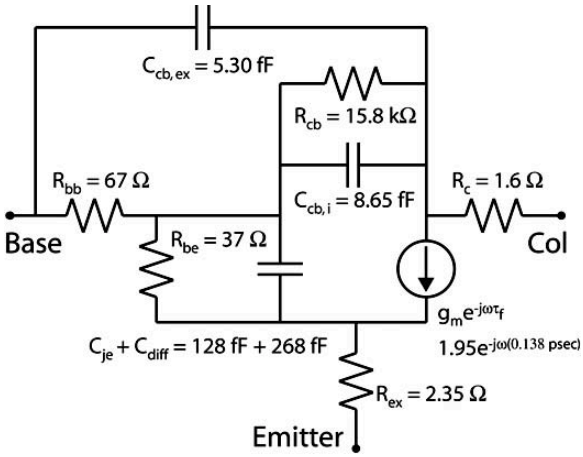


Fig. 5. Hybrid-π equivalent circuit at the bias associated with peak 660 GHz f_τ from figure 4.

T$_{BCB}$ = 1.6 μm) between the device interconnects and InP substrate to reduce spurious resonances in the RF measurements through substrate mode coupling.

IV. Measurements and Results

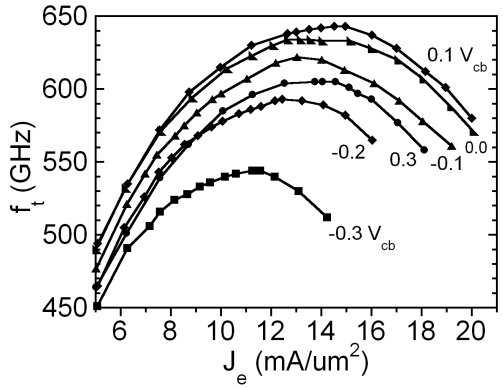
Standard transmission line measurements (TLM) show the collector sheet resistance ρ_s = 12.1 Ω and Ohmic contact resistance ρ_c = 4.7 $\Omega \cdot \mu$m^2. TLM extraction of the base Ohmic contact resistance produced values of $\rho_c \geq$ 200 $\Omega \cdot \mu$m^2; however, the value of base resistance R_{bb} determined from RF parameter extraction suggests the base ρ_c is more likely 70 $\Omega \cdot \mu$m^2. The emitter Ohmic contact resistance from RF parameter extraction varies between ρ_c = 5.5 to 7.0 $\Omega \cdot \mu$m^2.

The common-emitter current-voltage and Gummel characteristics are shown in figures 2 and 3, respectively The DHBTs have a peak current gain $\beta \cong$ 95, and common-emitter and common-base breakdown voltages BV$_{CEO}$ = 2.5 V and BV$_{CBO}$ = 2.7 V (at $J_{e,c}$ = 1.0 kA/cm^2). The collector and base ideality factors are n_c = 1.17 and n_b = 1.82 respectively, and a low collector leakage current I_{cbo} < 500 pA (V_{cb} offset = 0.3 V) is observed.

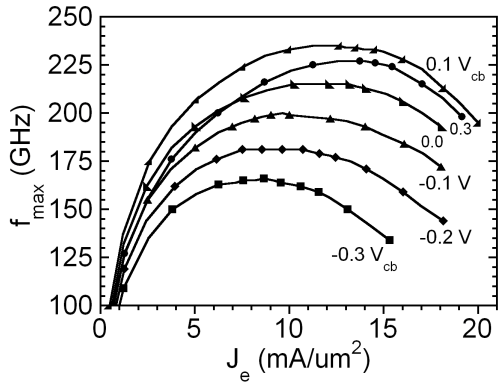
DC-67 GHz RF measurements were carried out after performing an off-wafer Line-Reflect-Reflect-Match (LRRM) calibration on an Agilent E8361A PNA. An open and short circuit pad structure identical to the one used by the devices was measured after calibration in order to de-embed their associated parasitics from the S-parameter measurements. From an HBT having emitter dimensions A_{je} = 0.40 × 7.0 μm^2, a peak 660 GHz f_τ with a 218 GHz f_{max} (fig. 4) were determined from extrapolation through a least-square-fit between the transfer functions

$$|H_{21}(f)|^2 = \frac{H_{21,DC}}{1 + H_{21,DC} \cdot (f/f_\tau)^2} \quad (1)$$

$$U(f) = \frac{U_{DC}}{1 + U_{DC} \cdot (f/f_{max})^2} \quad (2)$$



(a) Variation of f_τ with J_e and V_{cb}



(b) Variation of f_{max} with J_e and V_{cb}

Fig. 6. Trend of f_τ and f_{max} for various bias conditions. A_{je} = 0.40 × 5.0 μm^2, A_{jc} = 0.65 × 7.0 μm^2.

TABLE II

VARIATION OF PEAK f_τ ASSOCIATED WITH DIFFERENT EMITTER DIMENSIONS. NOTE: FOR ALL DEVICES, THE COLLECTOR MESA EXTENDS 150 NM PER SIDE OF THE EMITTER MESA.

A_{je}	f_τ	J_e	C_{cb}/I_c	f_{max}
0.40 × 2.0	580	15.1	0.62	249
0.40 × 3.0	600	13.5	0.54	228
0.40 × 5.0	643	14.5	0.39	230
0.40 × 7.0	660	12.9	0.39	218
0.40 × 9.0	618	13.9	0.45	186
0.30 × 5.0	634	15.2	0.47	259
0.35 × 5.0	629	12.9	0.48	238
0.45 × 5.0	654	13.9	0.38	220
0.45 × 7.0	657	12.8	0.37	201
0.30 × 2.0	539	14.9	0.73	294
0.55 × 5.0	641	13.2	0.36	196
μm^2	GHz	mA/μm^2	ps/V	GHz

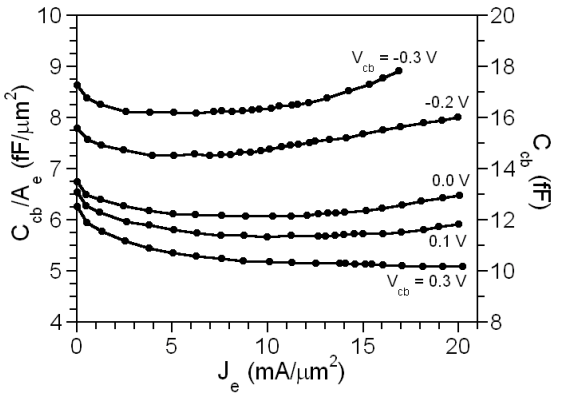


Fig. 7. Variation of C_{cb} with V_{cb} and J_e. A_{je} = 0.40 × 5.0 μm^2, A_{jc} = 0.65 × 7.0 μm^2.

to the measured microwave gains H_{21} and U at measured frequencies at a bias of I_c = 36.1 mA and V_{ce} = 1.15 V (V_{cb} = 0.1 V, J_e = 12.9 mA/μm^2, C_{cb}/I_c = 0.39 ps/V). A hybrid-π equivalent circuit (fig. 5) of this device was generated from the measured S-parameters and device parameters modeled at the bias associated with peak 660 GHz f_τ. Table II details the variation of peak f_τ for different emitter junction dimensions, and the variation of f_τ and f_{max} with operating current density J_e and base-collector potential V_{cb} are shown in figures 6a and 6b. Figure 7 shows the variation of C_{cb} versus operating J_e and V_{cb} for use in current mode logic (CML) circuit design.

ACKNOWLEDGMENT

This work was supported by DARPA under the TFAST program N66001-02-C-8080, the DARPA SWIFT program, and by the ONR under N0001-40-4-10071.

REFERENCES

[1] M.J.W. Rodwell et al., "Submicron Scaling of HBTs" *IEEE Trans. on Electron Devices*, Vol. 48, pp. 2606-2624, November 2001.

[2] M.J.W. Rodwell et al., "Developing bipolar transistors for Sub-mm-wave amplifiers and next-generation (300 GHz) digital circuits", *Device Research Conference*, Penn State, PA, June, 26-28, 2006.

[3] E. Lind et al., "250nm InGaAs/InP DHBTs w/ 650 GHz f_{max} and 420 GHz f_τ, operating above 30mW/μm^2", *Device Research Conference*, Penn State, PA, June, 26-28, 2006.

[4] Z. Griffith et al., "InGaAs/InP DHBTs with a 75nm collector, 20nm base, demonstrating 544 GHz f_τ, BV_{CEO} = 3.2V, and BV_{CBO} = 3.4V", *IEEE Int. Conf. on Indium Phosphide and Related Materials*, Princeton, New Jersey, May, 7-11, 2006.

[5] W. Hafez et al., "Experimental demonstration of pseudomorphic heterojunction biploar transistor with cutoff frequencies above 600 GHz", *Applied Physics Letters*, vol. 86, no. 152101, pp. 1-3, 2005.

[6] W. Hafez et al., "12.5nm base pseudomorphic heterojunction bipolar transistors achieving f_τ = 710 GHz and f_{max} = 340 GHz", *Applied Physics Letters*, vol. 87, no. 252109, pp. 1-3, 2005.

[7] Bandprof, Semiconductor Device Simulation Tool, Prof. W. Frensley, University of Texas, Dallas.