A MIXED-SIGNAL ROW/COLUMN ARCHITECTURE FOR VERY LARGE MONOLITHIC mm-WAVE PHASED ARRAYS

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The range of mm-wave radio communications is severely constrained by high losses arising from the short wavelength and from atmospheric attenuation. Large phased arrays can overcome these limitations, but it is very difficult to realize them using present monolithic beamsteering IC architectures. We propose an alternative architecture for large monolithic phased arrays. The beam is steered in altitude and in azimuth by separately imposing vertical and horizontal phase gradients. This choice reduces IC complexity, making large arrays feasible. Since extensive digital processing provides robust amplitude control and reduces die area, the LOs are processed as digital signals. Being very sensitive to compression, the IF signals are processed as analog signals and distributed by means of synthetic transmission-line buses. With careful frequency planning, this mixed-signal approach can allow large phased arrays to operate at frequencies much higher than those achievable with pure analog design.

Keywords: Phased array; Mixed-signal design; mm-Wave.

1. Introduction

The large bandwidth available for mm-wave radio communications allows data rates in the $1 - 10$ Gbit/s range. The usable link range of these channels is severely constrained by the short wavelength and the atmospheric attenuation. The channel loss can be expressed as

$$\frac{P_{rx}}{P_{tx}} = \frac{D_t D_r}{16\pi^2} \left(\frac{\lambda}{R}\right)^2 e^{-\alpha R} \tag{1}$$

where $P_{rx,tx}$ and $D_{rx,tx}$ are power and antenna directivities at receiver and transmitter sides, R is the link range. Apparently, large antenna directivities can enable large ranges: if N-element transmit and receive arrays are used, then $D \sim \pi N$, $P_{tx} \propto N$ and $P_{rx} \propto N^3$. Using 32×32 arrays, link SNR is increased ~ 90 dB, permitting e.g. 10 Gbit/s *mobile* communication over a long ~ 1 km range, even in heavy rain[1]. Two issues arise form the use of arrays. First, unless antennas are fixed, such a high directivity requires electronic beam steering. Second, the element pitch must be smaller than $\lambda/2$, and this constrains maximal area per element in a bi-dimensional array. This area must accommodate beam steering, LNA, PA and

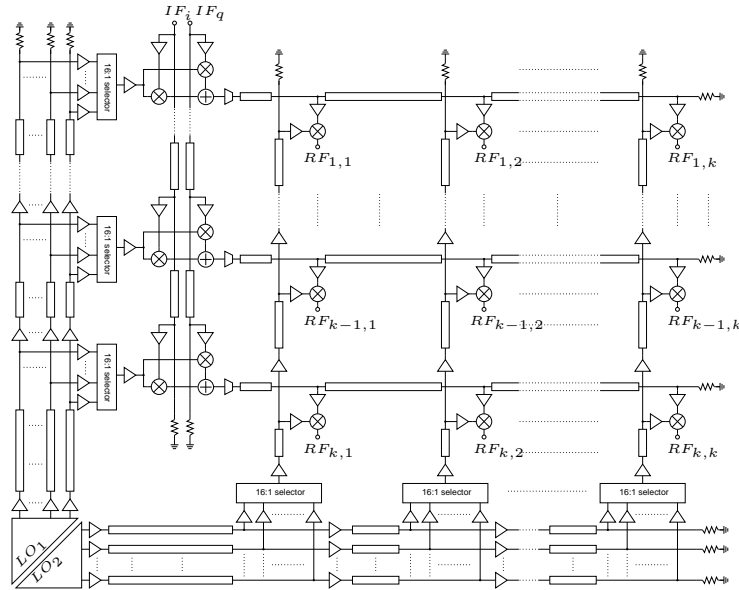2   *Corrado Carta, Munkyo Seo and Mark Rodwell*

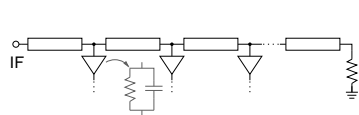Fig. 1. System architecture of a large monolithic phased array.
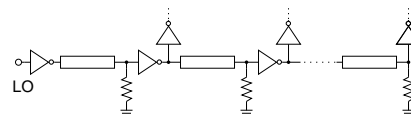

Fig. 2. The synthetic t-line IF bus.

Fig. 3. LOs are processed as digital signals.

T/R switch: as frequency increases, integration becomes necessary. Modern and non-expensive Si technologies offer performances sufficient for the $30 - 100$ GHz range and are, thus, suitable for the integration of monolithic mm-wave arrays.

While the integration of large arrays is attractive, it is very difficult to realize them with present beamsteering IC architectures[2,3]. In this paper, we propose an alternative architecture, which bases its operation on steering the beam in altitude and azimuth by separately imposing vertical and horizontal phase gradients. This simple assumption enables a neat separation of IF and LO distribution lines, and allows improvements in both array size and maximal operation frequency.

2. System Architecture and Design

The system architecture we propose for large monolithic arrays is illustrated in Fig. 1 with a $k \times k$ double-upconversion transmitter. Making use of two LO signals, the input I-Q IF signals are first multiplied by a vertical phase gradient, then an independent horizontal gradient is applied and summed by means of a second up-
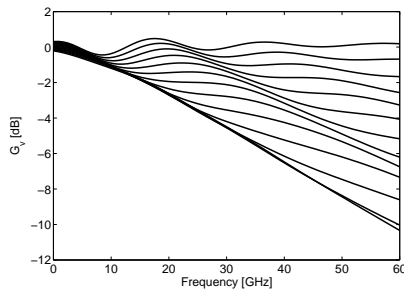
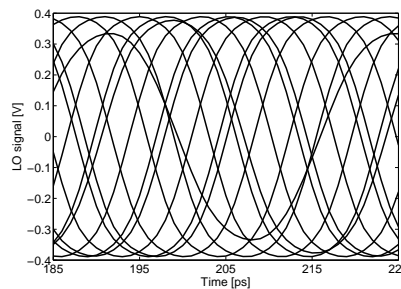Fig. 4. Voltage gain at thirteen tap points along an IF bus.

Fig. 5. Time domain simulation of a fifteen tap-point 30 GHz LO bus.

conversion mixing. This allows the IC to steer the beam in altitude and azimuth, with minimal wiring complexity. In a N-element array, the number of IF buses and phase selectors grows as $2\sqrt{N}$, not as N. IC complexity is reduced, making large arrays feasible. In terms of maximal array dimension, the fundamental limitation of this architecture is in the maximum number of elements per row and column that can be reached with IF and LO buses without excessive signal degradation.

IF synthetic transmission-line bus — The IF signals are analog and must be processed avoiding compression. We propose to distribute the IF signals along transmission-line buses, which absorb their periodic gate loading capacitance into synthetic transmission-lines. As shown in Fig. 2, the design is similar to a distributed amplifier and avoids area-inefficient reactively-matched subcircuits.

Fig. 4 shows the simulation of an IF bus. The transmission lines are modeled as microstrips in a standard six-metal RF BiCMOS technology (0.18 μm); the line is loaded every 300 μm with the input of an active upconversion mixer in the same technology. The application will set the maximum number of tap points. For example, in applications which can tolerate 2 dB of attenuation, more than 10 tap points could be used at 15 GHz. Depending on the frequency plan, this relatively low IF frequency would not necessarily limit the output RF frequency: a 45 GHz RF would be possible with a first LO at 15 GHz and a second at 30 GHz. The baseband or first IF signal would travel on a low speed IF bus, the second IF signal on a 15 GHz IF bus, in order to be dstributed and mixed with the 30 GHz second LO. This approach, while relaxing significantly the performance requirements for the IF bus, requires a different design strategy for the LO buses, which need to operate at much higher frequencies with the same number of tap points.

LO digital bus — For relatively low frequency applications, or for small-size arrays, the synthetic transmission-line approach can be considered for the LO bus as well: it offers the advantage of being entirely passive. On the other hand, the synthetic transmission line is linear, and common microwave mixers do not need the LO

signal to be linear. We propose to trade linearity for maximal frequency of operation
by processing LO signals as digital signals, using ECL selectors, transmission-line
drivers and repeaters. Fig. 3 shows the schematic of the LO bus: digital inverters
are designed to drive terminated transmission-lines; at each tap point the signal
is restored. The loading gates can be either mixer LO ports or selector inputs, all
ECL compatible. While saturating the signal amplitude, the digital inverters are
able to preserve the phase information and provide very robust signal restoration
up to their maximal operation frequency. Fig. 5 shows the simulation of the time-
domain signal at fourteen 300 μm-spaced tap points on a 30 GHz LO bus. The two
smallest-amplitude signals are the output of the first two buffers from the input of
the bus: after these, signal levels are steady and adequately recovered at each stage,
with no sensible degradation even after a large number of restorations. This LO dis-
tribution strategy appears to be very robust, and is limited only by the maximal
operation frequency of ECL inverters available. This is, for large arrays, a frequency
much higher than that reachable with linear IF buses: the combination of analog
and digital design for IF and LO distributions allows faster RF output signals and
larger array sizes than those achievable with analog-only design approaches.

3. Conclusion

While modern Si-based RF technologies allow integration of mm-wave transceivers,
the integration of large arrays is difficult using IC architectures previously reported.
We propose a mixed-signal row/column architecture, which bases its operation on
the imposition of vertical and horizontal phase gradients. This greatly simplifies the
array internal wiring, and reduces the system design to the design of adequate IF
and LO buses. For the design of these two crucial subsystems, we propose a mixed
signal approach. Given an adequate frequency plan, the robustness of digital design
can be exploited for high-frequency non-linear LO signals, while linear analog design
is necessary only for lower-frequency IF buses. The maximal output frequency and
array size depends strongly on the application and available technology. We have
presented preliminary simulations, based on libraries and technical data of an RF
BiCMOS 0.18 μm commercial technology, which show that arrays larger than 12×12
are feasible in the $40 - 60$ GHz range.

References

1. R. Olsen, D. Rogers, and D. Hodge, "The aR^b relation in the calculation of rain attenuation," *Antennas and Propagation, IEEE Transactions on [legacy, pre - 1988]*, vol. 26, no. 2, pp. 318–329, 1978, 0096-1973.
2. A. Hajimiri, H. Hashemi, A. Natarajan, G. Xiang, and A. Komijani, "Integrated Phased Array Systems in Silicon," *Proceedings of the IEEE*, vol. 93, no. 9, pp. 1637–1655, 2005, 0018-9219.
3. A. Natarajan, A. Komijani, X. Guan, A. Babakhani, Y. Wang, and A. Hajimiri, "A 77GHz Phased-Array Transmitter with Local LO-Path Phase-Shifting in Silicon," in *IEEE International Solid-State Circuits Conference*, 2006, pp. 182–183.