CURRENT DENSITY LIMITS IN INP DHBTS: COLLECTOR CURRENT SPREADING AND EFFECTIVE ELECTRON VELOCITY

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Abstract

To minimize the dominant delay term in emitter-coupled logic, $\Delta V_{logic}C_{cb}/I_c$, HBTs must operate at high current densities [1]. Current density is limited by device thermal failure and by the Kirk effect. We here experimentally determine two key factors influencing the Kirk-effect limit. The collector current spreads laterally away from each side the emitter stripe over a distance Δ approximately equal to the collector depletion thickness. This effect substantially increases the achievable current in submicron-emitter HBTs. Further, the variation of the Kirk-effect-limited current density with bias voltage indicates a $3.2(10^5)$ m/s effective collector electron velocity, consistent with that extracted from the measured transistor f_τ.

I. Introduction

In developing InP HBTs for ~150-200 GHz logic operation, it is critical to minimize the collector capacitance charging time $\Delta V_{logic}C_{cb}/I_c$ [1]. This requires very high current density operation, and the maximum current density is set by the Kirk limit and by device heating. An analysis of the Kirk-effect-limited maximum current density show it scales inversely proportional to the square of the collector thickness, while the collector capacitance increases in proportion to the collector thickness [1]. Thinning the collector thus proportionally reduces the capacitance charging time but requires high current density. In the collector at high current densities, the injected electron charge induced field opposes the field induced by the collector doping and by the collector applied and built-in potentials [2-12]. At high current densities field reversal causes the base region to extend into the base and the collector transit time to increase; this is the Kirk effect. Understanding of the Kirk effect is particularly important in design of high speed HBTs for fast digital circuits.

II. Theory

As the current density in the collector of a HBT is increased eventually a critical current density is reached - the Kirk current density. The Kirk effect arises when the electric field at the base-collector interface becomes zero [2,5]. In SHBTs, further increases in current density force the base to extend into the collector, degrading f_τ and increasing C_{cb}, while in DHBTs an additional electron barrier is induced at the base-collector interface [4], again degrading f_τ as well as gain.

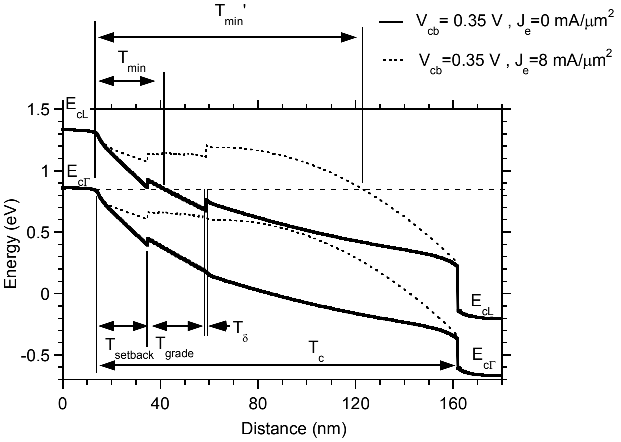

Figure 1: Γ (solid) and L (dotted) conduction bands for a 150-nm collector InP DHBT at zero current density and at a current density corresponding to the Kirk current density (J_e of 0 and 8 mA/μm^2). The dotted horizontal line show the conduction band level at the end of the base and indicate the position (T_{min} and T_{min}') where Γ-L scattering is possible. Note that the valence band is not shown.

Ishibashi [7-8] showed that the effective electron collector velocity v_{eff} is dominated by the local electron velocity next to the base. Figure 1 illustrates the Γ and L conduction bands at zero and at high (8 mA/μm^2) current density. The injected electron charge changes the band structure, moving the position where Γ-L scattering can occur (T_{min} and T_{min}') further away from the base-collector interface.

Transistor f_τ is often enhanced at currents immediately below J_{Kirk}, where the effective electron velocity v_{eff} is increased due to the increased distance an electron must travel before it can undergo *Γ-L* scattering [8].

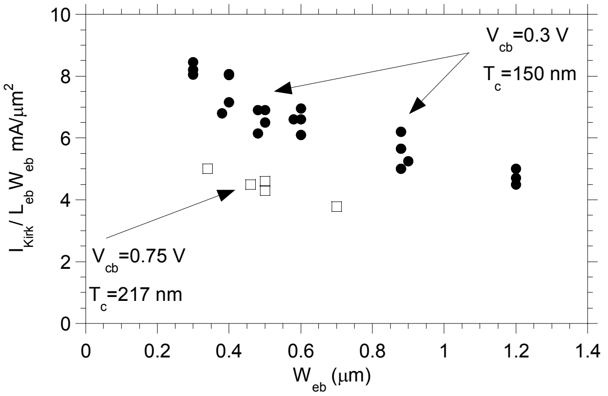

Figure 2: Kirk current density threshold from f_τ and C_{cb} measurements for transistors with 150 and 217 nm thick collectors, plotted against base-emitter junction width. V_{cb} was held constant.

In addition to the expected variation with T_C, we observe (fig. 2) a very large (1.6:1) variation in the apparent Kirk-effect threshold as the emitter-base junction width W_{eb} is decreased from 1.2 µm to 0.3 µm. This effect arises because the collector current spreads laterally away from each side of the emitter stripe over a distance Δ [9-10], increasing the area of the current flux in the collector. The Kirk-effect limit is then modified as:

$$I_{Kirk} = J_{Kirk} L_e [W_{eb} + 2\Delta] =$$

$$= v_{eff}\left[\begin{matrix} \dfrac{2\varepsilon(V_{cb} + \Phi_{bi} - \Delta V_b)}{qT_c^2} + qN_C - \dfrac{\varepsilon \Delta E_c}{q}\left(\dfrac{2T_c - 2T_{set} - T_{grade}}{T_c^2 T_{grade}}\right) \\ + 2qT_\delta (N_\delta - N_c)\left(\dfrac{T_c - T_{set} - T_{grade} - T_\delta / 2}{T_c^2}\right) \end{matrix}\right] L_e [W_{eb} + 2\Delta] \qquad [1]$$

where L_e is the emitter junction length, V_{cb} is the applied base-collector bias, Φ_{bi} the junction built-in potential. ΔV_b is the potential drop emerging from the rapid drop in doping at the base interface (and is on the order of 0.1-0.2 V). ΔE_c is the InGaAs-InP conduction band offset. T_c, T_{set}, and T_{grade} are the thickness of the collector, setback and grade layers respectively (Table 1). N_δ and T_δ are the doping and thickness of the delta-doping layer after the grade, chosen to offset the electric field in the grade [6,12].The terms associated with the conduction band offset, the grade, and the δ-doping in eq. 1 cancel each other almost completely with the correct choice of grade thickness and doping.

The collector doping N_C is selected to force full collector depletion at zero volts V_{cb}, resulting in low base-collector capacitance, C_{cb}, important in low-voltage ECL logic circuits.

With emitter junction lengths of 7.5 µm and widths of 0.3-1.2 µm, the current spreading can be modeled as one-dimensional, with current spreading Δ on either side of the emitter. A plot (fig. 3) of the Kirk current over emitter width, $I_{kirk} / L_e = J_{kirk}(W_{eb} + 2\Delta)$, versus emitter junction width W_{eb} allows determination of the spreading distance Δ and the intrinsic Kirk current density in the absence of current spreading (eq. 1). The variation of intrinsic current density J_{Kirk} with applied bias then allows determination of the effective electron velocity (fig. 4), as $dJ_{Kirk}/dV_{cb} = 2\varepsilon v_{eff}/qT_c^2$, if one assumes that the variation of effective electron velocity v_{eff} and the current spreading term Δ change slowly with applied bias, under bias conditions corresponding to the Kirk threshold [2,11]. The accuracy of these assumptions will be discussed later.

Table 1: Summary of DHBT-19 with 150 nm collector

Thickness (nm)	**Material**	**Doping (cm^{-3})**	**Description**
40	$In_{0.53}Ga_{0.47}As$	$3 \cdot 10^{19}$: Si	Emitter Cap
80	InP	$3 \cdot 10^{19}$: Si	Emitter
10	InP	$8 \cdot 10^{17}$: Si	Emitter
30	InP	$3 \cdot 10^{17}$: Si	Emitter
30	$In_{0.53}Ga_{0.47}As$	$8\text{-}5 \cdot 10^{19}$: C	Base
20	$In_{0.53}Ga_{0.47}As$	$3 \cdot 10^{16}$: Si	Setback
24	InGaAs/ InAlAs SL	$3 \cdot 10^{16}$: Si	Grade
3	InP	$3 \cdot 10^{18}$: Si	Delta doping
100	InP	$3 \cdot 10^{16}$: Si	Collector
10	InP	$1 \cdot 10^{19}$: Si	Sub Collector
12.5	$In_{0.53}Ga_{0.47}As$	$2 \cdot 10^{19}$: Si	Sub Collector
300	InP	$2 \cdot 10^{19}$: Si	Sub Collector
Substrate	SI : InP		

III. Experiment and Measurements

The HBTs in this study had 25 or 30 nm thick bases, carbon doped at $4 \cdot 10^{19}$ cm^{-3} or higher [13-14]. The InP collector have 150 or 217 nm total thickness, including a 20 nm InGaAs setback layer and a 20 nm InGaAlAs super lattice base-collector grade (Table 1). Four wafers had a 150 nm collector (N_c=$3 \cdot 10^{16}$ cm^{-3}) and three a 217 nm collector (N_c=$2 \cdot 10^{16}$ cm^{-3}). The devices were processed in an all-wet-etch mesa process [14]. The DC gain was 15-25. The 150 nm collector devices show 369 GHz peak f_τ and 460 GHz $f_{\max}$ [14] while the 217 nm collector devices show 282 GHz peak f_τ and $f_{\max}$ > 400 GHz [13]. J_{Kirk} (fig. 2) was extracted from the point of 5 % degradation in either f_τ or C_{cb}, with C_{cb} determined from 5-40 GHz Y-parameter measurements. As the devices reach the Kirk current threshold the increased base-collector transit time will decrease f_τ, and the displacement of holes into the setback layer and grade will increase C_{cb}.

The per-side lateral current spreading distance Δ was extracted to be 140 nm for a 150 nm thick collector and 190 nm for a 217 nm thick collector, extracted at a constant base-collector bias V_{cb} (fig. 3).

By applying the spreading term Δ to eq. 1 we obtain the Kirk current density in the absence of current spreading. The current spreading provides a significant increase in effective Kirk current density for HBTs with emitter width close to Δ.

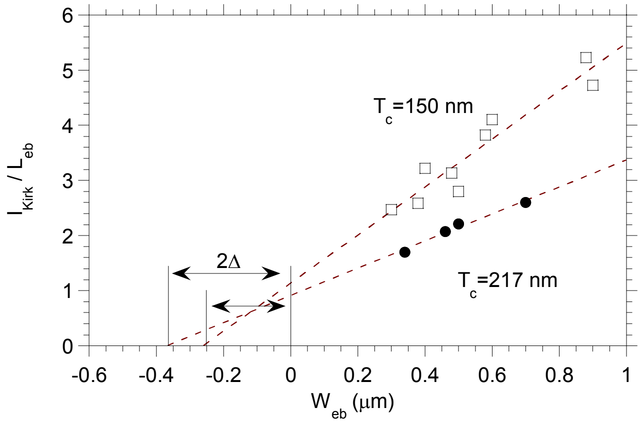

Figure 3: The measured Kirk current threshold plotted against emitter-base junction width, with V_{cb}=0.3 V for HBTs with 150 nm thick collector, and V_{cb} = 0.75 V for HBTs with 217 nm thick collector. A current spreading distance Δ of 140 respectively 190 nm is obtained.

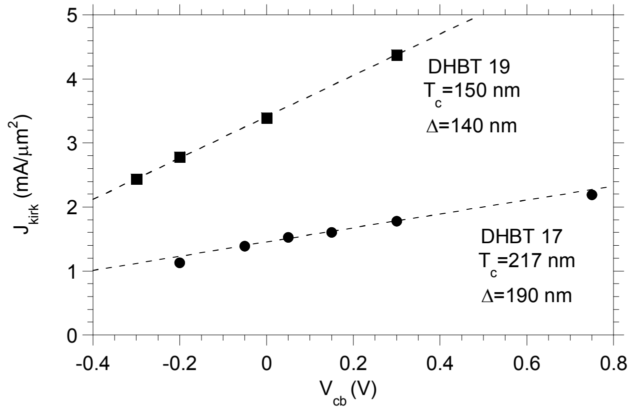

Figure 4: The current spreading corrected Kirk current threshold plotted against base—collector bias. The slope is proportional to the collector electron velocity. The linearity indicates v_{eff} is constant over this range of V_{cb}.

From the variation of J_{Kirk} with V_{cb} an effective collector velocity of $3.2\cdot 10^5$ m/s is extracted (fig. 4). Over a lager data set, we find $v_{eff} = (3.2 \pm 0.7)\cdot 10^5$ m/s for all DHBTs studied[1]. The effective collector velocity is in close agreement with the value $3.3\cdot 10^5$ m/s, determined from S-parameter device model extraction [14].

V. Discussion

It can be expected that the current spreading distance Δ as well as the effective electron velocity v_{eff} show variation with V_{cb} [3,7-8]. However, no such evidence is found in fig. 4, as the relation of J_{kirk} with V_{cb} is linear [11]. The effective electron velocity has been shown to be dominated by the local electron velocity close to the base [7]. It has been observed that increased base-collector bias voltage V_{cb} leads to increased Γ-L scattering and thus to a lower effective electron velocity. The observation that v_{eff} is constant with regards to V_{cb} is not in contradiction with these observations by Ishibashi *et al* [7-8] regarding effective electron velocity. Referring to fig. 1, at conditions close to the Kirk current density threshold, the region where Γ-L scattering can take place (T_{min}') is far removed from the base-collector interface and can be expected to have a reduced impact on the effective electron velocity; at bias conditions corresponding to the Kirk current threshold this will always be the case. At low current densities T_{min} will be much closer to the base collector junction interface (fig. 1), and subject to strong dependence on V_{cb}. Strong collector velocity modulation due to V_{cb} variation can thus be expected while biasing at low current densities. Further, note that successive points on figure 4 correspond to points of increasing V_{cb} and J_e ; increasing V_{cb} decreases v_{eff} while increasing J_e increases v_{eff} , and the overall variation of v_{eff} is thereby reduced. Our extraction of v_{eff} ignores any potential variation of current spreading distance Δ with V_{cb}. Fig. 4 indicate that the variation in Δ is proportional to the collector thickness T_c and the effective collector velocity v_{eff}.

Resistive losses in the base, subcollector as well as in the measurement set-up are small but need to be considered, since the currents are large and the bias voltages rather small ($I_c \leq 40$ mA, $V_{cb} \leq 0.75$ V). Different transistor size results in a slightly different base and collector access resistance, but the largest effect arises from the fact that maintaining the same current density for a larger device requires more current, and thus leads to a larger ohmic potential drop. The calculated difference in J_{kirk} for otherwise identical HBTs, using measured values of access resistances, is 2 % when the emitter with changes from 1.0 to 0.5 mm. We extract low base and subcollector resistances for our HBTs [13-14].

Device heating could be a factor leading to a lower apparent Kirk current density in larger HBTs, but the HBTs show the expected trend – a linear increase - with regards to J_{kirk} at higher applied bias (power) V_{bc}, with no indication of thermal degradation. The thermal resistance of these devices has been measured to be low, and this is reported elsewhere [14-16], additionally the bias voltages used here are rather low (V_{bc}<0.75 V).

VI. Conclusion

C_{cb} / I_C is a key parameter for HBTs in digital circuits. Current spreading allows a significantly higher current before the Kirk effect limits device performance. We report the first experimental determination of the amount of current spreading in InP HBTs, found to be 140 nm for a 150 nm thick collector, and 190 nm for a 217 nm thick collector. The observed current spreading sets a lower bound on the desirable emitter-collector width difference in transferred-substrate, undercut-collector, implanted-subcollector, and

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[1] $v_{eff} = (3.5 \pm 0.4)\cdot 10^5$ m/s for 150 nm collector
$v_{eff} = (2.8 \pm 0.5)\cdot 10^5$ m/s for 217 nm collector.

similar low-C_{cb} HBT designs. The effective electron velocity was measured to be $3.2 \pm 0.7 \cdot 10^5$ m/s and no indication of velocity modulation with bias was found.

Acknowledgement

The authors would like to thank Z. Griffith and V. Paidi for processing and IQE Inc. for material growth. This work was funded by ONR under N-00014-01-1-0024 and by DARPA under the TFAST program N66001-02-C-8080.

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