$In_{0.53}Ga_{0.47}As$/InP Type-I DHBTs having 455 GHz f_t and 485 GHz f_{max} w/ C_{cb}/I_c @ 0.36 ps/V

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We report InP/$In_{0.53}Ga_{0.47}As$/InP DHBTs fabricated using a conventional mesa structure, exhibiting a 455 GHz f_t and 485 GHz f_{max}, which is to our knowledge the highest simultaneous f_t and f_{max} for a mesa HBT . The collector has been scaled vertically to 120nm for reduced electron collector transit time, aggressively scaled laterally to minimize the base-collector capacitance associated with thinner collectors, and the base and emitter contact resistances r_c have been reduced. The device reported here employs a 30 nm highly doped InGaAs base and an InGaAs/InAlAs superlattice base-collector grade. Previously reported device results from our laboratory with 150nm collector had a 391 GHz f_t, 505 GHz f_{max}, and $C_{cb}/I_c \cong 0.51$ps/V operating at $J_e = 5.17$ mA/μm^2, $V_{ce} = 1.54$ V [1].

Development of digital logic and mixed-signal systems operating at higher clock speeds and bandwidth require continued improvement in transistor performance [2,3]. Projected HBT performance for 160 Gb/s systems include an f_t and $f_{max} > 440$ GHz, a breakdown voltage $V_{BR,CEO} > 3$ V, operating current density $J_e > 10$ mA/μm^2 at $V_{cb} = 0$ V, and low base-collector capacitance ($C_{cb}/I_c < 0.5$ psec/V). When designing an HBT for use in a digital IC, it should be done with emphasis on minimizing the major delay $t = C_{cb}\Delta V_{logic}/I_c$. If the device can operate at the Kirk current density $J_{Kirk} \propto T_c^{-2}$ ($\vec{E} = 0$ at the base-collector (B-C) junction) as the collector T_c is thinned, the delay $C_{cb}\Delta V_{logic}/I_c$ scales $\propto T_c$. For an InP DHBT to effectively operate at the higher J_e associated with thinner collectors, proper design and growth of the base-collector grade (Type-I DHBT) is crucial to prevent current blocking related to the conduction band discontinuity $\Delta E_c \approx 0.26$ eV between $In_{0.53}Ga_{0.47}As$ and InP--these include a chirped superlattice InGaAs / InAlAs grade with pulse doping or step-graded InGaAs / InGaAsP / InP collector. Type-II DHBTs are an alternative where no B-C grading is required because of the staggered band lineup of the GaAsSb base and InP collector, but this comes at the expense of a lower hole mobility m_p for GaAsSb. We present here a Type-I DHBT with chirped-superlattice B-C grade operating at current densities $J_e \geq 12$ mA/μm^2 at a 120nm collector scaling generation without current blocking associated with the conduction band discontinuity ΔE_c.

The epitaxial material was grown by commercial vendor IQE Inc. on a 3" SI-InP wafer and the HBTs were fabricated in an all wet etch, standard triple mesa process. An SEM image of the device is shown in figure 1 and the layer structure is provided in table 1. Details of the base and collector design are given in [4]. The devices are passivated with and the wafer is planarized in benzocyclobutene (BCB) to minimize device leakage currents associated with semiconductor surface charge effects. BCB also provides a low-loss spacer ($e_r = 2.7$, $T_{BCB} = 1.6$ μm) between the device interconnects and InP substrate to reduce spurious resonances from the RF measurements through substrate mode coupling.

Standard transmission line measurements (TLM) show the base $r_s \approx 610$ Ω and $r_c \approx 4.6$ Ω·μm^2, and the collector $r_s \approx 12.1$ Ω and $r_c \approx 8.4$ Ω·μm^2. The emitter r_c was determined from RF parameter extraction and ≈ 8.4 Ω·μm^2. The HBTs have $b \approx 40$, a common-emitter breakdown voltage $V_{BR,CEO} = 3.9$ V (at $I_c = 50$ μA), and a collector leakage current $I_{cbo} < 30$ pA (at $V_{cb,offset} = 0.3$ V). A plot of the common-emitter current-voltage and Gummel characteristics are shown in figures 2 and 3. In addition, figure 2 demonstrates the effectiveness of the chirped-superlattice base-collector grade with no evidence of current blocking until $J_e \geq 12$ mA/μm^2 at $V_{ce} = 2.0$ V. Thermal resistance q_{JA} (K/mW) and device junction temperature were measured at different V_{cb} to account for the redistribution with bias the dissipated power in the InGaAs setback, ternary grade, and InP layers. Under the following relationship, $q_{JA} = 2.6561 + 1.0878 \cdot V_{cb}$ (K/mW) when $J_e = 5.8$ mA/μm^2. These devices show little effect of self-heating until 20 mW/μm^2 and fail at 25 mW/μm^2 when biased $J_e = 10$ mA/μm^2, $V_{ce} = 2.5$ V, $\Delta T_{failure} \cong 301$ K.

DC-40 GHz RF measurements were carried out after performing an off wafer Line-Reflect-Line (LRL) calibration on an Agilent 8510C network analyzer. An on-wafer open circuit pad structure identical to the one used by the devices was measured after calibration in order to de-embed this associated capacitance from the device measurements. A maximum 455 GHz f_t and 485 GHz f_{max} (fig. 4) at $I_c = 22.5$ mA and $V_{ce} = 1.54$ V ($V_{cb} = 0.6$ V, $J_e = 8.7$ mA/μm^2, $C_{cb}/I_c = 0.36$ psec/V, $\Delta T \cong 115$ K) was determined from $|h_{21}|$ and Mason's unilateral gain |U|--extrapolated at -20 dB/dec using a single-pole fit to the small-signal hybrid-π equivalent circuit (fig. 5) for the device. This DHBT has a 0.6×4.3 μm^2 emitter semiconductor junction area A_{je} and 1.3 μm wide collector mesa--collector to emitter width ratio $W_c/W_e = 2.17$. Peak f_t and f_{max} for all devices is between $J_e = 7$-9 mA/μm^2 at $V_{cb} = 0.6$ V for different device dimensions on the wafer. Figure 6 shows the variation of C_{cb}/A_e vs operating current density J_e and V_{cb} for use in emitter coupled logic (ECL) and current mode logic (CML) circuit design.

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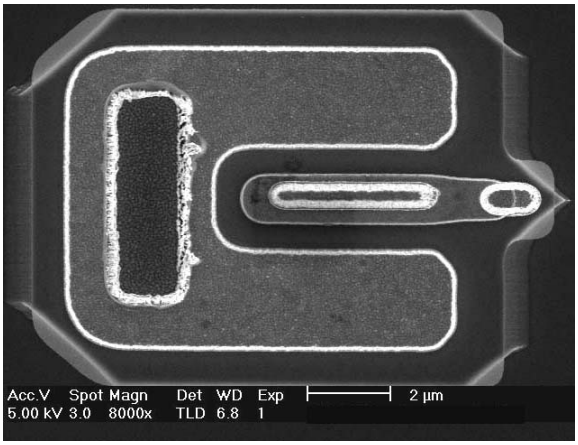


Figure 1: Top view SEM of DHBT

Table 1: DHBT layer structure

Thickness, nm	Material	Doping, cm^{-3}	Description
30	InGaAs	$7\text{-}4\cdot10^{19}$: C	Base
15	$In_{0.53}Ga_{0.47}As$	$3\cdot10^{16}$: Si	Setback
24	InGaAs / InAlAs	$3\cdot10^{16}$: Si	B-C Grade
3	InP	$3\cdot10^{18}$: Si	Pulse doping
78	InP	$3\cdot10^{16}$: Si	Collector
5	InP	$1\cdot10^{19}$: Si	Sub-Collector
6.5	$In_{0.53}Ga_{0.47}As$	$2\cdot10^{19}$: Si	Sub-Collector
300	InP	$2\cdot10^{19}$: Si	Sub-Collector
Substrate	SI : InP		

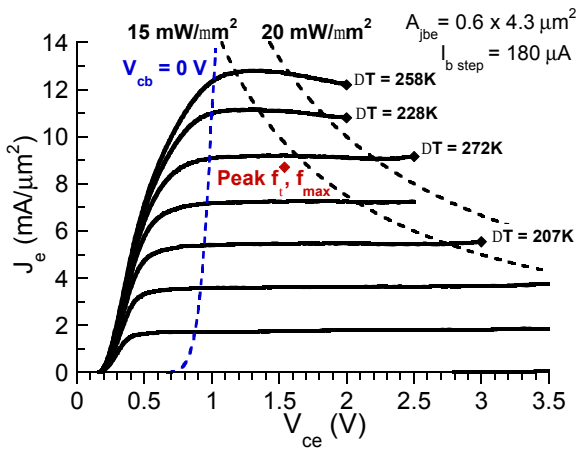


Figure 2: Common-emitter I-V characteristics

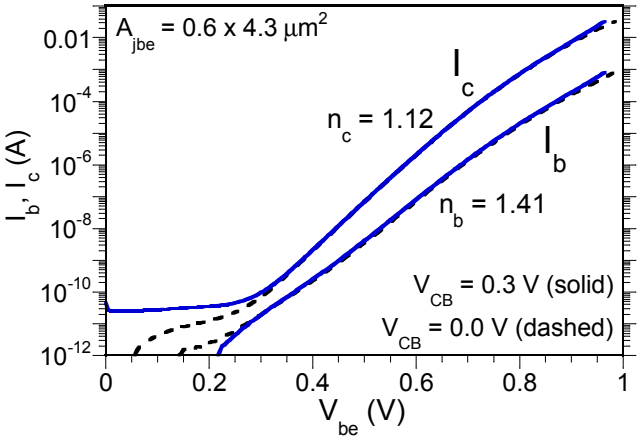
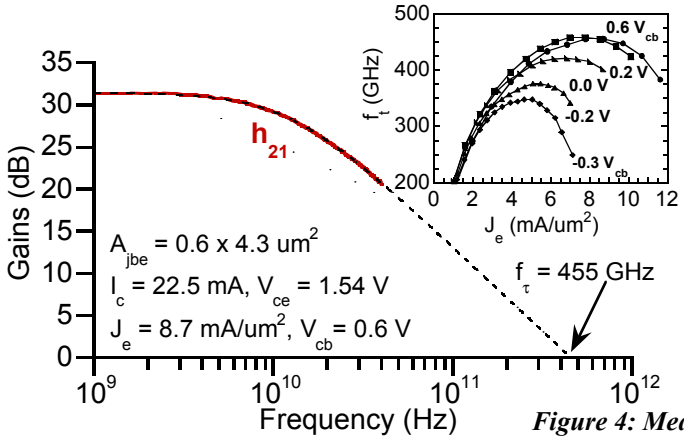


Figure 3: Gummel characteristics



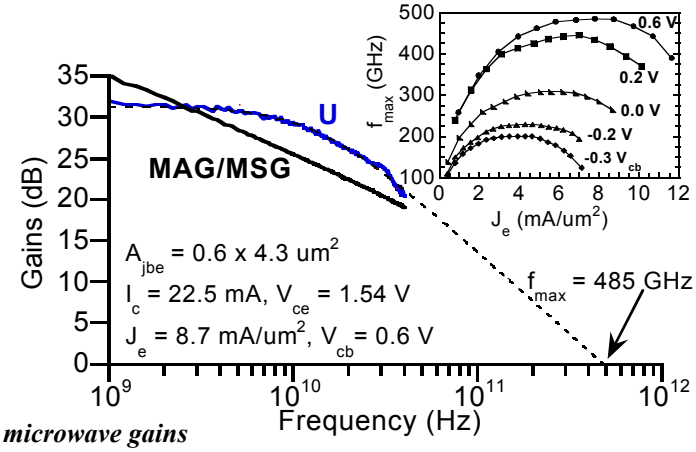


Figure 4: Measured microwave gains

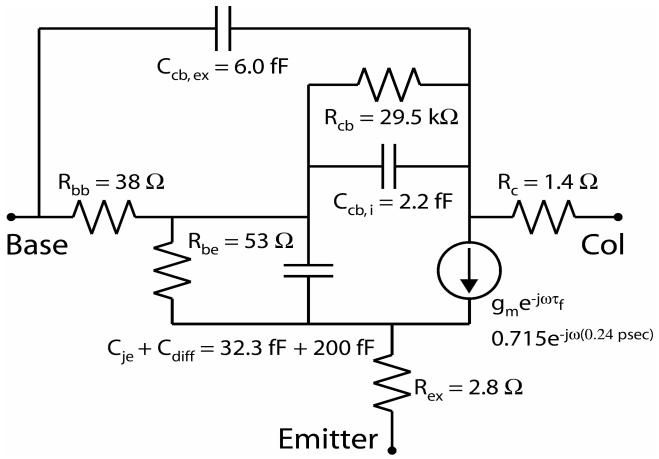


Figure 5 : Small-signal hybrid-p model

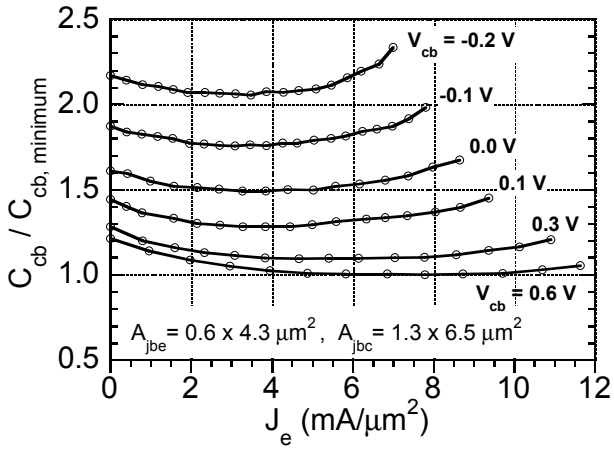


Figure 6 : C_{cb} variation with bias--$C_{cb,min}$ = 8.11 fF