InGaAs/InP DHBTs With 120-nm Collector Having Simultaneously High f_τ, $f_{\max} \geq 450$ GHz

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***Abstract*—InP/$In_{0.53}$ $Ga_{0.47}$As/InP double heterojunction bipolar transistors (DHBT) have been designed for increased bandwidth digital and analog circuits, and fabricated using a conventional mesa structure. These devices exhibit a maximum 450 GHz f_τ and 490 GHz $f_{\max}$, which is the highest simultaneous f_τ and $f_{\max}$ for any HBT. The devices have been scaled vertically for reduced electron collector transit time and aggressively scaled laterally to minimize the base–collector capacitance associated with thinner collectors. The dc current gain β is $\approx$ 40 and $V_{\mathrm{BR,CEO}} = 3.9$ V. The devices operate up to 25 mW/μm^2 dissipation (failing at $J_e = 10$ mA/μm^2, $V_{\mathrm{ce}} = 2.5$ V, $\Delta T_{\mathrm{failure}} = 301$ K) and there is no evidence of current blocking up to $J_e \geq 12$ mA/μm^2 at $V_{\mathrm{ce}} = 2.0$ V from the base–collector grade. The devices reported here employ a 30-nm highly doped InGaAs base, and a 120-nm collector containing an InGaAs/InAlAs superlattice grade at the base–collector junction.**

***Index Terms*—Heterojunction bipolar transistor (HBT), indium phosphide (InP).**

I. Introduction

InP-based double heterojunction bipolar transistors (DHBT) have been aggressively pursued because of their superior material transport properties over SiGe [1]. This is demonstrated by the increased value of small-signal unity current gain f_τ, unity power gain $f_{\max}$, and higher operating current density J_e that InP devices possess over SiGe at a given scaling generation [2], [3]. As Si based processing technologies are much more advanced than InP, SiGe HBTs have been scaled to dimensions where the reduction in base–collector capacitance C_{cb} and higher J_e are such that the speed of digital circuits in both material systems have been comparable. Over the past year, techniques to aggressively scale InP HBTs to submicrometer features vertically and laterally have resulted in record performance for f_τ and $f_{\max}$ [4]–[7]. Applications for these devices include mixed-signal ICs for digital radar and advanced communication systems [8]. Efforts to simultaneously produce submicrometer InP HBTs and have high circuit yield >10 000 devices per IC are underway, with the first step in the realization of such a process producing static frequency dividers with an operating $f_{\mathrm{clk}} > 150$ GHz[5], [9], [10].

Continued scaling of the HBT base and collector epitaxial layers is needed, along with simultaneous reductions to the device parasitics to increase the bandwidth of digital and analog circuits [11], [12]. As discussed in [3], when the collector is thinned and the operating J_e is maintained at J_{Kirk} (the electric field at the base edge of the base–collector junction becomes zero) for reduced digital IC gate delay, the major delay scales $\tau = C_{\mathrm{cb}} \cdot \Delta V_{\mathrm{logic}}/I_c \propto T_c$, the collector thickness. But as J_{Kirk} increases $\propto T_c^{-2}$, the parasitic voltage drop across the emitter resistance also increases as $\Delta V_{\mathrm{parasitic}} = I_e \cdot R_{\mathrm{ex}} \approx J_e \cdot \rho_c \propto T_c^{-2}$. If for the same circuit the bias currents $I_c = A_e \cdot J_{\mathrm{Kirk}} \propto A_e \cdot T_c^{-2}$ are kept constant as the collector is thinned and the devices scaled *and* the emitter contact resistance ρ_c is reduced $\propto T_c^2$, $\Delta V_{\mathrm{parasitic}}$ will be unchanged and circuit speed will improve.

Prior to this letter, the highest f_τ reported for an InP DHBT was 406 GHz with an $f_{\max}$ of 423 GHz [6], having a 35-nm base and 120-nm collector. The highest reported $f_{\max}$ for a mesa DHBT is 519 GHz, with a 252 GHz f_τ [7], having a 40-nm base and 150-nm collector. Here, we report a 450 GHz f_τ and 490 GHz $f_{\max}$ InP DHBT—the first transistor to have a simultaneous f_τ and $f_{\max}$ beyond 450 GHz.

II. Design, Growth, and Fabrication

The epitaxial material was grown by commercial vendor IQE, Inc. on a 3″ SI–InP wafer and the HBTs were fabricated in an all wet etch, standard triple mesa process. The device layer structure is provided in Table I and details of the base and collector design are given in [13]. The devices are passivated with and the wafer is planarized in benzocyclobutene (BCB) to minimize device leakage currents associated with semiconductor surface charge effects. BCB also provides a low-loss spacer ($\varepsilon_r = 2.7$, $T_{\mathrm{BCB}} = 1.6$ μm) between the device interconnects and InP substrate to reduce spurious resonances from the RF measurements through substrate mode coupling. The improvements in the device design here compared to [3] include the use of an indium rich $In_{0.85}$ $Ga_{0.15}$As emitter cap with increased doping $N_{\mathrm{cap}} = 6 \cdot 10^{19}$ cm^{-3} for a $\approx$ 17% reduction to the emitter contact ρ_c, and improved surface preparation to remove surface oxides (ozone plasma descum, diluted NH_4OH dip) [14] prior to base metal evaporation for a 2:1 reduction in base contact ρ_c.

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TABLE I
DHBT LAYER COMPOSITION

Thickness (nm)	Material	Doping cm^{-3}	Description
5	$In_{0.85}Ga_{0.15}As$	$6{\cdot}10^{19}$: Si	Emitter cap
15	$In_xGa_{1-x}As$	$>4{\cdot}10^{19}$: Si	Emitter cap grading
20	$In_{0.53}Ga_{0.47}As$	$4{\cdot}10^{19}$: Si	Emitter
80	InP	$3{\cdot}10^{19}$: Si	Emitter
10	InP	$8{\cdot}10^{17}$: Si	Emitter
40	InP	$5{\cdot}10^{17}$: Si	Emitter
30	InGaAs	7-4 10^{19} : C	Base
15	$In_{0.53}Ga_{0.47}As$	$3{\cdot}10^{16}$: Si	Setback
24	InGaAs / InAlAs	$3{\cdot}10^{16}$: Si	B-C Grade
3	InP	$3{\cdot}10^{18}$: Si	Pulse doping
78	InP	$3{\cdot}10^{16}$: Si	Collector
5	InP	$1{\cdot}10^{19}$: Si	Sub Collector
6.5	$In_{0.53}Ga_{0.47}As$	$2{\cdot}10^{19}$: Si	Sub Collector
300	InP	$2{\cdot}10^{19}$: Si	Sub Collector
Substrate	SI : InP		

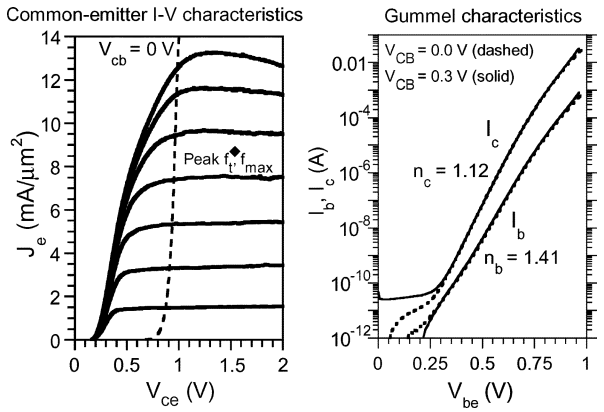

Fig. 1. Common–emitter *I–V* characteristics ($I_{b,\mathrm{step}} = 140\ \mu$A) and Gummel characteristics. Device junction dimensions $A_{\mathrm{je}} = 0.6 \times 4.3\ \mu\mathrm{m}^2$, $A_{\mathrm{jc}} = 1.3 \times 6.5\ \mu\mathrm{m}^2$.

III. RESULTS

Standard transmission line measurements (TLM) show the base $\rho_s \approx 610\ \Omega$ and $\rho_c \approx 4.6\ \Omega \cdot \mu\mathrm{m}^2$, and the collector $\rho_s \approx 12.1\ \Omega$ and $\rho_c \approx 8.4\ \Omega \cdot \mu\mathrm{m}^2$. The emitter ρ_c was determined from RF parameter extraction and $\approx 8.4\ \Omega \cdot \mu\mathrm{m}^2$. The HBTs have $\beta \approx 40$, a common-emitter breakdown voltage $V_{\mathrm{BR,CEO}} = 3.9$ V (at $I_c = 50\ \mu$A), and a collector leakage current $I_{\mathrm{cbo}} < 30$ pA ($V_{\mathrm{cb,offset}} = 0.3$ V). A plot of the common–emitter current–voltage and Gummel characteristics are shown in Fig. 1. These devices show little effect of self-heating until 20 mW/μm^2 operation and function up to 25 mW/μm^2 when biased at $J_e = 10$ mA/μm^2, $V_{\mathrm{ce}} = 2.5$ V, $\Delta T_{\mathrm{failure}} \approx 301$ K. In addition, Fig. 1 demonstrates the effectiveness of the chirped-superlattice base–collector grade with no evidence of current blocking associated with the ΔE_c between $In_{0.53}Ga_{0.43}As$ and InP until $J_e \geq 12$ mA/μm^2 at $V_{\mathrm{ce}} = 2.0$V—well beyond the bias needed for peak f_τ, $f_{\max}$ and minimum C_{cb} measured for these DHBTs.

DC-110 GHz RF measurements were carried out after performing an off wafer line-reflect-reflect-match calibration on an Agilent 8510XF network analyzer. On-wafer open and short circuit pad structures identical to the ones used by the devices were measured after calibration in order to deembed their associated

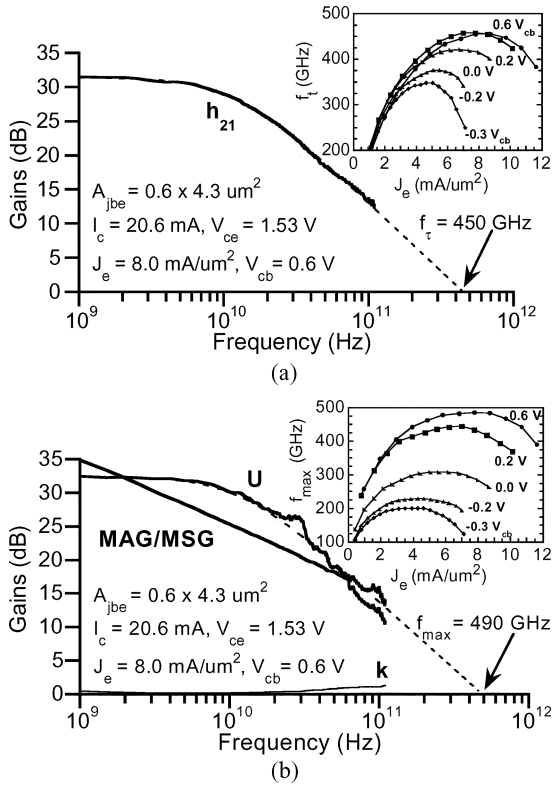

Fig. 2. Measured microwave gains. (a) h_{21} from peak extrapolated f_τ (b) MSG/MAG and Mason's unilateral power gain U from peak extrapolated $f_{\max}$.

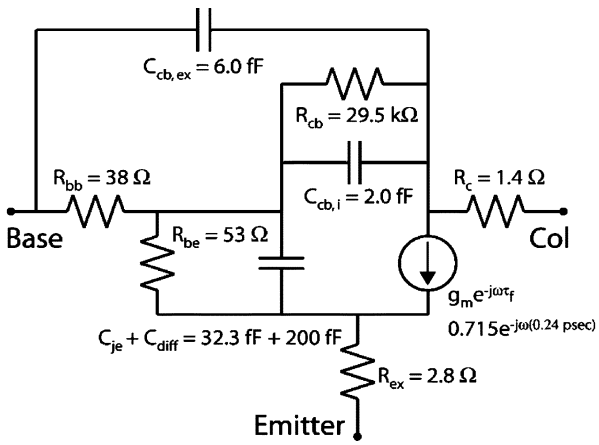

Fig. 3. Small signal *hybrid-*π equivalent circuit model.

parasitics from the device measurements. A maximum 450 GHz f_τ and 490 GHz $f_{\max}$ (Fig. 2) at $I_c = 20.6$ mA and $V_{\mathrm{ce}} = 1.53$ V ($V_{\mathrm{cb}} = 0.6$ V, $J_e = 8.0$ mA/μm^2, $C_{\mathrm{cb}}/I_c = 0.38$ ps/V, $\Delta T \cong 106$ K) was determined from extrapolation through a least-square-fit between the transfer functions

$$|h_{21}(f)|^2 = \frac{h_{21,\mathrm{DC}}^2}{1 + h_{21,\mathrm{DC}}^2 \cdot \left(\frac{f}{f_\tau}\right)^2} \tag{1}$$

$$U(f) = \frac{U_{\mathrm{DC}}}{1 + U_{\mathrm{DC}} \cdot \left(\frac{f}{f_{\max}}\right)^2} \tag{2}$$

to the measured microwave gains h_{21} and U at measured frequencies. A small-signal hybrid-π equivalent circuit for this

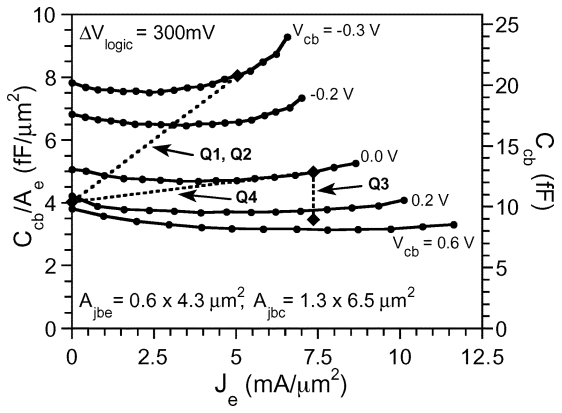

Fig. 4. Variation of $C_{\rm cb}$ with J_e and $V_{\rm cb}$ bias, labeled to show the corresponding device switching endpoints within the CML divider schematic (Fig. 5). Lines connecting the switching endpoints have been superimposed to act as a guide.

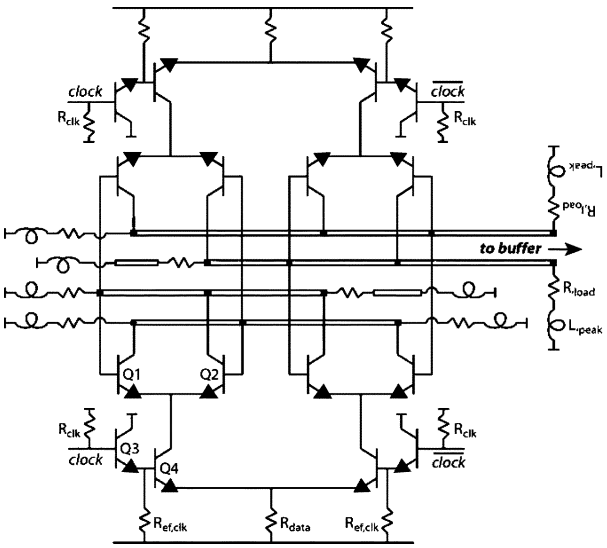

Fig. 5. Schematic of current mode logic (CML) static frequency divider.

device at peak f_τ and $f_{\rm max}$ is shown in Fig. 3. This DHBT has a $0.6 \times 4.3\ \mu{\rm m}^2$ emitter semiconductor junction area $A_{\rm jbe}$ and 1.3-μm base mesa width—collector to emitter width ratio ${\rm W}_c/\ {\rm W}_e = 2.17$. Peak f_τ and $f_{\rm max}$ for all devices is between $J_e = 7 - 9\ {\rm mA}/\mu{\rm m}^2$ at $V_{\rm cb} = 0.6$ V for different device dimensions on the wafer.

The variation of $C_{\rm cb}$ versus J_e and $V_{\rm cb}$ for use in current mode logic (CML) circuit design is shown in Fig. 4, where switching endpoints for devices from the CML static frequency divider (Fig. 5) are shown. Lines connecting the switching endpoints have been superimposed to act as a guide. At the indicated bias points, data steering devices (Q1, Q2) have a minimum $C_{\rm cb}/I_c \approx 1.6$ ps/V, emitter follower devices (Q3) $C_{\rm cb}/I_c \approx 0.57$ ps/V, and clock steering devices (Q4) $C_{\rm cb}/I_c \approx 0.67$ ps/V [12]. Some of the bias points have been selected beyond J_{Kirk} for reduced $C_{\rm cb}/I_c$ ratio. While $C_{\rm cb}$ may be increasing, inspection of the microwave gains versus J_e and $V_{\rm cb}$ (Fig. 3) shows that the initial rolloff of f_τ and $f_{\rm max}$ is soft—this suggests that the initial field collapse in the setback layer of the base–collector interface does not significantly impact the forward delay of the HBT. Because of this, the selection of a smaller device size for a J_e slightly above J_{Kirk} will translate to a higher maximum clock rate. At J_e substantially above J_{Kirk}, the field will reverse in the collector setback and grade. The forward delay will increase rapidly—this is when the roll-off of both f_τ and $f_{\rm max}$ becomes significant, and digital circuit speed will suffer.

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