$In_{0.53}Ga_{0.47}As$/InP TYPE-I DHBTs w/ 100 nm COLLECTOR AND 491GHz f , 415 GHZ f_{max}

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Abstract

$In_{0.53}Ga_{0.47}As$/InP double heterojunction bipolar transistors (Type-I DHBT) have been designed and fabricated having 100 nm drift collector and 30 nm highly doped base. The DHBTs have been scaled vertically for reduced electron transit time and aggressively scaled laterally to minimize the base-collector capacitance C_{cb} associated with thinner collectors. Devices employing a proven effective InGaAs/InAlAs superlattice base-collector grade (42 nm transition) exhibit a 491 GHz f and 415 GHz f_{max} and show no signs of current blocking until $P > 20$ mW/μm^2 due to device self-heating. We also report devices of the same layer structure where the base-collector transition has been thinned to 25 nm exhibiting a 465 GHz f and 416 GHz f_{max} and show no signs of current blocking until $J_e > 9$ mA/μm^2 at 2.0 V_{ce} associated with the base-collector grade. For both, the DC current gain > 40, $V_{BR,CEO} = 3.1$ V, and similar ideality factors n_c, n_b.

I. Introduction

Development of digital logic and mixed-signal systems operating at higher clock speeds and bandwidth require continued improvement in transistor performance [1]. Projected HBT performance for 160 Gb/s systems include an f and f_{max} > 440 GHz, a breakdown voltage $V_{BR,CEO} > 3$ V, operating current density $J_e > 10$ mA/μm^2 at $V_{cb} = 0$ V, and low base-collector capacitance ($C_{cb}/I_c < 0.5$ psec/V) [2]. When designing an HBT for use in a digital IC, it should be done with emphasis on minimizing the major delay terms associated with $= C_{cb}$ V_{logic}/I_c. If the device can operate at the Kirk threshold current density J_{Kirk} T_c^{-2} (electric field at the base-collector junction is zero) as the collector thickness T_c is reduced, the delay C_{cb} V_{logic}/I_c scales T_c. In order for an InP DHBT to effectively operate at the high current densities associated with thinner collectors, proper design and growth of the base-collector grade (Type-I DHBT) is crucial to prevent current blocking related to the conduction band discontinuity E_c 0.26 eV between $In_{0.53}Ga_{0.47}As$ and InP--these include a chirped superlattice InGaAs / InAlAs grade with pulse doping [3,4] or step-graded InGaAs / InGaAsP / InP collector [5]. Type-II DHBTs are an alternative where no base-collector grading is required because of the staggered band lineup of the GaAsSb base and InP collector [6], but this comes at the expense of a lower hole mobility $_p$ for GaAsSb [7]. We present here experimental evidence that with proper design and growth, a Type-I DHBT with chirped superlattice base-collector grade can operate at current densities J_e > 16 mA/μm^2 at a 100 nm collector scaling generation without current blocking associated with the conduction band discontinuity E_c.

II. Design

For Type-I DHBTs to operate effectively at high J_e, the conduction band discontinuity between InGaAs and InP must be removed. Previous DHBT designs from our laboratory have employed a 47 nm transition region (20 nm setback / launcher,

Table 1: DHBT layer structures, 42 / 25 nm transitions

Thickness, nm	Material	Doping, cm^{-3}	Description
30	InGaAs	7-4 10^{19} : C	Base
15 / 10	$In_{0.53}Ga_{0.47}As$	9 10^{16} : Si	Setback
24 / 12	InGaAs / InAlAs	9 10^{16} : Si	B-C Grade
3	InP	. 10^{18} : Si	Pulse doping
58 / 75	InP	9 10^{16} : Si	Collector
10	InP	1.5 10^{19} : Si	Sub-Collector
8.5	$In_{0.53}Ga_{0.47}As$	2 10^{19} : Si	Sub-Collector
300	InP	2 10^{19} : Si	Sub-Collector
Substrate	SI : InP		

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Table 2: Summary of device characteristics

Transition	Peak	$V_{BR,CEO}$	c,emitter Ω-μm²	s, base	c, base Ω-μm²	s, col	c, col Ω-μm²	n_b	n_c	T,peak f , f_{max}	Peak f	Peak f_{max}
42 nm	41	3.1	7.8	629	6.2	12.9	4.0	1.44	1.12	105 K	491	415
25 nm	47	3.1	10.4	616	3.8	13.3	5.8	1.51	1.11	111 K	465	416

24 nm grade, 3 nm pulse doping) between the base and InP portion of the collector--this proved effective and device and circuit results for such have been previously reported [4,8,9]. As T_c is scaled, the ternary materials associated with the setback and grade occupy a greater portion of the collector and the device operating temperature will increase rapidly at moderate base-collector voltages V_{cb} [10]. There are two approaches to reduce them from the collector.

The conduction-band potential drop across the setback layer associated with launching electrons into the grade is [4]:

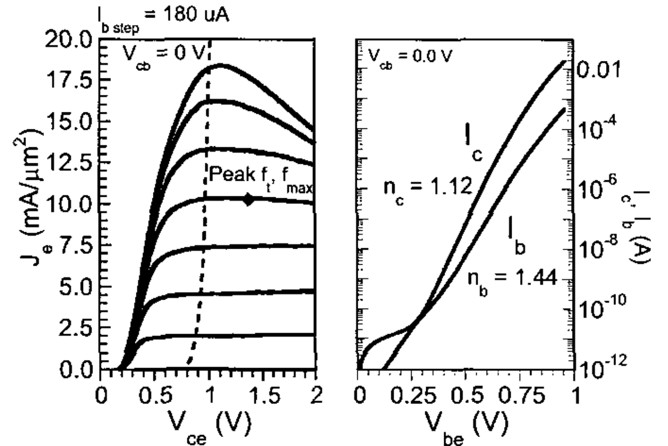
$$_{setback} \quad (V_{cb} \quad _{bi}) \frac{T_{setback}}{T_c} \quad \frac{qN \; T \; T_{setback}}{_{o \; r}} \quad \frac{(qN_c \quad J(x)/ \; _{eff}) T_c T_{setback}}{2 \; _{o \; r}} \tag{1}$$

For the device designs reported in [4,8], the 200 nm and 150 nm T_c with 20 nm $T_{setback}$ had a $_{setback}$ 0.370 and 0.378 eV, respectively. Scaling to 100 nm T_c w/ 20 nm $T_{setback}$ would give $_{setback}$ 0.442 eV. Based on the previous results and the effectiveness of the grade with the values of $_{setback}$ just listed, the setback was thinned for these 100 nm collector devices to 15 nm (42 nm transition) for $_{setback}$ 0.332 eV.

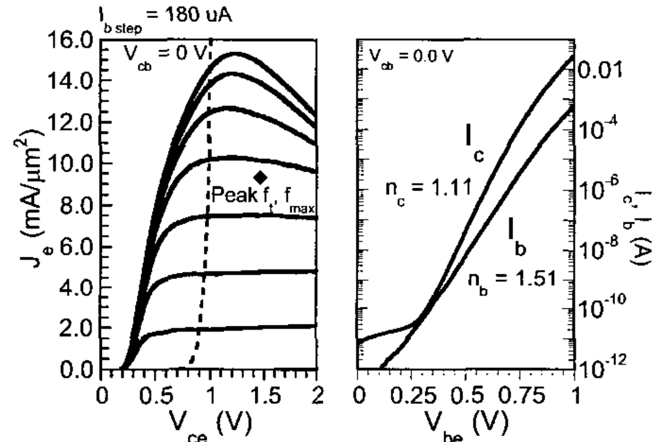
A pulse-doping is required to suppress the change in the conduction band quasi-field at the InP interface within the collector when a chirped-superlattice grade is used to remove the E_c discontinuity and is determined from the following relationship [3,4]:

$$N \; T = \frac{_{o \; r} \quad E_c}{q^2 T_{grade}} \tag{2}$$

The second device design explored employs the same layer structure and doping values as pursued for the 42 nm transition device, but the grade has been reduced by 2:1, with the pulse doping and setback adjusted (25 nm transition) to produce a $_{setback}$ 0.338 eV



(a) 42 nm transition device



(b) 25 nm transition device

Figure 1: Common emitter I-V and Gummel Characteristics Emitter junction area, A_{jbe} = 0.6 4.3 μm²

III. Growth and Fabrication

The epitaxial material was grown by commercial vendor IQE Inc. on a 3" SI-InP wafer and the HBTs were fabricated in an all wet etch, standard triple mesa process. The device layer structure is provided in table 1 and further details of the base and collector design are given in [4]. The devices are passivated with and the wafer is planarized in benzocyclobutene (BCB) to minimize device leakage currents associated with semiconductor surface charge effects. BCB also provides a low-loss spacer ($_r$ = 2.7, T_{BCB} = 1.6 μm) between the device interconnects and InP substrate to reduce spurious resonances from the RF measurements through substrate mode coupling.

IV. Measurements and Results

A summary of the device characteristics is provided in table 2. Standard transmission line measurements (TLM) were performed to extract the sheet resistance $_s$ and contact resistance $_c$ for the base and collector layers. The emitter $_c$ was determined from RF parameter extraction. DHBTs for both layer structures have a peak > 40, a common-emitter breakdown voltage $V_{BR,CEO}$ = 3.1 V (at I_c = 50 μA), and a collector leakage current I_{cbo} < 150 pA (at $V_{cb,offset}$ = 0.3 V). A plot of the common-emitter current-voltage and Gummel characteristics are shown in figure 1.

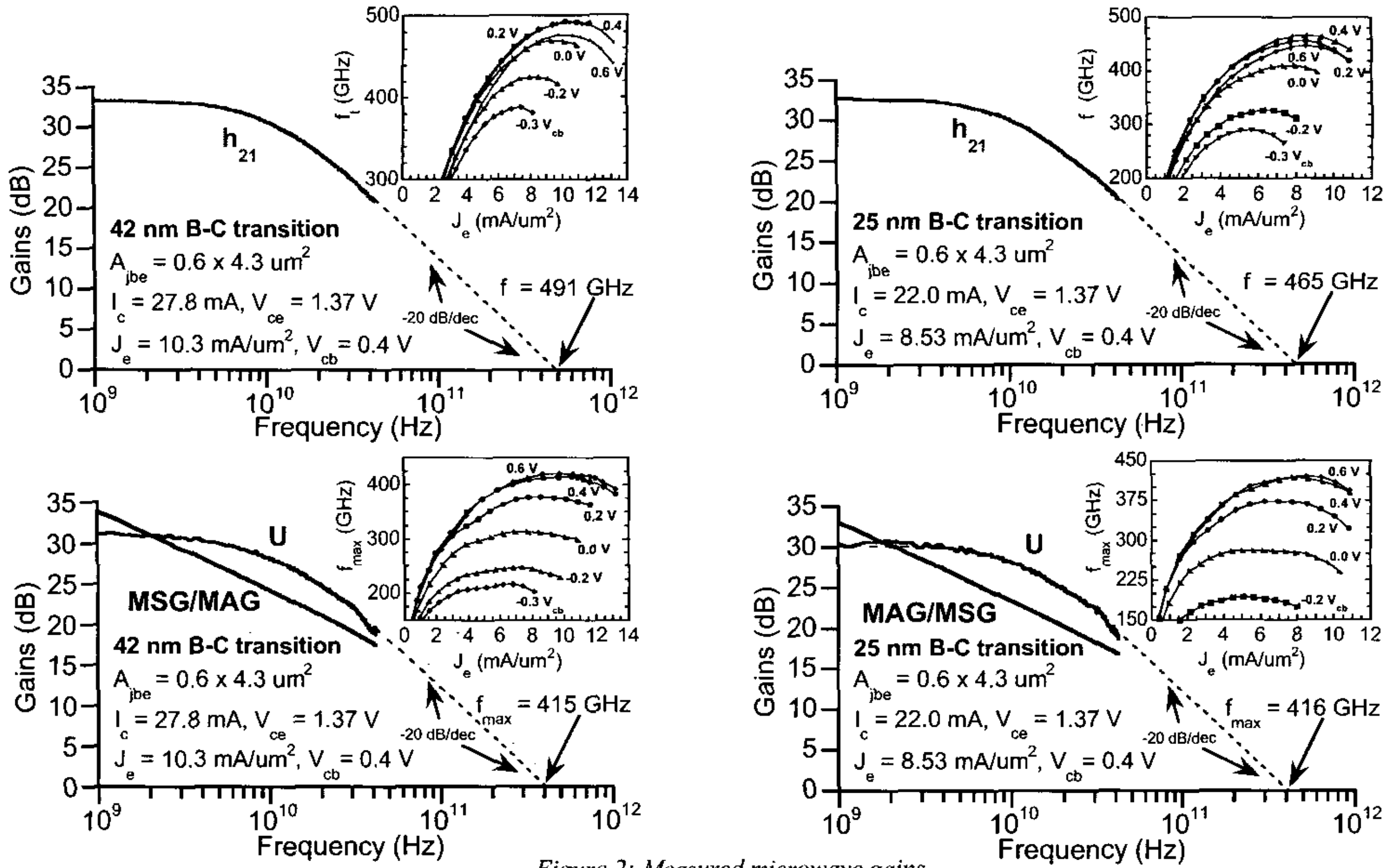


Figure 2: Measured microwave gains

DC-42 GHz RF measurements were carried out after performing an off wafer Line-Reflect-Line (LRL) calibration on an Agilent 8510C network analyzer. An on-wafer open circuit pad structure identical to the one used by the devices was measured after calibration in order to de-embed this associated capacitance from the device measurements. Peak f and f_{max} were determined from extrapolation through a least-square-fit between the transfer functions $|h_{21}(f)| = h_{21,DC} /(1 + h_{21,DC}^2 (f^2/f^2))^{1/2}$ and $|U(f)| = U_{DC}/(1 + U_{DC}^2 (f^2/f_{max}^2))^{1/2}$, to the measured microwave gains $|h_{21}|$ and $|U|$, at measured frequencies. Both DHBTs have a 0.6 4.3 μm^2 emitter s/c junction area A_{jbe} and 1.3 μm collector mesa width--collector to emitter width ratio $W_c/W_e = 2.17$. Peak f and f_{max} for all devices is between J_e = 7-11 mA/μm^2 at V_{cb} = 0.4 V for different device dimensions on the wafers.

Thermal resistance $_{JA}$ and device junction temperature were measured by the method of Liu [11] at different V_{cb} to vary the field distribution and thus power dissipation in the InGaAs setback, ternary grade, and InP layers of the collector. Because InGaAs, InAlAs, and InP have substantially different thermal resistivities, variation of $_{JA}$ with V_{cb} and J_e should be expected. Table 3 shows $_{JA}$ (from J_e = 5.8 mA/μm^2) for varying V_{cb} and the temperature rise at different bias points. Note that the change in thermal feedback coefficient, (V/K) is adjusted to account for the difference in operating current density. Also, the collector junction may be considerably hotter than the emitter junction due to the emitter interconnect metal, and the high thermal resistance of the InGaAs base.

Table 3 -- Thermal data, 42 nm transition

$_{JA}$ = 2.3613 + 0.8056 V_{cb} (K/mW) -- A_{jbe} = 0.6 4.3 μm^2		
V_{ce} (V)	J_e (mA/μm^2)	T (K)
2.5	9.61	242
2.5	7.40	179
2.0	14.49	271
2.0	13.66	253
2.0	12.36	226
1.11	18.41	153
1.37	10.30	105

Thermal data, 25 nm transition

$_{JA}$ = 2.9195 + 1.4154 V_{cb} (K/mW) – A_{jbe} = 0.6 4.3 μm^2		
V_{ce} (V)	J_e (mA/μm^2)	T (K)
2.5	8.60	304
2.5	7.12	247
2.0	14.90	386
2.0	12.33	311
2.0	10.90	272
1.23	15.30	176
1.37	8.53	111

Acknowledgement

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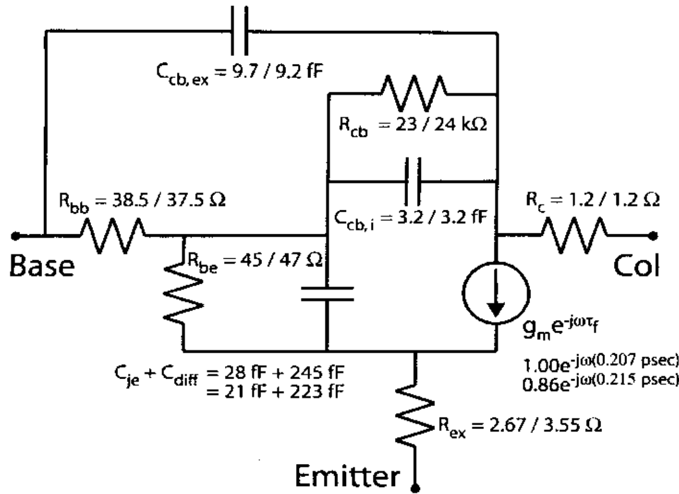

Figure 3: Hybrid-π model, 42 / 25 nm transitions

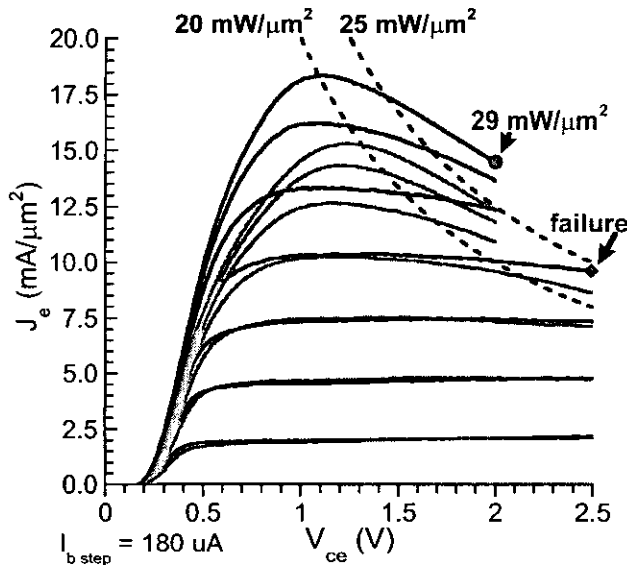

Figure 4: High power density Common-emitter curves
42 nm transition black, 25 nm transition blue

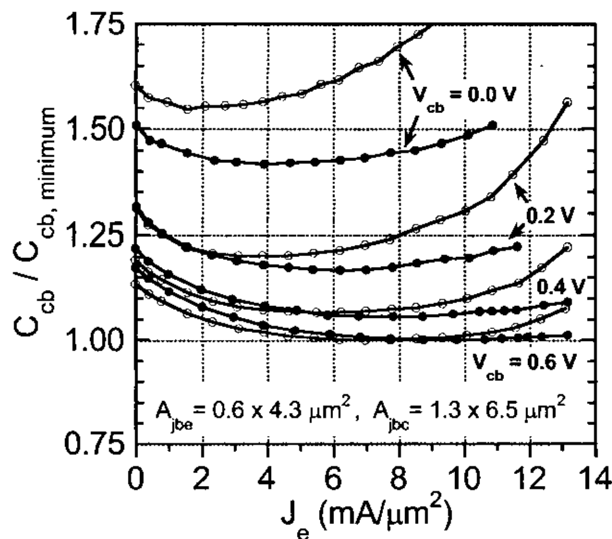

Figure 5: C_{cb} variation w/ bias
42 nm transition filled, 25 nm transition hollow

V. Discussion

Figures 3, 4 and 5 show a direct comparison of the two DHBTs. The hybrid- model shows that the devices have similar values of resistive and capacitive parasitics--thus performance disparity can be focused on the different B-C grades. The common-emitter I-V curves from figure 4 are also comparable for J_e 9 mA/μm². At higher J_e, the 25 nm transition device suffers from current blocking while the 42 nm transition device behaves normally until J_e 18 mA/μm². We are certain that current blocking is observed because of the increase in C_{cb} shown in figure 5 at higher J_e. The inability of the 25 nm transition devices to operate well at high J_e may be due to imperfect design, deviation between design and growth, or more fundamental issues regarding the design of the graded layers. Further investigation is required.

Because InP has a higher breakdown field and higher thermal conductivity than InGaAs and InAlAs, it might be expected that the 25 nm transition devices show significantly improved $V_{BR,CEO}$, $_{JA}$, or P_{max}. The data does not support these expectations. The lower $_{JA}$ of the 42 nm transition devices at high J_e J_{Kirk} is due in part to the relatively small electrostatic potential drop in the setback and grading layers of the collector.

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