n^+-InAs–InAlAs Recess Gate Technology for InAs-Channel Millimeter-Wave HFETs

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***Abstract*—We report a submicrometer, self-aligned recess gate technology for millimeter-wave InAs-channel heterostructure field effect transistors. The recess gate structure is obtained in an n^+-InAs–InAlAs double cap layer structure with a citric-acid-based etchant. From molecular-beam epitaxy-grown material functional devices with 1000-, 500-, and 200-nm gate length were fabricated. From all three device geometries we obtain drive currents of at least 500 mA/mm, gate leakage currents below 2 mA/mm, and RF-transconductance of 1 S/mm. For the 200-nm gate length device f_τ and $f_{\max}$ are 162 and 137 GHz, respectively. For the 500-nm gate length device f_τ and $f_{\max}$ are 89 and 140 GHz, respectively. We observe scaling limitations at 200-nm gate length, in particular a negative threshold voltage shift from -550 to -810 mV, increased kink-effect, and a high gate-to-drain capacitance of 0.5 pF/mm. The present limitations to device scaling are discussed.**

***Index Terms*—Antimonides, heterojunction field-effect transistor (HFET), millimeter-wave transistor, molecular-beam epitaxy.**

I. Introduction

THE III-V heterostructure field effect transistors (HFETs) are promising devices for millimeter-wave (mm-wave) applications. This has been demonstrated, for example, by an InP-based HFET with 25-nm gate length with a current gain cutoff frequency f_τ of 562 GHz and a maximum frequency of oscillation $f_{\max}$ of 330 GHz [1]. These results have been obtained with a strained $In_{0.7}Ga_{0.3}As$ channel on the InP lattice constant. For some time, it has been recognized that pure InAs channels have potential application for improved HFETs because of their high electron mobility, up to 30 000 $cm^2/V \cdot s$ [2]. Such InAs channels can be embedded into antimonide-based barrier materials at a lattice constant of approximately 6.1 Å. InAs-channel HFETs with antimonide-based barriers have been demonstrated by several groups [3]–[5], and there has been recent interest in such devices for mm-wave, low-power, low-noise amplifiers [6]–[11].

With the exception of the devices in [4] and [9], InAs-channel HFETs have not employed a recess gate technology. In other advanced III-V HFET technologies, however, recess gate technology is commonly used for multiple purposes [1], [12]: these include to simultaneously obtain low access resistance and low threshold voltage, to control the electric field between gate and drain for higher breakdown voltages or higher electron velocities, or to provide surface protection during device fabrication.

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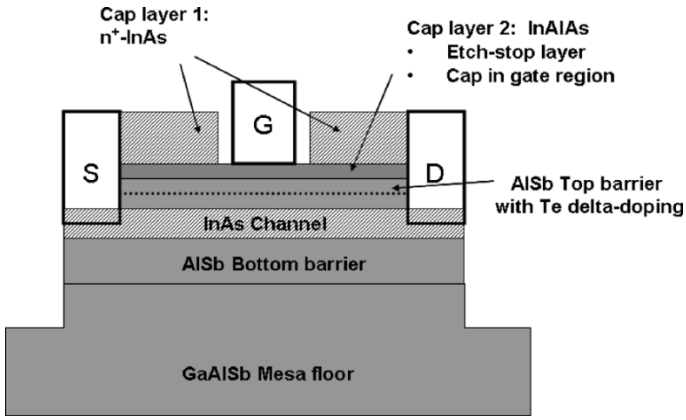

Fig. 1. Schematic device structure. The recessed gate is formed by selectively removing cap layer 1 before gate deposition.

Here we report on the development of a recess gate technology for HFETs at a lattice constant of 6.1 Å and the demonstration of mm-wave HFETs. The only other reports on recess gate technology for InAs-channel HFETs are based on a fundamentally different approach employing a thin, fully depleted InAs cap layer [4], [9]. In contrast, the recess technology presented here employs an undepleted n^+-InAs–InAlAs double cap structure.

II. Recess Gate Design

The presented recess structure is aimed at simultaneously obtaining low source resistance, R_S, and low threshold voltage, $V_{\rm th}$. In addition, the recess technology is aimed at providing surface protection. Low R_S is needed for good RF performance. Low $V_{\rm th}$ is desirable for several reasons: First, high output resistance hence high $f_{\max}$ operation of HFETs requires a pinched-off channel or $V_d > V_{\rm th} + V_g$, where V_d is the drain voltage and V_g the gate voltage. Hence, low $V_{\rm th}$ allows operation at low V_d. This results in low power dissipation, which is one of the main motivations for developing InAs-channel HFETs. In addition, low V_d operation is desirable because the maximum V_d of InAs-channel HFETs is limited by source-to-drain breakdown due to impact ionization [4], [5], [13]. Second, low $V_{\rm th}$ reduces the gate-to-drain voltage, $V_{\rm gd}$, under operation. Hence, gate-to-drain breakdown phenomena are also reduced.

Fig. 1 shows a schematic cross section of the recessed HFETs. Both $V_{\rm th}$ and R_S depend on n, the electron density in the channel: $V_{\rm th}$ is proportional to n in the gate region and R_S

TABLE I
SUMMARY OF MBE GROWTH RESULTS

Sample	Cap doping [10^{19} cm^{-3}]	Te-doping [10^{12} cm^{-2}]	Top barrier [Å]	Buffer	R(sheet) as-grown [Ω/sq.]	R(sheet) cap 1 removed [Ω/sq.]	Mobility [cm^2/Vs]	Electron Density [10^{12} cm^{-2}]
A	2.0	3.0	140	AlGaSb	83	120	22,600	2.25
B	2.0	1.0	180	AlSb	110	180	23,800	1.49
C	2.0	none	190	AlSb	130	300	25,300	0.81
D	none	none	190	AlSb	670	300	22,300	0.92

is inversely proportional to n in the source access region. In a nonrecessed HFET, n is the same in the gate region and in the access regions. Hence low $V_{\rm th}$ and low R_S lead to conflicting requirements on n in a nonrecessed HFET. The presented recess design aims at independent control of n in the access regions and in the gate region. This is achieved by using a double cap structure as shown in Fig. 1. Cap layer 1 is heavily n-type doped InAs. This layer is present in the access regions, and it is selectively removed in the gate region. Cap layer 2 is undoped strained InAlAs. This layer is the cap layer in the gate region. The position of the Fermi-level at the top interface of cap layer 2 determines n. The main objective of the recess structure is to control the Fermi-level at the top interface of cap layer 2 by the bulk doping level in cap layer 1. To achieve high n in the access regions, the Fermi-level needs to be high relative to the InAs conduction band edge. This is achieved by doping the InAs degenerately to 2×10^{19} cm^{-3}. In addition thickness and doping of cap layer 1 are chosen so high that the field in the barrier is screened from the surface Fermi-level pinning. Because of the large nonparabolicity of InAs, the effective mass cannot be considered constant [14] when calculating the Fermi level. Fig. 2 shows band diagrams in the access regions of the transistors. These were calculated with one–dimensional (1-D) Poisson, a self-consistent Poisson–Schrödinger solver [15]. The surface Fermi-level of as-grown InAs is assumed to pin 1320 meV below the conduction band edge of AlSb, $E_c(\mathrm{AlSb})$ [16]. The surface Fermi-level of InAlAs is assumed to pin 1050 meV below $E_c(\mathrm{AlSb})$ based on fitting measured electron densities. Because 1-D Poisson does not model the nonparabolicity of InAs, the cap layer doping in the input file was adjusted to 1.1×10^{19} cm^{-3} from the real value of 2.0×10^{19} cm^{-3}. The three band diagrams are for a heavily n-type doped InAs cap layer 1 (a), for an undoped InAs cap layer 1 (b), and for an air-exposed InAlAs cap layer 2 (c) at the surface. n increases monotonically with the doping in cap layer 1. For high enough doping in cap layer 1, n is higher with the n$^+$ InAs cap layer 1 than with the InAlAs cap layer 2 on the surface. In the region under the gate, n is controlled, among other facts, by the difference between the gate metal work function and the InAlAs electron affinity. To first approximation, the Fermi-level pinning is similar at the InAlAs-metal interface and the InAlAs–air interface.

In addition to modifying n, the n$^+$-InAs cap layer provides surface protection. The InAlAs layer under the gate metal is only exposed to the ambient for a short time (few minutes) during the gate process. This is desirable because InAlAs can quickly oxidize during processing. This work has concentrated on n$^+$-InAs for cap layer 1 and strained InAlAs for cap layer 2. Strained

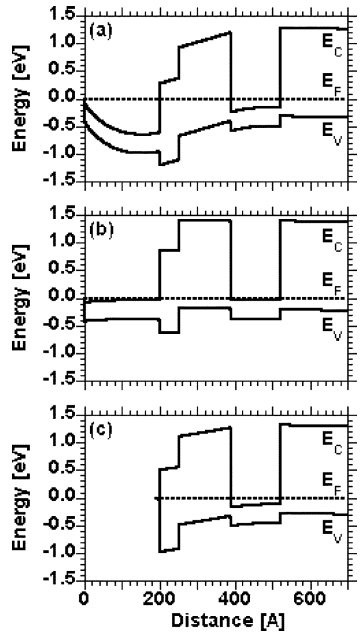

Fig. 2. Band diagrams in the access regions of the transistor. Part (a) shows data for a heavily n-type doped InAs cap layer (Sample C, as-grown). Part (b) shows data for an undoped InAs cap layer (Sample D, as-grown). Part (c) shows data for an air-exposed InAlAs surface (Samples C and D after removal of cap layer 1).

InAlAs was first introduced as a cap layer by Boos *et al.* [4] and is used successfully in other nonrecessed devices [6]–[8]. n$^+$-InAs was chosen for cap layer 1 over other materials such as GaSb because InAs can be n-type doped very heavily and it is more stable in processing than GaSb.

Experimental procedures are needed to determine n in the different regions of the HFET. In this report Hall measurements were used to measure n in the gate region as described in Section III. In the access regions, n could not be determined experimentally. Instead the sheet resistance in the access regions was determined from measurements of the S/D resistance, $R_{\rm DS}$, on HFETs as described in Section IV. Because of parallel conduction through the n$^+$-InAs cap layer, Hall measurements cannot determine n in the access regions.

III. EPITAXIAL GROWTH

All samples were grown by molecular-beam epitaxy (MBE) employing a solid-source MBE machine. The growth front was monitored by reflection high-energy electron diffraction (RHEED) and the growth temperatures were measured by a pyrometer facing the wafer. This report concerns four MBE-grown samples, samples A, B, C, and D. Their layer structure can be

seen schematically in Fig. 1. The four samples differ mainly in their doping levels, which are summarized in Table I.

The active part of the device was grown on top of a 1-μm -thick $Al_{0.80}Ga_{0.20}Sb$ or AlSb buffer layer, which was grown metamorphically on a semi-insulating 2-in GaAs wafer. The initial samples used AlSb for the buffer layer; later samples used $Al_{0.80}Ga_{0.20}Sb$ instead because it is more resistant to oxidation. Growth was initiated at 570 °C by growing a 500-Å-thick GaAs layer. Then we grew a 100-Å-thick AlAs layer followed by a 300-Å-thick AlSb layer. For the growth of the $Al_{0.80}Ga_{0.20}Sb$ buffer layer the temperature was lowered to 530 °C.

The RHEED pattern was streaky during the growth of the GaAs and AlAs layers. During the growth of the mismatched AlSb layer, the RHEED pattern initially became spotty without losing intensity. Within the first 100 Å of AlSb growth, the RHEED pattern recovered to a streaky, 1×3 reconstructed pattern. This evolution of the RHEED pattern indicates a transition from a smooth growth front to a rough growth front when nucleating the mismatched AlSb layer and a transition back to a smooth growth front within the first 100 Å of AlSb.

On top of this buffer structure, a 2000-Å-thick $Al_{0.75}Ga_{0.25}Sb$ layer was grown, which serves as a chemically stable mesa floor. Then, a 200-Å-thick AlSb back barrier, a 130-Å-thick InAs quantum well, an AlSb top barrier, a 50-Å strained $In_{0.50}Al_{0.50}As$ cap layer, and a 200-Å InAs cap layer were grown. Samples A, B, and C have Si-doped cap layers. Sample D has an undoped cap layer. Samples A and B also contain a Te delta doping sheet in the AlSb top barrier. The differences between the four samples in doping level, top barrier thickness, and the type of buffer structure are summarized in Table I.

After growth, the wafers appeared featureless to the naked eye and under an optical microscope. Room temperature Hall measurements were performed in van-der-Pauw geometry both on as-grown material and after selectively removing the top n^+-InAs layer. The results are also shown in Table I. On as-grown samples the conductivities of the n^+-InAs cap layer and of the InAs channel are measured in parallel. When the n^+-InAs cap layer has been removed, only the conductivity of the InAs channel is measured. This conductivity is the sheet resistance in the gate region of the HFETs at $V_g = 0$ mV. As discussed in Section II, the purpose of the n^+-InAs cap layer is to change the electron density in the InAs channel, n, in the access regions of the HFET. A direct measurement of the sheet resistance in only the InAs channel in the presence of the n^+-InAs cap layer is presented in Section IV. Hall measurements cannot provide this information.

After removing the n^+-InAs cap layer, the four samples have identical InAlAs surface layers. As expected, the measured sheet resistance and the measured n depend monotonically on the Te doping level. The high mobilities, above 22 000 $cm^2/V \cdot s$, indicate good material quality. After cap removal, Sample C and D have nominally identical structures, and very similar numbers are measured for both samples. As shown in Table I, the sheet resistance of Samples A, B, and C is reduced in the presence of the n^+-InAs cap layer. This difference is partly due to conduction through the n^+-InAs cap layer and partly due to the increased n in the InAs channel.

Sample D has an undoped InAs cap layer and is included as a reference. In contrast to the other three samples, Sample D has a higher sheet resistance in the presence of the InAs cap layer. Because the InAs cap layer of Sample D is undoped, conduction through the InAs cap is small. Assuming conduction in only the InAs channel, we calculate an electron density of 0.58×10^{12} cm^{-2} and an electron mobility of 16 100 $cm^2/V \cdot s$. For sample D, the electron density is lower in the presence of the InAs cap layer. This is due to different surface Fermi level pinning of InAs and InAlAs. The three band diagrams in Fig. 2 correspond to the as-grown Sample C (a), the as-grown Sample D (b), and Sample C and D after removal of cap layer 1 (c). The same phenomenon has been observed in samples with InAs and GaSb surface layers [16].

IV. Device Fabrication and Recessed Gate Technology

HFETs were fabricated in a mesa-isolated process. First, Pd–Ti–Pd–Au ohmic contacts were formed using optical lithography and electron beam evaporation [17]. In the recess process the contact resistance cannot be measured with transfer length method (TLM) patterns due to the conductive cap layer. These Pd-based ohmic contacts routinely give specific contact resistances below 10^{-6} $\Omega \cdot cm^2$ and below 0.1 $\Omega \cdot$ mm in a nonrecessed process [6]. Device mesas were defined by optical lithography. The 100-nm-high mesas were formed by first selectively removing the InAs cap layer in an aqueous solution of citric acid and hydrogen peroxide (equal parts of 1-M citric acid and 30% H_2O_2) [18] and then by dry etching in BCl_3. This was followed by another wet etch in the same solution to undercut the InAs quantum wells. To fabricate the recess gates, a self-aligned recess gate process was developed: the gates were defined by electron beam lithography in a trilayer resist stack, which consisted of 150-nm-thick 950 k PMMA, 370-nm-thick copolymer and 120-nm-thick 50 k PMMA. After development, wet-chemical etching in the same citric acid-based etchant was performed for 30 s to form the recess structure. This etchant selectively removes the n-InAs layer. After etching through the n-InAs layer, the etch proceeds to undercut the resist laterally. In separate etch experiments, we have observed identical lateral and vertical etch rates of 90 nm/min. After the recess etch, Ti–Pd–Au was deposited by electron beam evaporation and T-shaped gates were formed by lift-off. Fig. 3 shows a scanning electron microscope (SEM) image of a cleaved cross section through a gate fabricated in this process. The gate length is 290 nm with symmetric, 50-nm-long recessed regions. In this process, the amount of lateral etching, and hence the recess length, is limited to 50 nm by degradation of the InAs channel after long etch times. The maximum acceptable etch time was determined in separate experiments on Hall samples in van-der-Pauw geometry. On these samples an increase of the electron density from 1.5×10^{12} cm^{-2} to 4.0×10^{12} cm^{-2} and a reduction of the electron mobility from 25 000 to 10 000 $cm^2/V \cdot s$ was observed for etch times exceeding 30 s. We attribute this to residual etching of the InAlAs layer during the recess etch. Recessed gates with length between 200 and 1000 nm were fabricated in this process. At last one layer

TABLE II
SUMMARY OF THE DEVICE GEOMETRIES AND THEIR dc PERFORMANCE. THE DEVICES WERE FABRICATED ON SAMPLE A

Gate length [nm]	Source-drain separation [μm]	I_d at V_d = 400mV and V_g = 0mV [mA/mm]	R_{DS} [Ω]	I_g(on) [mA/mm]	I_g(off) [mA/mm]	V_{th} [mV]	g_m(DC) [S/mm]
1000	2.5	500	13.9	0.7	0.9	-510	1.3
500	2.0	575	13.2	0.7	1.0	-550	1.6
200	1.4	690	10.9	0.7	1.0	-810	1.2

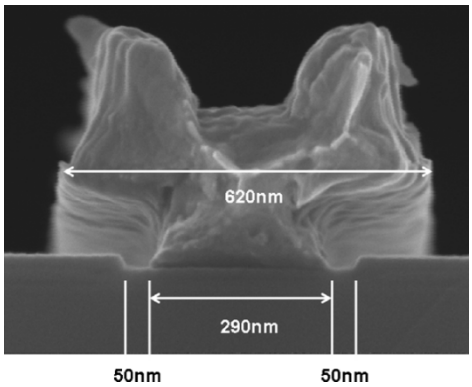

Fig. 3. SEM image of a cleaved cross section of a recessed gate. The gate length is 290 nm, and the lateral recess length is 50 nm.

of Ti–Pd–Au interconnect metal was deposited using optical lithography and electron beam evaporation.

To evaluate the effectiveness of the recess, a method for measuring the sheet resistance of the InAs channel layer in the access regions of the transistor is required. This measurement must not incorporate the parallel conduction of the n^+-InAs cap layer, as this parallel conduction does not contribute to the transistors source and drain resistances, R_s and R_d. As discussed before, normal TLM or Hall measurements of the full set of epitaxial layers measure the parallel conduction paths of the n^+-InAs cap and the InAs quantum well layers, and hence do not provide the required information. Nor does removing the n^+-InAs cap layer prior to Hall or TLM measurements suffice because cap layer removal changes the electron density in the InAs channel, n. Required instead is a TLM measurement with the doped cap layer present but no conduction through the doped cap layer. The sheet resistance of the source and drain access region, $R_{\rm access}$, is measured by measuring the source/drain (S/D) resistance, $R_{\rm DS}$, of a series of HFETs of identical gate length as a function of S/D separation $L_{\rm SD}$. This measurement is taken at $V_d = 0$ mV so as to maintain the HFET channel regions in their linear resistive bias region.

Fig. 4 shows results of such measurements for different gate voltages on Sample C. The data analysis is identical to that of TLM test structures. The rate of variation of $R_{\rm DS}$ with $L_{\rm SD}$ is the product of the device width, W, and $R_{\rm access}$. The y-intercept (extrapolation of $R_{\rm DS}$ to zero $L_{\rm SD}$) is the sum of the contact resistances and the channel resistance in the gate region. It can be seen in Fig. 3 that the measured $R_{\rm access}$ is independent of the gate voltage, V_g, as expected. The y-intercept does depend on V_g because the resistance under the gate increases as the device is pinched off. With this method, $R_{\rm access}$ of Samples A, B, and C was determined to be 110 $\Omega/$sq, 140 $\Omega/$sq, and 200 $\Omega/$sq,

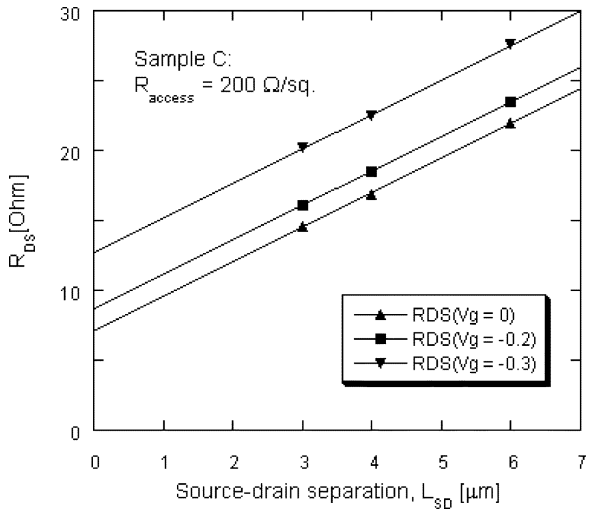

Fig. 4. Determination of the access sheet resistance, $R_{\rm access}$, by a TLM-like measurement: The S/D resistance $R_{\rm DS}$ is plotted for different devices on Sample C as a function of their S/D separation $L_{\rm SD}$. From the slope the access sheet resistance of 200 $\Omega/$sq is calculated. As expected, the slope is independent of gate voltage V_g and the y-intercept increases as the device is pinched off.

respectively. These values should be compared to the sheet resistance of the material after selectively removing the n^+-InAs cap (as shown in Table I). In the case of Sample A, the conductivity increased by 10%, in the case of Sample B by 30%, and in the case of Sample C by 50%.

V. DEVICE RESULTS AND DISCUSSION

The following dc and RF measurements were made on HFETs on Sample A. All measurements are common-source. The measured HFETs have two gate fingers with a total width W of 40 μm. Devices with gate length L_g of 1000, 500, and 200 nm were measured. Table II summarizes the device geometry and the dc performance. The RF performance and the dc operating points are summarized in Table III.

Fig. 5(a) shows the drain current I_d as a function of drain bias V_d of a 500-nm gate length HFET. Fig. 5(b) shows the gate leakage current I_g. There are two contributions to I_g. First, there is a peak at $V_g = -300$ mV, which dominates I_g when the device is turned on. This contribution is well understood and is due to holes generated in the InAs channel by impact ionization [4], [5], [13]. Second, there is a contribution to I_g that increases monotonically with reverse gate bias. This second contribution dominates I_g when the device is turned off and is believed to be due to tunneling through the AlSb barrier. The dc transconductance, $g_m(dc)$, of this HFET is shown in Fig. 5(c). As normally observed in InAs-channel HFETs [5]–[7], $g_m(dc)$ peaks

TABLE III
SUMMARY OF RF DEVICE PERFORMANCE AND dc OPERATING POINTS. THE DEVICES WERE FABRICATED ON SAMPLE A

Gate length [nm]	V_d [mV]	V_g [mV]	g_m (at 25GHz) [S/mm]	C_{gs} [pF/mm]	C_{gd} [pF/mm]	f_τ [GHz]	f_{max} [GHz]
1000	450	-400	0.98	3.18	0.70	40	89
500	450	-475	1.16	1.58	0.49	89	140
200	350	-650	1.05	0.59	0.44	162	137

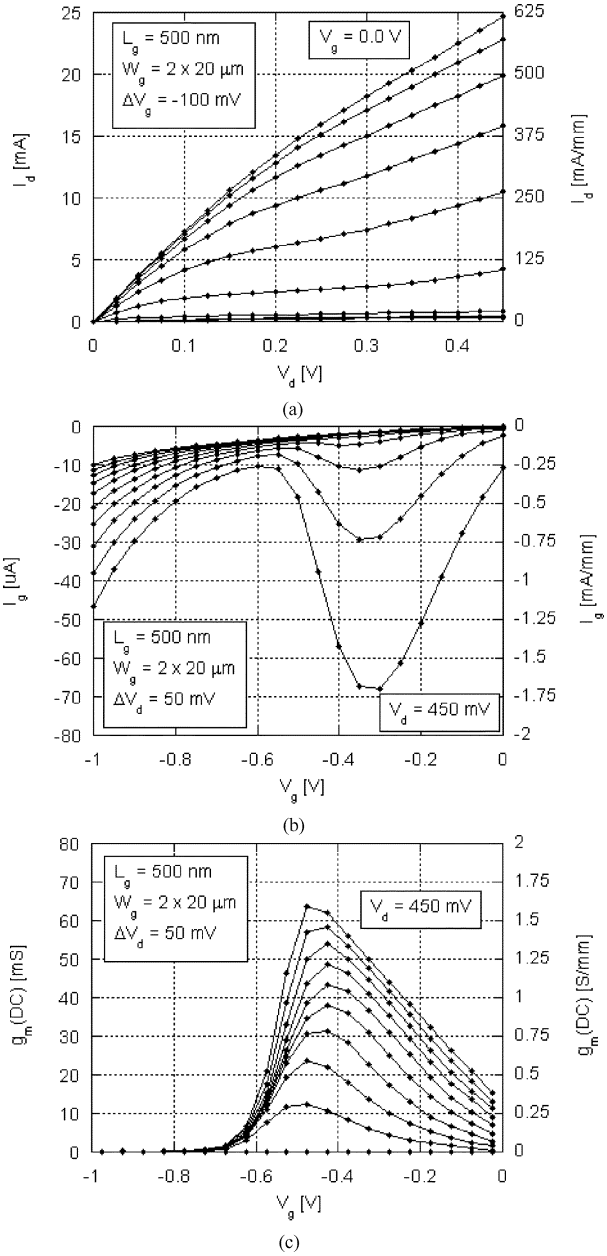

Fig. 5. Common-source dc characteristics of an HFET with gate length L_g of 500 nm. The device has two gate fingers with total gate width W_g of 40 μm. (a) Drain current I_d as a function of drain bias V_d. (b) Gate leakage current I_g as a function of gate bias V_g (c) DC transconductance $g_m(dc)$ as a function of V_g.

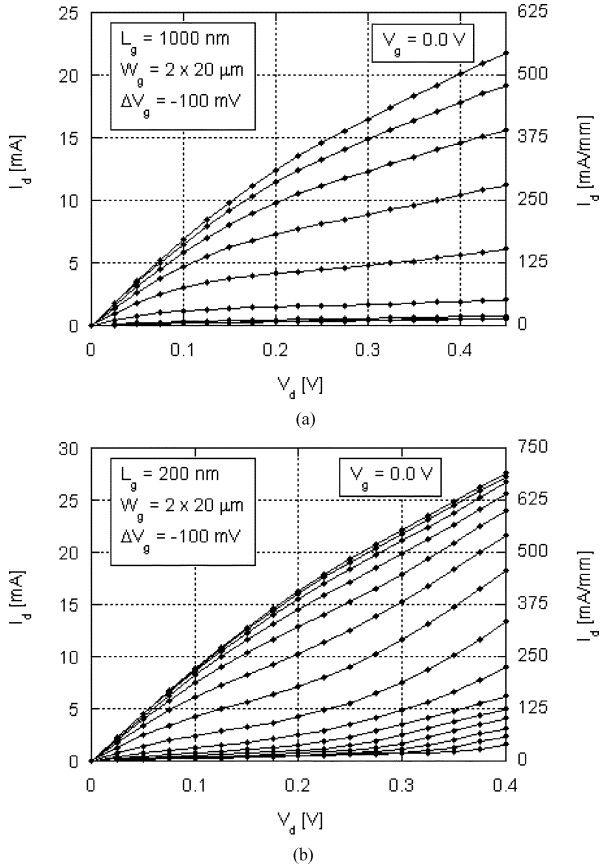

Fig. 6. Common-source dc characteristics of HFETs with L_g of (a) 1000 and (b) 200 nm. Both devices have two gate fingers with total gate width W_g of 40 μm.

just above $V_{\rm th}$; in this case at $V_g = -475$ mV. In Fig. 6(a) and (b), the I_d-ndash;V_d characteristics of devices with $L_g = 1000$ and $L_g = 200$ nm are shown. The dc performance at $L_g = 1000$ and $L_g = 500$ nm are similar. However, at $L_g = 200$ nm the HFET shows poorer dc performance than at the two longer gate lengths: its $V_{\rm th}$ increases from -810 to -970 mV as V_d increases from 250 to 400 mV. In addition, the output conductance is increased. As shown in Table III, the S/D resistance $R_{\rm DS}$ decreases from 13.9 to 10.9 Ω as L_g decreases from 1000 to 200 nm. This is due to the different S/D separation, $L_{\rm SD}$. Similarly, I_d at $V_d = 400$ mV increases from 500 to 690 mA. As discussed earlier, we have independently measured an access sheet resistance of 110 Ω/sq and a sheet resistance in the gate region of 120 Ω/sq. We find good agreement between the measurements and the calculations if we assume a contact resistance of 0.14 Ω-mm. In this calculation, we also assume that the sheet resistance in the gate region is unaffected by the presence of the gate metallization for $V_g = 0$ mV. We believe the contact resistance can be decreased below 0.1 Ω-mm, the value in the nonrecessed gate process, by further process development. Table II also shows the maximum on-state I_g for $V_d = 400$ mV, I_g(on), and the

off-state I_g, I_g(off), at $V_g = -1000$ mV and $V_d = 400$ mV. Both I_g(on) and I_g(off) are independent of L_g. For the purpose of this paper, the threshold voltage $V_{\rm th}$ is defined as the intercept of the x-axis and the tangent fitted to the steepest point of the transfer characteristics. There is some variation of $V_{\rm th}$ with V_d. The minimum value is given as $V_{\rm th}$ in Table II. Note that there is a large negative shift of $V_{\rm th}$ from -550 to -810 mV when L_g is reduced from 500 to 200 nm.

S-parameters were measured on-wafer from 5–40 GHz employing on-wafer TRL calibration structures. From the measured S-parameters, we determined Y-parameters, the current gain h_{21}, and Mason's unilateral power gain U. We fitted the Y-parameters to a simple equivalent circuit model, which included only the gate/source capacitance, $C_{\rm gs}$, the gate-drain capacitance, $C_{\rm gd}$, and the transconductance, g_m. The maximum frequency of oscillation, $f_{\rm max}$, was obtained by extrapolating U by -20 dB/decade to unity. In the measurements we observe that $|h_{21}|^2$ rolls off more slowly than -20 dB/decade. This is due to two effects: First, $C_{\rm gd}$ is significant and leads to an additional high-frequency zero in the transfer function. Second, the gate leakage current limits $|h_{21}|^2$ at low frequencies. For this reason, the current gain cutoff frequency, f_τ, is calculated from the extracted circuit elements, $C_{\rm gs}$, $C_{\rm gd}$ and g_m by using $f_\tau = (1/2\pi) \cdot g_m/(C_{\rm gs} + C_{\rm gd})$. For our devices this approach leads to a more reliable and lower f_τ than extrapolating the measured $|h_{21}|^2$ by -20 dB/decade. The 1000-, 500-, and 200-nm gate length devices have f_τ of 40, 89, and 162 GHz, respectively, and $f_{\rm max}$ of 89, 140, and 137 GHz, respectively. As in nonrecessed devices [6], we find that the RF transconductance, g_m, is smaller than the dc value, $g_m(dc)$, and that g_m has little frequency dependence between 5 and 40 GHz. The measured $C_{\rm gs}$ values agree with our expectations based upon capacitance per unit area calculations using 1-D-Poisson [15]. $C_{\rm gd}$, however, is much larger then the value of 0.1 – 0.2 pF/mm, which we expect from two-dimensional field simulations of the device structure and which is commonly observed in III-V based HFETs [1]. We find that $C_{\rm gd}$ decreases with decreasing gate length. We observe variation in $C_{\rm gd}$ for nominally identical devices. For example, for the 500-nm gate length devices $C_{\rm gd}$ ranges from 0.8 pF/mm to 0.5 pF/mm. As expected, we find best device performance for small $C_{\rm gd}$ values.

The recessed-gate HFETs with 500-nm gate length, $L_{\rm g}$, show robust performance with a low threshold voltage, $V_{\rm th}$, of -550 mV. Their $f_{\rm max}$ of 140 GHz is the highest reported for an InAs-channel HFET with L_g of 500 nm. At $L_g = 200$ nm, however, unexplained scaling problems are observed. These scaling problems are evident in the dc characteristics in Fig. 5 as increased output conductance and as a negative threshold shift. This can be caused by parasitic back-gating due to accumulation of impact-ionization generated holes in the buffer layers, the so-called kink-effect [4], [5], [13]. As the gate length shortens, the electric field along the channel increases leading to higher impact-ionization rates. At all gate length, the RF measurements show larger than expected $C_{\rm gd}$ ranging from 0.7 to 0.4 pF/mm. To improve device performance, particularly for short gate length devices, $C_{\rm gd}$ must be reduced. First, the large $C_{\rm gd}$ significantly reduces $f_{\rm max}$. Second, the $C_{\rm gd}$ of 0.44 pF/mm is a significant fraction of the total input capacitance of the 200-nm L_g devices and reduces f_t from the expected 230 GHz to the observed 162 GHz. The physical origin of the large $C_{\rm gd}$ is not understood. However, we do know that the large $C_{\rm gd}$ is due to the recess design or the recess process. We observe a smaller $C_{\rm gd}$ of 0.1 to 0.2 pF/mm in nonrecessed devices fabricated in our laboratory. We speculate that unintentional charge accumulation in the recess structure or a too short lateral recess length causes the large $C_{\rm gd}$. As discussed earlier, in our present process it is not possible to widen the recess laterally due to channel degradation.

VI. Conclusion

We have developed a self-aligned recess gate technology for mm-wave InAs-channel HFETs. The technology employs an n^+-InAs–InAlAs double cap layer structure and a selective citric-acid-based wet etch. The experiments demonstrate a reduction of the access sheet resistance by up to 50%. HFETs with gate lengths of 200, 500, and 1000 nm were fabricated. The dc and RF performance is robust at 1000- and 500-nm gate length. At 200-nm gate length, increased output conductance and an increased threshold voltage were observed. At 500-nm gate length, the devices have low thresholds (-550 mV), high drain current (575 mA/mm), high dc transconductance (1.6 S/mm), and low gate leakage (below 1.7 mA/mm). We have demonstrated $f_\tau/f_{\rm max}$ values of 89/140 GHz and 162/137 GHz for the 500- and 200-nm gate length devices, respectively. Presently, the device performance and further scaling is limited by an abnormally high $C_{\rm gd}$ value of 0.4 to 0.5 pF/mm.

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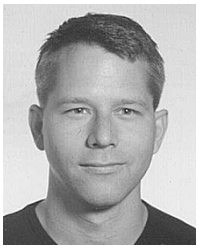

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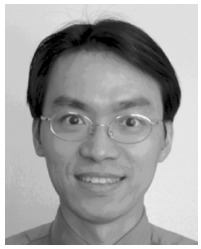

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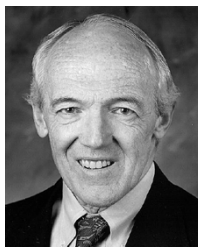

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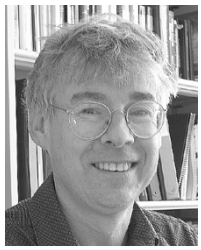

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J. I. Bergman (M'97), photograph and biography not available at the time of publication.