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Thermal Properties of Metamorphic Buffer Materials for Growth of InP Double Heterojunction Bipolar Transistors on GaAs Substrates

Y. M. Kim, M. Dahlstrom, M. J. W. Rodwell, and A. C. Gossard

***Abstract*—Metamorphic double heterojunction bipolar transistors (MDHBT) using InP or InAlP as metamorphic buffer layers were grown on GaAs substrates. For devices using InP buffer layers on GaAs substrates, measured junction-ambient temperature rise at 7.5 mW power dissipation is comparable to those of devices grown on InP substrates, while much larger temperature rises are observed when InAlP buffer layers are employed. By comparing the measured temperature rise with that computed as a function of the known transistor geometry and unknown buffer-layer thermal conductivity, we estimate that the thermal conductivity of a uniform InP buffer layer is 35 $\pm$ 5 W/k-m, while a linearly graded InAlP buffer layer with 0.2 μm InP upper layer has 8 $\pm$ 3 W/k-m effective thermal conductivity. These results strongly suggest the use of InP metamorphic buffer layers in metamorphic InP-based DHBTs grown on GaAs substrates.**

***Index Terms*—Heterojunction bipolar transistor (HBT), metamorphic, thermal conductivity.**

I. Introduction

InP-based double heterojunction bipolar transistors (DHBTs) are a key technology for high-speed optical fiber and wireless transmission ICs. InP substrates are expensive and are not available in as large sizes as GaAs substrates. Moreover, InP substrates are fragile and are easily broken in fabrication. This motivates development of lattice-mismatched metamorphic growth of InP DHBTs on GaAs substrates. Such devices are referred to as metamorphic DHBTs (MDHBTs). Thermal performance is of critical importance, as high-speed DHBTs must operate at emitter power densities exceeding 250 kW/cm^2.

Transistor thermal resistance is critically dependent upon the thermal resistance of layers lying immediately below the collector [1]. Therefore, the subcollector semiconductor must be selected for high thermal conductivity (avoiding thick layers of low thermal conductivity InGaAs with $\kappa = 5$ W/k-m). Additionally, in the MDHBTs, thermal resistance can be dominated by the poor thermal conductivity of the thick (1–1.5 μm) metamorphic buffer layer lying immediately below the subcollector. We have found that AlGaAsSb and InAlAs metamorphic buffer layers have very low effective thermal conductivities [2], and have earlier reported MDHBTs with higher thermal conductivity InP buffer layers [3], [4]. AlGaAsSb and InAlAs buffers have low effective thermal conductivities because they are alloy materials. Here we compare thermal characteristics of MDHBTs grown on InP (nonalloy) and graded InAlP (alloy) buffer layers to those of lattice-matched devices. An InAlP buffer is investigated for the following reason. Because the heat flux spreads as it flows away from the transistor junctions, the thermal conductivity of the upper part of buffer is more important in heat transfer than that of the lower part of buffer. The upper portions of the $In_xAl_{1-x}P$ buffer is composed of material with only a low AlP alloy fraction (almost pure InP), and hence a higher thermal conductivity than the lower portions of the buffer, where the alloy fraction is close to 50%. This is advantageous relative to the cases of InAlAs and AlGaAsSb linearly graded buffer layers. For those materials, the upper portions of the buffer layers are alloys (InAs–AlAs and AlGaAs–AlGaSb) of approximately equal composition of each constituent material and hence reduced thermal conductivity is expected in the upper portions of the buffer layers. We nevertheless find that use of InAlP buffer layers results in high DHBT thermal resistance.

In the case of InP buffer layers and narrow emitter geometries, MDHBT thermal resistance is comparable to that of lattice-matched HBTs. A low 32 °C junction-ambient temperature rise is obtained in a device operating at 235 kW/cm^2 (7.5 mW dissipation in a device with a 8 μm $\times$ 0.4 μm emitter).

II. Growth

The samples were grown using a Varian Gen II molecular beam epitaxy (MBE) system equipped with valved phosphorous (P) and arsenic (As) cracker cells. InAlP and InP metamorphic buffer layer materials were used for this study.

The InAlP buffer layer was grown at 400 °C in order to keep the surface smooth while the InP buffer layer was grown at 470 °C, as measured by a pyrometer. While a InAlP metamorphic buffer layer grown at 400 °C showed smoother surface morphology (3.6 nm rms roughness) than a sample grown at 470 °C (5.9 nm rms roughness), the InP buffer layers showed rougher surface morphology at 400 °C growth (13.3 nm rms roughness) than at 470 °C growth (9.5 nm rms roughness). The InAlP buffer was graded in composition from that matched to a GaAs lattice ($In_{0.49}Al_{0.51}P$) to that matched to an InP lattice. After a 1.3 μm linearly graded $In_xAl_{1-x}P$ layer, a 200-nm InP buffer was grown at 470 °C. The InP buffer was grown directly on the GaAs substrate to a thickness of 1.5 μm. In both cases, the metamorphic buffer layer growth was followed by growth of an InP-$In_{0.53}Ga_{0.47}As$ – InP DHBT structure. Key features of the layer structure include an InP emitter, a 400-Å-thick InGaAs base with 52 meV band-gap grading for base transit time reduction, a 100-Å $In_{0.53}Ga_{0.47}As$ setback layer, a 240-Å $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ base-collector heterojunction grade, and a 1660-Å InP collector. For applied $V_{CE} > 1.3$ V, the total collector depletion thickness is 2000 Å. The N^+ subcollector layer was composed of 250 Å $In_{0.53}Ga_{0.47}As$ and 1250 Å InP. The layer structures are shown in Fig. 1.

The reflection high-energy electron diffraction (RHEED) pattern was observed during buffer layer growth. The RHEED pattern showed diffraction streaks during growth of the InAlP buffer layers. These streaks suggest relatively smooth epitaxial growth. Even during InP buffer layer growth, low-intensity streaks were observed in the RHEED pattern.

Manuscript received November 8, 2002; revised January 22, 2003. This work was supported by the ONRby Grant N00014-01-1-0065. The review of this brief was arranged by Editor C.-P. Lee.

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Digital Object Identifier 10.1109/TED.2003.813225

Emitter cap	$In_{0.53}Ga_{0.47}As$: Si ($2x10^{19}$ cm^{-3})	300 Å
Emitter grade	$In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$: Si ($2x10^{19}$ cm^{-3})	200 Å
Emitter	InP : Si ($1x10^{19}$ cm^{-3})	700 Å
	InP : Si ($8x10^{17}$ cm^{-3})	500 Å
Grade	$In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$: Si ($4x10^{17}$ cm^{-3})	280 Å
Base	$In_{0.53}Ga_{0.47}As$: Be ($4x10^{19}$ cm^{-3})	400 Å
SetBack	$In_{0.53}Ga_{0.47}As$: Si ($2x10^{16}$ cm^{-3})	100 Å
Grade	$In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$: Si ($2x10^{16}$ cm^{-3})	240 Å
Delta doping	InP : Si ($5.6x10^{18}$ cm^{-3})	30 Å
Collector	InP : Si ($2x10^{16}$ cm^{-3})	1630 Å
Sub collector	$In_{0.53}Ga_{0.47}As$: Si ($1x10^{19}$ cm^{-3})	250 Å
Sub collector	InP : Si ($1x10^{19}$ cm^{-3})	1250 Å
Buffer	InP	2000 Å
	$In_{0.49}Al_{0.51}P \rightarrow$ InP or InP	1.3 μm
GaAs (100) semi-insulating substrate		

Fig. 1. Layer structure of the MDHBT grown on a GaAs substrate.

	MDHBT with InP buffer	MDHBT with InAlP buffer
Current gain	76	40
Collector current ideality factor	1.07	1.08
Base current ideality factor	1.62	1.37
Breakdown voltage (V)	5.5	4.5
Emitter resistance (Ω)	8.8	17.2
Base resistance (Ω)	44.0	27.6

Fig. 2. DC parameters for devices with InP and InAlP buffer layers.

III. Results

The dc parameters for the devices with InP buffer and InAlP buffer are summarized in Fig. 2. Fig. 3 shows the measured temperature rise of a device operating at 7.5-mW dissipation, plotted as a function of base mesa area. The measured transistors have emitter junction lengths of 8 μm and emitter junction widths of 0.3, 0.4, 0.7, and 1.7 μm. The base mesa length is 8.5 μm, while the base mesa widths are 1.0, 1.2, 1.6, 1.7, 2.0, 2.6, 2.7, 3.0, and 4.0 μm. Junction temperature was obtained by measuring the change of $V_{\rm BE}$ with a variable applied $V_{\rm CE}$ under conditions of constant forced collector bias current (I_C) [1]. Thermal characteristics of the MDHBTs are compared to that of a reference lattice-matched DHBT (LMDHBT) of similar geometry. The lattice-matched device has a similar layer structure except that the $In_{0.53}Ga_{0.47}As$ subcollector thickness is 500 Å and the substrate is InP. As is shown by the data (Fig. 3), MDHBTs with InP buffer layers show junction temperatures only slightly larger than that of lattice-matched devices. Much higher junction temperatures are observed with InAlP buffer layers. Since increased junction operating temperature will degrade device reliability [1], [2], these data strongly suggests the use of InP buffer layers in metamorphic HBTs.

In order to determine the metamorphic buffer layer thermal conductivity, the expected HBT collector junction temperature was calculated by solving the Laplace heat flow equation in three dimensions. The same emitter junction sizes and base mesa sizes as in the measurements were used in the calculation. The calculations also assumed a 2000 Å InP collector, a 250 Å $In_{0.53}Ga_{0.47}As$ upper N^+ subcollector, a 1250 Å InP lower N^+ subcollector, a 1.5 μm metamorphic buffer layer, and a 350 μm GaAs substrate. Junction temperature rise

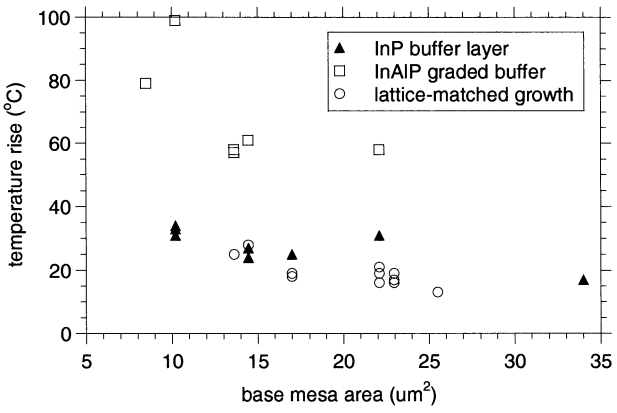

Fig. 3. Temperature rise of HBTs biased at 7.5–mW dissipation as a function of base mesa area for MDHBTs with InP and InAlP buffer layers, as compared to a DHBT grown lattice-matched (LM) on an InP substrate.

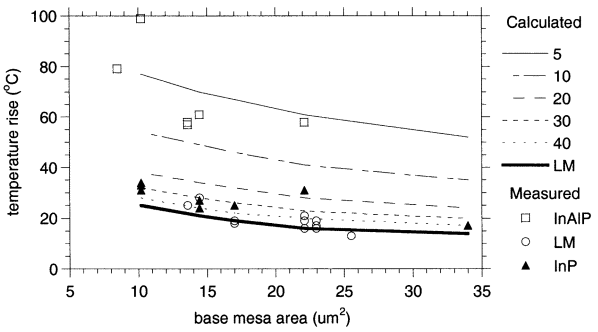

Fig. 4. Comparison of measured junction temperatures of MDHBTs with InP and InAlP buffer layers data and LM-DHBT with calculated junction temperatures, computed as a function of metamorphic buffer layer thermal conductivity. The upper five curves represent calculated temperature rises assuming metamorphic buffer layer thermal conductivities of 5, 10, 20, 30, and 40 W/k-m, while the lowest curve represents the calculated temperature rise of a DHBT grown lattice-matched on an InP substrate.

was calculated with 7.5 mW applied power. The power dissipation is assumed to be uniformly distributed within the collector depletion layer and the thermal conductivities were assumed to be 5 W/k-m for $In_{0.53}Ga_{0.47}As$, 68 W/k-m for lattice-matched InP, and 44 W/k-m for the GaAs substrate. Fig. 4 compares the results of the calculations with the measured data. The upper five curves of the plot represent calculated junction temperature rise assuming metamorphic buffer layer thermal conductivities of 5, 10, 20, 30, and 40 W/k-m, while the lowest curve of the plot represents the junction computed temperature of an HBT grown lattice-matched on an InP substrate. Comparing these, we estimate that the effective thermal conductivities of the InP and InAlP buffer layers are approximately 35 ± 5 W/k-m and 8 ± 3 W/k-m.

IV. Summary

We have investigated InP and InAlP as metamorphic buffer layer materials in MDHBTs. The temperature rises at 7.5 mW device dissipation were measured. MDHBTs with InP buffer layers showed thermal resistance comparable to LMDHBT, while MDHBTs with InAlP buffer layers showed large junction temperature rise. Thermal conductivities of metamorphic buffer layers were determined to be 35 ± 5 W/k-m for InP and 8 ± 3 W/k-m for InAlP, the difference resulting from phonon Rayleigh scattering in alloy semiconductors. The value of 35 ± 5 W/k-m for the InP metamorphic buffer is much lower than the value of 68 W/k-m for lattice-matched InP. We believe the reduced thermal conductivity results from the defects associated

with metamorphic growth. The data strongly suggests use of InP metamorphic buffer layers in metamorphic DHBTs.

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Temperature-Dependent Characteristics of Polysilicon and Diffused Resistors

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***Abstract*—The temperature-dependent characteristics of polysilicon and diffused resistors have been studied. By using the 0.18-μm CMOS technology, a cobalt salicide process is employed and silicide is formed at the ends of resistors. Based on a simple and useful model, some important parameters of resistors including bulk sheet resistance ($R_{\rm bulk}$) and interface resistance ($R_{\rm interface}$) are obtained at different temperature. For diffused resistors, the $R_{\rm bulk}$ and $R_{\rm interface}$ values are increased and decreased with the increase of temperature, respectively. Positive values of temperature coefficient of resistance (TCR) are observed. Furthermore, TCR values are decreased with the decrease of resistor size. For polysilicon resistors, the $R_{\rm interface}$ values are decreased with the increase of temperature. In addition, negative and positive TCR values of $R_{\rm bulk}$ are found in n^+ and p^+ polysilicon resistors, respectively. In conclusion, by comparing the studied diffused and polysilicon resistors, the negative trends of TCR are observed when the resistor sizes are decreased.**

***Index Terms*—Diffused resistor, polysilicon resistor, TCR.**

I. INTRODUCTION

Recently, due to the progressive requirements, the scaling down consideration and fabrication of deep submicron meter devices have become key roles in modern IC industry [1], [2]. In the ULSI's technologies, polysilicon and diffused resistors are widely used throughout the semiconductor industry for a variety of applications especially in a CMOS process [3], [4]. Polysilicon and diffused resistors are widely used in the integrated circuits. Diffused resistors are commonly used in electrostatic discharge (ESD) protection circuits. Also, the doped polysilicon is usually employed as a precise analog resistor element for a variety of applications [5]–[8]. It is known that the stability of resistors directly affects the accuracy of reference voltage, power consumption, and proper working of an electrical circuit. Previously, many models related to resistors were reported [9]–[13]. Experimentally, in order to reduce contact resistance, the salicide process has been widely applied to subquarter micron ULSI technology. The existence of interface between silicide and silicon causes undesired drawbacks of resistors. In a previous work [14], a simple model is reported to analyze and calculate the bulk resistance ($R_{\rm bulk}$) and interface resistance ($R_{\rm interface}$) between silicon and silicide. The size effect plays a key role in the resistor performance especially when devices are scaled down to submicron-meter regime. Furthermore, temperature variation results in the inaccuracies of resistance control of thin film resistors. This causes the undesired drawbacks in circuit applications. Particularly, in many high-speed mixed-signal IC applications, the highly precise and relatively temperature-independent performance is important and necessary [15].

In this work, the temperature-dependent characteristics of polysilicon and diffused resistors are studied. The temperature coefficient of resistance (TCR) characteristics of n^+/p^+ polysilicon and diffused resistors are compared. From the experimental results, negative TCR values of $R_{\rm interface}$ values are observed in the diffused and polysilicon resistors. Negative TCR values are observed in resistors with small dimensions. On the contrary, positive TCR values are found in resistors with larger dimensions.

II. EXPERIMENT

The studied resistors were fabricated by using a 0.18-μm CMOS technology. The diffused resistors were isolated by shallow trench isolation (STI) process. The amorphous silicon film of 2000 Å was deposited on STI by using a low-pressure chemical vapor deposition (LPCVD) system at 540 °C. After forming poly-gate and Si_3N_4 spacers, the n^+ and p^+ source/drain regions were formed by the n^+ implant condition of As/40KeV/5.0 $\times$ 10^{15} cm^{-2} and the p^+ implant condition of B/15KeV/3.0 $\times$ 10^{13} cm^{-2} and BF_2/5KeV/3.5 $\times$ 10^{15} cm^{-2}. At the same time, the n^+ and p^+ resistors were formed by n^+ and p^+ source/drain implantation, respectively. Then, a source/drain rapid thermal annealing (RTA) process was performed at 1025 °C for 30 s to activate the dopants. A resistor-protect-oxide (RPO) layer was deposited on resistors. The RPO layer prevents resistors from silicidation in the following cobalt salicide process. Co-silicide regions, formed on the polysilicon-gate and diffusion layers, were then introduced. After the interlevel dielectric (ILD) deposition, a chemical mechanical polish (CMP) process was used in planar process. Then, a via-hole etching collimated-Ti CVD TiN-barrier W-plug and W-CMP process were performed. Finally, the metallization process was followed by a forming N_2 gas annealing at 400 °C.

III. RESULTS AND DISCUSSION

Experimentally, typical values of bulk sheet resistances ($R_{\rm bulk}$) of n^+ (p^+) polysilicon and diffused resistors, formed by source/drain implantation, are about 311 (330) and 60 (135) $\Omega/\square$. The total resistance R can be expressed as [14]

$$R = R_C + R_{\rm silicide} + R_{\rm bulk} \times \frac{L}{W} + R_{\rm interface} \times \frac{W_0}{W} \qquad (1)$$

where R_C and $R_{\rm silicide}$ are the effective contact and silicide resistance, L and W are the length and width of polysilicon resistors, respectively. W_0 is a normalization constant (e.g., $= 1$ μm) to guarantee the right dimensions of the full equation. Experimentally, R_C and $R_{\rm silicide}$ are

Manuscript received October 17, 2002; revised January 17, 2003. This work was supported in part by the National Science Council, R.O.C., under Contract NSC 91-2215-E-006-016. The review of this brief was arranged by Editor J. Vasi.

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Digital Object Identifier 10.1109/TED.2003.813472