Substitutional-Gate MOSFETs With Composite $(In_{0.53}Ga_{0.47}As/InAs/In_{0.53}Ga_{0.47}As)$ Channels and Self-Aligned MBE Source–Drain Regrowth

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***Abstract*—We report enhancement-mode composite-channel ($In_{0.53}Ga_{0.47}As/InAs/In_{0.53}Ga_{0.47}As$) MOSFETs fabricated using a substitutional-gate process, with n^+ relaxed InAs source–drain regions formed by regrowth by molecular beam epitaxy. A device with 70-nm gate length and 2-nm $In_{0.53}Ga_{0.47}As$/3.5-nm InAs/3-nm $In_{0.53}Ga_{0.47}As$ channel showed a peak transconductance of greater than 0.76 mS/μm at $V_{ds} = 0.4$ V and showed $I_d = 0.5$ mA/μm at $V_{ds} = 0.4$ V and $V_{gs} - V_{th} = 0.7$ V. The subthreshold swing at $V_{ds} = 0.1$ V was 130 mV/dec.**

***Index Terms*—Composite channel, molecular beam epitaxy (MBE) regrowth, source–drain regrowth, substitutional gate, III–V MOSFETs.**

I. Introduction

THE low transport mass in InGaAs MOSFETs provides high electron velocity; dependent upon the dielectric thickness [1] and the density D_{it} of dielectric–semiconductor traps, this can result in high ON-state currents. InGaAs MOSFETs have therefore drawn attention for application in VLSI [2]–[4].

MOSFET on-current and integration density are also determined by the design of the source and drain regions. High source electron concentrations are needed to prevent source starvation [5]. Source and drain bulk and metal–semiconductor contact resistances must be low [1]; this demands [6] doping approaching 10^{20} cm^{-3}. To obtain small drain-induced barrier lowering (DIBL), the source and drain regions must be very shallow.

MOSFETs having shallow heavily doped source and drain can be formed using gate-last processes where the channel is accessed by etching through an n^+ source/drain (S/D) contact layer [2]. Shallow heavily doped source–drain regions can also be formed by epitaxial regrowth. In the gate-first regrowth processes in [1] and [4], the gate electrode and its sidewall were defined by sputtering, PECVD, and reactive-ion etching; such processes can readily damage the channel and dielectric–channel interface via exposure to energetic ions or electrons, UV photons, or X-rays [7], [8]. Gate-last source–drain regrowth processes [3], [9] can be designed to reduce or avoid such damage.

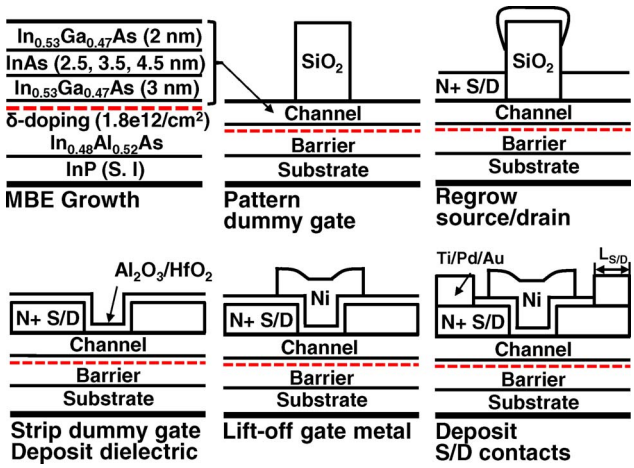

Fig. 1. Epitaxial layer structure and schematic illustration of the substitutional-gate process.

Here, we report gate-last III–V MOSFETs using for the first time source–drain regions regrown by molecular beam epitaxy (MBE). Through MBE regrowth of n^+ InAs source and drain, we obtain $\rho_C = 1.0\ \Omega \cdot \mu m^2$ S/D contact resistivity, as opposed to 49 $\Omega \cdot \mu m^2$ reported [3] for MOCVD regrowth. Given contact length [1] $L_{S/D}$ (Fig. 1) and gate width W_G, the contacts contribute $\rho_C / L_{S/D} W_G$ to the source and drain access resistivities, and resistivities of $\sim 1\ \Omega \cdot \mu m^2$ [1], [3] are necessary for MOSFETs at the 15-nm node. The devices use $In_{0.53}Ga_{0.47}As/InAs/In_{0.53}Ga_{0.47}As$ composite channels [10] and show improved transfer characteristics at low supply voltage when compared to 10-nm $In_{0.53}Ga_{0.47}As$-channel devices, showing > 0.76 mS/μm of peak transconductance at $V_{ds} = 0.4$ V.

II. Device Structure and Fabrication

Fig. 1 shows the fabrication process sequence. The epitaxial layers, grown by solid source MBE, consist of an InP (100) semi-insulating substrate, a 300-nm unintentionally doped (UID) $In_{0.52}Al_{0.48}As$ barrier/buffer layer, a 3-nm Si-doped (1.8×10^{12}/cm^2) $In_{0.52}Al_{0.48}As$ pulse doping layer,

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a 3-nm $In_{0.52}Al_{0.48}As$ (UID) setback layer, and the channel. Four different channel designs are reported here: 1) 2-nm $In_{0.53}Ga_{0.47}As$/2.5-nm InAs/3-nm $In_{0.53}Ga_{0.47}As$; 2) 2-nm $In_{0.53}Ga_{0.47}As$/3.5-nm InAs/3-nm $In_{0.53}Ga_{0.47}As$; 3) 2-nm $In_{0.53}Ga_{0.47}As$/4.5-nm InAs/3-nm $In_{0.53}Ga_{0.47}As$; and 4) 10-nm $In_{0.53}Ga_{0.47}As$ (UID). This final sample has no setback layer between the channel and the pulse-doped layer.

After wafer growth, 300 nm of SiO_2 was deposited at 250 °C by PECVD, and a 20-nm chromium etch mask layer was deposited by e-beam evaporation. Dummy gate patterns having gate lengths between 50 nm and 1 μm were first patterned by e-beam lithography using ma-N 2403 resist, subsequently transferred to the Cr hard mask by ICP dry etching with Cl_2/O_2, and finally transferred to the SiO_2 layer by ICP dry etching with SF_6/Ar. The Cr hard mask was then removed by photoresist planarization [11] and etching.

Prior to transfer into the MBE chamber, samples were oxidized by exposure to UV ozone for 30 min and dipped in dilute HCl (1:10 HCl:H_2O) for 1 min to remove surface oxides. Inside the MBE chamber at a pressure less than 1×10^{-9} torr, samples were heated for 1 h at 325 °C and then were heated to 420 °C and treated with thermally cracked hydrogen ($\approx 1 \times 10^{-6}$ torr) for 40 min before regrowth. Approximately 60 nm of 6×10^{19} cm^{-3} Si-doped InAs was grown relaxed on the sample surface nonselectively.

MBE regrowth leaves amorphous InAs debris on the top surfaces and edges of the dummy gates. Debris on the top surface of the dummy gates was removed by a photoresist planarization process [11]. The devices were then mesa isolated by wet etching in a mixture of 50-mL H_2O: 50-g anhydrous citric acid and 75-mL H_2O_2. The SiO_2 dummy gate is then removed using a buffered oxide etch (BOE) and a dilute concentration of an ethylene oxide/propylene oxide copolymer surfactant to suppress deposition of the debris on the exposed channel surface.

Immediately prior to gate dielectric deposition, samples were treated in dilute HCl (1:10 HCl:H_2O) to remove the native oxide on the channel surface. The dielectric was then deposited using an Oxford Instruments FlexAL atomic layer deposition system. Thirty-cycle Al_2O_3 ($\sim$3.3 nm) was deposited at 300 °C after a multiple-cycle [12] TMA and H_2 plasma surface preparation. Fifteen-cycle HfO_2 ($\sim$1.5 nm) was then deposited at 300 °C; this layer protects the Al_2O_3 from etching in photoresist developer. Samples were then transferred in air to a rapid thermal annealer and annealed at 400 °C for 1 h with forming gas.

To minimize channel damage [7], [8], 90 nm of Ni was thermally evaporated for the gate electrode. The S/D electrode area was defined by optical lithography, and the gate oxide was removed with BOE. Finally, (20-nm Ti/20-nm Pd/130-nm Au) S/D electrodes were defined by e-beam evaporation and lift-off.

III. Results and Discussion

In Fig. 2, the output (I_d–V_{ds}) and transfer (I_d–V_{gs}) characteristics of composite-channel FETs [Fig. 2(a)–(d)] are compared to those of a 10-nm-thick $In_{0.53}Ga_{0.47}As$-channel FET [Fig. 2(e) and (f)]. The composite-channel (2-nm $In_{0.53}Ga_{0.47}As$/3.5-nm InAs/3-nm $In_{0.53}Ga_{0.47}As$) device shows a maximum drain current density (I_d/W_g) of

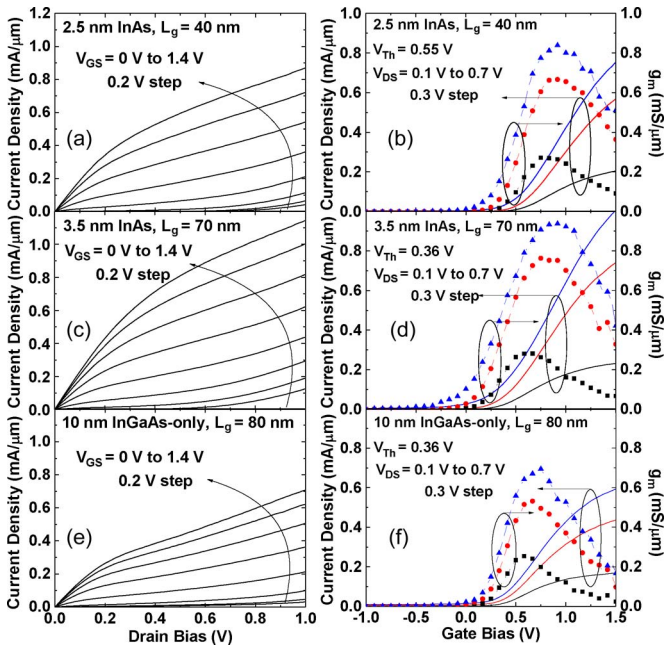

Fig. 2. (a) Output (I_d–V_{ds}) and (b) transfer (I_d–V_{gs} and g_m) characteristics for the composite-channel (2-nm $In_{0.53}Ga_{0.47}As$/2.5-nm InAs/3-nm $In_{0.53}Ga_{0.47}As$) device with 40-nm L_g. (c) and (d) Characteristics for the (2-nm $In_{0.53}Ga_{0.47}As$/3.5-nm InAs/3-nm $In_{0.53}Ga_{0.47}As$)-channel device with 70-nm L_g. (e) and (f) Characteristics for the 10-nm $In_{0.53}Ga_{0.47}As$-channel device with 80-nm L_g.

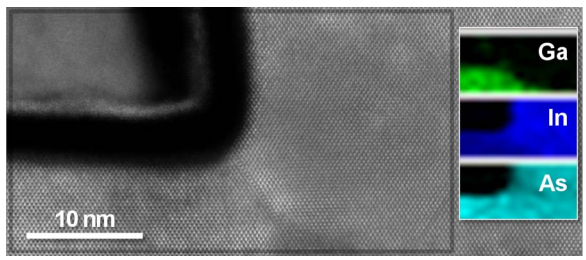

Fig. 3. Cross-sectional STEM image of the source–channel junction of the InGaAs-channel device. The insets show the Ga, In, and As spatial distributions derived from EDX analysis.

~ 0.5 mA/μm at $V_{gs} - V_{th} = 0.7$ V and $V_{ds} = 0.4$ V and a maximum transconductance (g_m) of 0.76 mS/μm at $V_{ds} = 0.4$ V, a bias at which I_d does not show a significant increase from impact ionization. Its threshold voltage extracted from linear extrapolation is $\sim$0.36 V. The composite-channel device shows significantly larger I_d and g_m than the $In_{0.53}Ga_{0.47}As$-channel device; there are several possible causes. First, Ga out-migration during regrowth converts the channel to InAs in the regions under the regrown source and drain, as shown in the EDX analysis in Fig. 3. There is consequently an InAs/$In_{0.53}Ga_{0.47}As$ heterobarrier in the source–channel junction of the InGaAs-channel device. In the composite-channel FETs, the average indium composition is higher, and the barrier is partially suppressed. Second, the mean depth of the electron wave function is greater for the composite-channel device; this reduces surface scattering. Third, the lower bound state effective mass in the composite channel should increase the carrier injection velocity. It is difficult to distinguish these effects given the available data. Fig. 4 shows the $\log(I_d)$–V_d plots for the devices as a function of InAs layer thickness. For

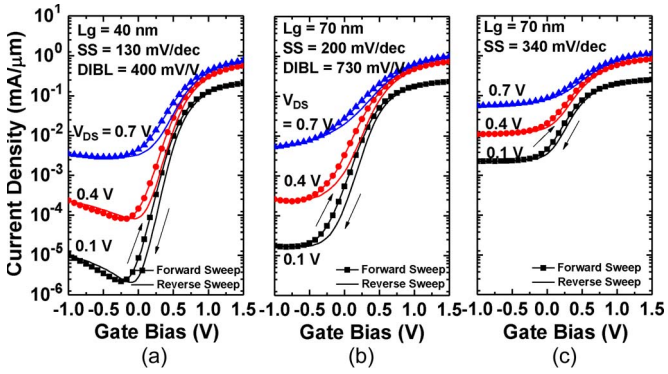

Fig. 4. $\log(I_d)-V_{\rm gs}$ plots of the composite-channel devices with (a) 2.5-, (b) 3.5-, and (c) 4.5-nm-thick InAs.

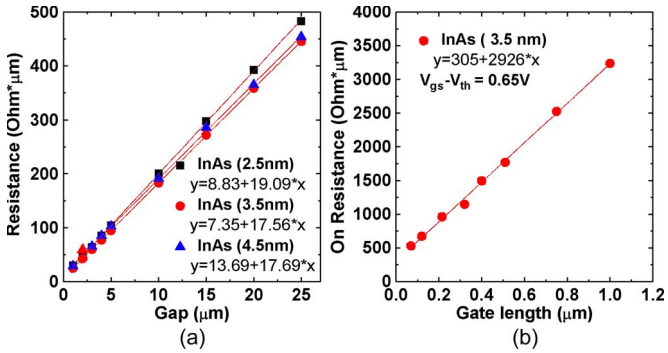

Fig. 5. (a) TLM data for contacts to the regrown n^+ InAs layer. (b) Variation with gate length of the drain–source on-resistance $R_{\rm ds}$ at $V_{\rm gs}-V_{\rm th}=0.65$ V and $V_{\rm ds}=0.025$ V for the composite-channel devices.

all devices, approximately 60-mV hysteresis is observed in the subthreshold region. Source–drain leakage increases, and drain breakdown voltage decreases, as the InAs layer thickness is increased. The increased leakage may be attributed to misfit dislocations at the heterointerface acting as a structural donor source [13]. The strain due to the lattice mismatch is relaxed by the generation of misfit dislocations as the InAs critical thickness is less than 4.5 nm at the growth conditions that we used ($\sim$460 °C and $\sim$30 As/In flux ratio) [14]. The device with the 2.5-nm InAs layer [Fig. 4(a)] shows 130-mV/dec subthreshold swing (SS) at $V_{\rm ds}=0.1$ V and 400-mV/V DIBL.

Fig. 5(a) shows the transmission line method (TLM) measurements of contacts to the InAs n^+ regrowth, from which 1-$\Omega\cdot\mu$m^2 metal-regrowth contact resistivity and $\sim$18-$\Omega/\square$ n^+-layer sheet resistance are determined. Fig. 5(b) shows, as a function of L_g, the FET normalized output resistance $R_{\rm ds}$ measured at $(V_{\rm gs}-V_{\rm th})=0.65$ V. At $L_g=70$ nm, $R_{\rm ds}W_g=530\ \Omega\cdot\mu$m.

Note that source and drain access resistances R_s and R_d *cannot be inferred* from the $R_{\rm ds}$ data in Fig. 5(b). Consider, as a single example, the case of a ballistic FET with degenerate population inversion and with $R_s=R_d=0\ \Omega$ [15], [16]. In this limiting case, $I_d/W_g=K(V_{\rm gs}-V_{\rm th})^{3/2}-K(V_{\rm gd}-V_{\rm th})^{3/2}$ for $(V_{\rm gs},V_{\rm gd})>V_{\rm th}$, from which it is found that $g_m\equiv\partial I_d/\partial V_{\rm gs}=(3/2)K(V_{\rm gs}-V_{\rm th})^{1/2}$, while at $V_{\rm ds}$ of 0 V, we find that $1/R_{\rm ds}=g_{\rm ds}=(3/2)K(V_{\rm gs}-V_{\rm th})^{1/2}=g_m$. In this ballistic example, nonzero output resistance is observed even with zero source and drain resistances.

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