Collector-Pedestal InGaAs/InP DHBTs Fabricated in a Single-Growth, Triple-Implant Process

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***Abstract*—This letter reports InP/$In_{0.53}Ga_{0.47}As$/InP double heterojunction bipolar transistors (DHBTs) employing an N^+ subcollector and N^+ collector pedestal—formed by blanket Fe and patterned Si ion implants, intended to reduce the extrinsic collector-base capacitance C_{cb} associated with the device footprint. The Fe implant is used to compensate Si within the upper 130 nm of the N^+ subcollector that lies underneath the base ohmic contact, as well as compensate the $\sim 1 - 7 \times 10^{-7}$ C/cm^2 surface charge at the interface between the indium phosphide (InP) substrate and the N^- collector drift layer. By implanting the subcollector, C_{cb} associated with the base interconnect pad is eliminated, and when combined with the Fe implant and selective Si pedestal implant, further reduces C_{cb} by creating a thick extrinsic collector region underneath the base contact. Unlike previous InP heterojunction bipolar transistor collector pedestal processes, multiple epitaxial growths are not required. The InP DHBTs here have simultaneous 352-GHz f_τ and 403-GHz f_{max}. The dc current gain $\beta \approx 38$, $BV_{ceo} = 6.0$ V, $BV_{cbo} = 5.4$ V, and $I_{cbo} < 50$ pA at $V_{cb} = 0.3$ V.**

***Index Terms*—Collector pedestal, heterojunction bipolar transistor (HBT), indium phosphide (InP), ion implantation.**

I. Introduction

WHILE indium phosphide (InP)-based double heterojunction bipolar transistors (DHBTs) benefit from high-carrier mobilities and saturated velocities [1], SiGe heterojunction bipolar transistors (HBTs) have smaller junction dimensions and smaller extrinsic parasitics. Consequently, digital circuit speed in SiGe and InP has been comparable [2], with SiGe offering higher integration scales. Similar scaling of InP HBTs is therefore important.

Manufacturable InP HBT processes [3]–[6] utilizing $\leq$ 500-nm width emitter junctions (W_e) and $\leq$ 500-nm wide base contacts (W_b) have been reported. These processes have demonstrated 350-GHz f_τ, 400-GHz f_{max}, and 150-GHz static frequency dividers. In order to realize a $\sqrt{2}:1$ increase in f_τ, f_{max}, and digital logic speed through device scaling [7], the emitter and collector junctions must be narrowed $\sim$ 2:1. If the collector junction lies under the base contact, W_b must be reduced and the base contact resistivity ρ_c lowered substantially. Reducing ρ_c is not simple, and narrower base contacts present significant challenges for high-yield IC fabrication as well as present a significant bulk metal resistance along the length of the contact. Furthermore, the parasitic base interconnect pad capacitance $C_{cb,pad}$ becomes a significant fraction of the total C_{cb} in HBTs with small emitter lengths, which are used for low-power logic.

Several approaches have been pursued to reduce C_{cb} [8]–[11] as alternatives to reducing W_b. In collector pedestal processes [10], [11], Si is implanted into an undoped InP layer above the N^+ subcollector to form an N^+ electrical link between the collector drift region and subcollector. Outside this implanted region, the depletion depth is increased and C_{cb} reduced. There are several difficulties with this method that must be addressed. Two MBE growths are required, the first forming the subcollector and pedestal layers, and the second providing the active HBT layers. DHBTs reported in [11] suffer from a process-dependent charge at the regrowth interface—which if left uncompensated does not decrease C_{cb} at low bias voltages. The pedestal doping must be kept in the low-10^{18} cm^{-3} range to minimize broadening of the pedestal through implant lateral straggle. Lastly, the pedestal processes reported in [10] and [11] only reduce the extrinsic base pad capacitance—it is not removed completely.

In this letter, an alternative process for reducing C_{cb} is demonstrated, wherein ion implantation alone forms the subcollector and pedestal, and multiple MBE growths are not required. This process utilizes an Fe implanted extrinsic semi-insulating layer for an increased depletion depth underneath the extrinsic collector-base junction, a selectively implanted buried subcollector formed by a deep Si implant, and an N^+ collector pedestal is created by a second set of Si implants. In addition to reducing C_{cb} and compensating interface charge at the epitaxial growth interface, this technology provides the following enhancements: C_{cb} associated with the base interconnect pad is eliminated, only one MBE growth is needed, increased wafer planarity is realized, and hence potentially improved yield in the fabrication of large circuits.

Prior to this letter, the highest f_τ and f_{max} reported for an InP DHBT employing a collector pedestal was 252 and 283 GHz [10], respectively, having a 35-nm base and a 110-nm collector, where two MBE growths were required. Here, we report a 352-GHz f_τ and 403-GHz f_{max} InP DHBT utilizing only an ion implantation to form the subcollector and pedestal-like

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structure. This is the first demonstration of an HBT employing these implant techniques, while being the highest f_τ and $f_{\max}$ for a device utilizing ion implants.

II. Experimental Details

The process flow is shown in Fig. 1(a)–(d) and the top view of the device is shown in Fig. 1(e). A semi-insulating InP substrate is implanted with Fe at 150 keV at a fluence of 2.4×10^{14} ions-cm^{-2} [Fig. 1(a)], and the wafer is annealed at 700 °C for 5 min. The sample is then selectively implanted [Fig. 1(b)], using SiN_x as an implant mask, with Si at 350 keV/5×10^{14} ions-cm^{-2} and partially activated at 600 °C/10 s. The buried subcollector thus formed extends 0.5 μm beyond the length of the emitter stripe [Fig. 1(e)]. Iron is a mid-gap acceptor in InP; it fully compensates the Si donors when the Fe concentration exceeds that of Si [12], [13]. This forms a selectively patterned, buried, and isolated N^+ subcollector [Fig. 1(b)] layer. Further, the Fe implant compensates the N-type interface charge between the substrate and collector drift epitaxial layer; importantly, this compensation implant can accommodate a significantly wider range of interface charge variance than could be realized by a p-type compensation layer [11]. An N^+ pedestal linking to the buried subcollector is then formed by a second set of patterned Si implants at 100 keV/4×10^{14} ions-cm^{-2}, 40 keV/7×10^{13} ions-cm^{-2}, and 10 keV/3×10^{13} ions-cm^{-2}. Raised N^+ pedestals for the collector contacts are simultaneously realized [Fig. 1(c)]. The sample is then annealed at 800 °C/30 s to activate the Si [14]. Note, to prevent a phosphorous outdiffusion during all anneals, the wafer is capped using SiN_x.

The active InP DHBT layers are grown by MBE. Growth is initiated with 3.5 nm of undoped InGaAs—it is needed to act as an etch-stop layer between the InP collector and the InP substrate. The collector, base, and emitter layers are then grown using the same design reported in [15] for a triple-mesa InP DHBT. The active device junctions are formed by chemical wet-etch, and since the subcollector has been implanted, a mesa isolation etch is not required—reducing the height of the HBT by $\sim$ 500 nm.

III. Results

Standard transmission line measurements (TLMs) show the base $\rho_s \approx 610\ \Omega$ and $\rho_c \approx 16\ \Omega \cdot \mu\text{m}^2$. The emitter ρ_c determined from RF parameter extraction is $\approx 10\ \Omega \cdot \mu\text{m}^2$. From TLM and Hall measurements, the sheet resistance of the subcollector is $\rho_s \approx 21\ \Omega$. The resistivity of the pedestal layer measured on separate test wafers is $\rho \approx 6\ \Omega \cdot \mu$m; similar test structures are not available on the wafer carrying HBTs. The collector contact is made to N^+ InP (without an N^+ InGaAs contact layer) and only partially annealed (Ge/Ni/Ge/Au/Ni/Au, 320 °C/60 s) because at higher temperatures the base ρ_c would increase rapidly. Consequently, the collector ρ_c is very high $\approx 200\ \Omega \cdot \mu\text{m}^2$.

The HBTs exhibit $\beta \approx 38$, common–emitter and common–base breakdown voltages $\text{BV}_{\text{ceo}} = 6.0$ V and $\text{BV}_{\text{cbo}} = 5.4$ V ($I_c = 50\ \mu$A), collector and base ideality factors $n_c = 1.18$ and $n_b = 1.53$, and a collector leakage current $I_{\text{cbo}} < 50$ pA (at an applied $V_{\text{cb,offset}} = 0.3$ V). A plot of the common–emitter current–voltage and Gummel characteristics is shown in Fig. 2. The device β, ideality factors, and collector leakage current are consistent with those measured from the triple-mesa HBT equivalent [15]. By comparison, the triple-mesa HBT

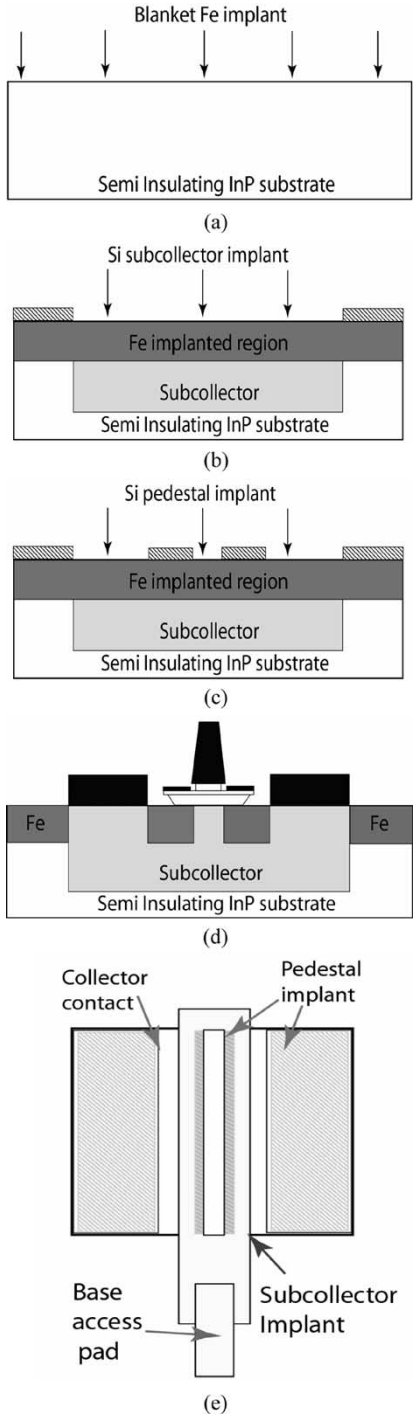

Fig. 1. Pedestal/subcollector process cross section—(a) blanket surface Fe implant to suppress interface states and form the extrinsic collector depletion regions, (b) deep Si implant to form the subcollector, (c) Si pedestal implant to electrically link the N^- drift collector and collector contacts to the subcollector, (d) active HBT layers are then grown and device formation ensues, and (e) top view of the device showing the pedestal (hatched lines) and subcollector implants.

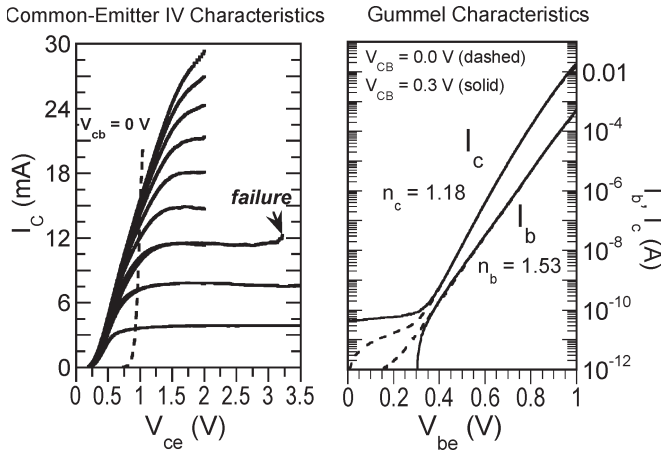

Fig. 2. Common–emitter $I-V$ characteristics ($I_{b,\mathrm{step}} = 100\ \mu$A) and Gummel characteristics. Emitter junction dimension $A_{\mathrm{je}} = 0.6 \times 4.3\ \mu\mathrm{m}^2$.

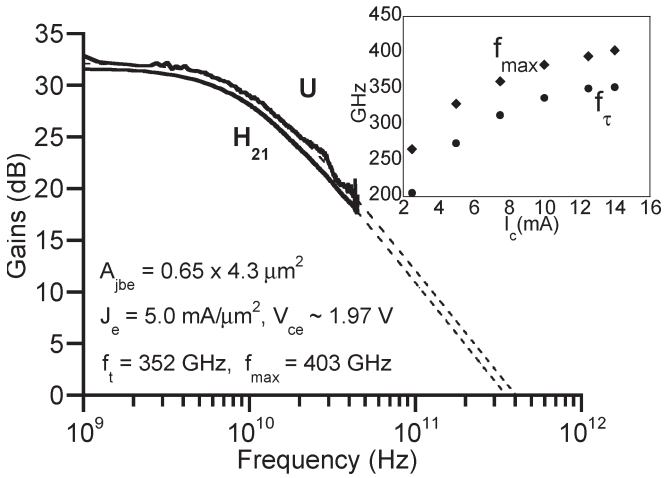

Fig. 3. Measured microwave gains H_{21} and Mason's unilateral power gain U at a bias associated with peak f_τ and $f_{\max}$. Figure inset $-f_\tau$ and $f_{\max}$ versus I_c.

in [15] has $\mathrm{BV}_{\mathrm{ceo}} = 3.9$ V and $\mathrm{BV}_{\mathrm{cbo}} = 4.3$ V. SIMS and capacitance–voltage data indicate that the Fe implant compensates the N^+ subcollector implant to a depth of 130 nm, increasing the depletion depth of the extrinsic collector by this amount. Leakage between adjacent HBTs at 5 μm separation is ~ 10 pA/μm at 3 V, indicating adequate device isolation.

DC 45-GHz S-parameter measurements are carried out after performing an off-wafer line-reflect-reflect-match calibration on an Agilent 8510C network analyzer. On-wafer open and short circuit pad structures identical to the ones used by the devices are measured after calibration in order to de-embed their associated parasitics from the device measurements. A maximum 352-GHz f_τ and 403-GHz $f_{\max}$ (Fig. 3) is demonstrated at $I_c = 14$ mA and $V_{\mathrm{ce}} = 1.96$ V ($J_e = 5.0$ mA/μm^2, $C_{\mathrm{cb}}/I_c = 0.43$ ps/V). The f_τ and $f_{\max}$ are determined from an extrapolation through a least square fit between the single-pole transfer functions for H_{21} and U to the measured data [13]. This HBT has a $0.6 \times 4.3\ \mu\mathrm{m}^2$ emitter junction area A_{je} and base mesa width of 1.3 μm. The pedestal stripe as defined on the photomask is $0.9 \times 5.25\ \mu\mathrm{m}^2$ while the length of the subcollector as defined on the photomask is 5.25 μm [Fig. 1(e)].

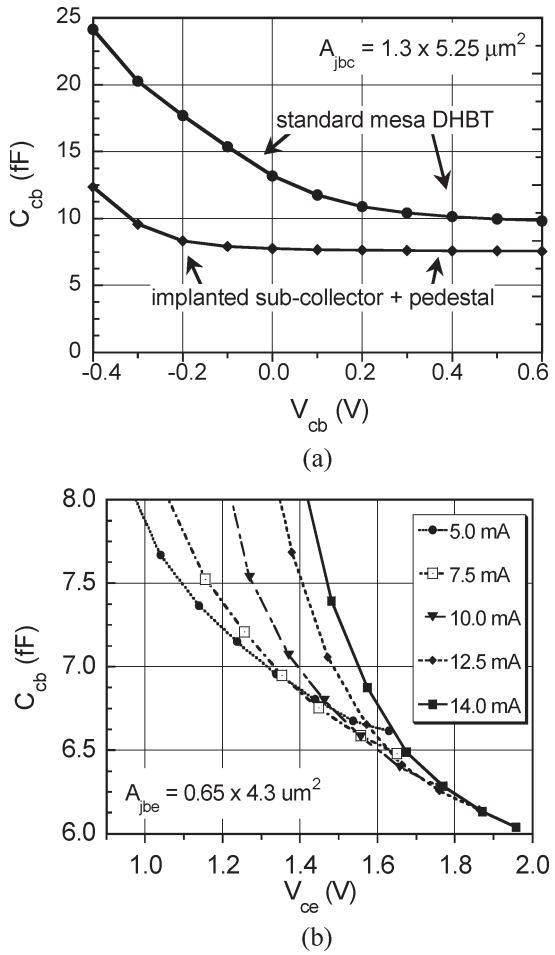

Fig. 4. Variation of C_{cb} with V_{cb} at $I_c = 0$ mA for (a) a mesa HBT and the pedestal HBT (b) and variation of C_{cb} with V_{ce} at different I_c to show the effect of high-series collector resistance. Junction areas as well as the emitter, base, and drift collector layer structures of the two HBTs are identical.

Fig. 4(a) compares the variation of C_{cb} versus $V_{\mathrm{cb}}(I_c = 0$ mA) between the implanted HBT and a triple-mesa device [13], both using the same footprint and similar active device layer structure. At moderate reverse biases when the collector is fully depleted, C_{cb} is reduced $\sim 30\%$. The compensation of interface charge is evident, as seen by the reduction in C_{cb}, compared to a mesa DHBT [15], over the entire measured range of bias voltages. Fig. 4(b) shows the variation of C_{cb} versus I_c and V_{ce}. The HBTs reported here have high-collector resistance $R_c \sim 32\ \Omega$, which is also evident from the I_c-V_{ce} characteristics. The voltage drop $I_c \cdot R_c$ is significant and the collector potential must be progressively increased as I_c, to fully deplete the drift collector. The lower f_τ and $f_{\max}$ demonstrated by the implanted HBTs compared to their triple-mesa counterpart (450/490 GHz $f_\tau/f_{\max}$) [15] is mostly due to the increased delay associated with the terms $kT/qI_c \cdot (C_{\mathrm{cb}} + C_{\mathrm{je}})$ and $R_c \cdot C_{\mathrm{cb}}$. The origin of the increased R_c is in part due to the increased contact resistance and in part due to the resistance in the implanted pedestal and subcollector. The collector-ohmic-contact process steps are being revised so that the collector ohmic is formed prior to a base contact formation by recess etching the base and the collector layers. Experiments on test samples indicate that a high-temperature anneal

(365 °C/60 s) reduces the contact resistivity of the alloyed collector ohmic contact (Ni/GeAu/Ni/Au) to $\approx 25\ \Omega \cdot \mu\text{m}^2$. TLM test structures from a coprocessed wafer indicate an anomalously high vertical-access resistance through the N^+ pedestal layer. Implant dose variability for Fe and Si is thus also under investigation as a secondary cause of the observed high collector access resistance.

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