PLANAR DEVICE ISOLATION FOR InP BASED DHBTs

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Device isolation of InP based HBTs in the mesa technology, is done by etching down to the substrate; this process suffers from lack of planarity and does not lend itself well to high levels of integration. We report on two techniques for planar isolation of InP based HBTs using selective implantation. The first method involves Fe implantation to isolate the InP collector-subcollector layers. Iron implantation has been performed through the entire HBT layer stack but the sheet resistance obtained was ~5 MΩ/$\square$ [1]. By performing Iron implantation to isolate the InP collector-subcollector regions, we have obtained a maximum sheet resistance of 27MΩ/$\square$ while planarity is improved by ~0.25µm. We believe this is the highest reported value of sheet resistance for Iron implanted samples, when starting with such highly doped templates of 1×10^{19} cm^{-3}. In the second approach, we have utilized selective Si implantation in SI InP to form an isolated, N^{++} subcollector. InP DHBTs were earlier reported with an implanted, narrow N^{+} subcollector stripe lying under the emitter[2], but such structures can have large collector access resistance R$_c$ arising from long, narrow N^{+} layer. We propose to use the isolated subcollector in conjunction with a N^{+} pedestal[3], to obtain a planar device with low C$_{cb}$. DC devices with this implanted subcollector show low base-collector leakage and excellent device isolation is obtained. Furthermore, both these techniques result in zero base pad capacitance.

Iron implantation is performed on epitaxial 130nm InP (1×10^{17} : Si) over 80nm N^{+} InP(1×10^{19}:Si), having a sheet resistance of 45Ω/$\square$. ^{56}Fe implant is performed at an energy of 190 KeV, with a fluence of 4×10^{15} ions/cm^2 and at a substrate temperature of 200°C. The concentration profile of Iron is determined after implant by secondary ion mass spectroscopy(SIMS) and is shown in Figure 1. It shows extensive Iron diffusion and pile up at the surface. The sheet resistance is measured as a function of anneal temperature and is plotted in Figure 2. The maximum sheet resistance observed 27MΩ/$\square$, is after annealing at InP growth temperature (~520°C), in the MBE chamber. The leakage current in the implanted region is ~5 nA/µm at 3V (Figure 3). To measure the extent of non-crystallinity, ion channeling is used. It indicates that the thickness of the amorphous region after implant and anneal at 425°C is 104nm (Figure 4). From the plot of sheet resistance, it is evident that isolation is not by the mechanism of chemical compensation but instead due to the large defect density caused by the Iron implant. The sheet resistance reported here, 27MΩ/$\square$ is the highest known for a damage implant on such highly doped N^{++} InP (1×10^{19} :Si).

Such Fe implants induces large defect density and are not suitable where crystalline regrowth is required. For non-damage, planar isolation, SI InP substrate was selectively implanted with Si, using SiN$_x$ as the implant mask. A multiple energy implant at 200°C has been performed to obtain a flat doping profile of 2×10^{19} cm^{-3} upto 2000Å. The SIMS concentration profile of Si, shown in figure 5 indicates no extensive Si diffusion into the substrate. The sheet resistance is measured as a function of anneal temperature and time (figure 6). A low sheet resistance of 17 Ω/$\square$ is obtained after annealing at 900°C and the mobility (~830 cm^2 /V-s) and sheet charge density(4.3×10^{14} cm^{-2}) are comparable to those for 2000Å epitaxial N^{++} InP (2×10^{19} cm^{-3}:Si). The surface roughness, as measured by AFM, after implant is 1.274nm which after an 800°C anneal is 0.4nm, comparable to virgin InP. Leakage currents measured in the region masked during Si implant ~0.07 nA/µm which indicates the excellent degree of isolation. InP/InGaAs/InP DHBTs(from collector upwards) were grown on the Si implanted InP subcollector. The DC I-V characteristics are shown in figure 7 and the base collector leakage is shown in figure 8. The current gain measured on a large area device of 60x60 µm^2 is ~12. The base collector leakage is low, ~ 0.7 nA/µm^2. We believe that the 0.7 nA/um^2 obtained here is the lowest reverse base collector leakage reported for HBTs grown on implanted InP substrate, while effectiveness of isolation is also demonstrated (~ 0.07 nA/um).

In conclusion, two techniques for planar device isolation are demonstrated. When combined with existing HBT technologies, improved planarity and significant reduction in parasitic base pad capacitance is possible.

[1] S.C. Subramanian *et al.*, 2003 IEEE GaAs IC conference proceedings
[2] M. Sokolich, *et al*, 'InP HBT Integrated Circuit Technology with Selectively Implanted Subcollector and Regrown Device Layers', 2003 IEEE GaAs IC conference proceedings, p.219
[3] Y. Dong, *et al*, 'InP Heterojunction Bipolar Transistor with a Selectively Implanted Collector Pedestal', Proceedings of 2003 International Semiconductor Device Research Symposium, pp. 348-349, December 10-12, Washington, D.C
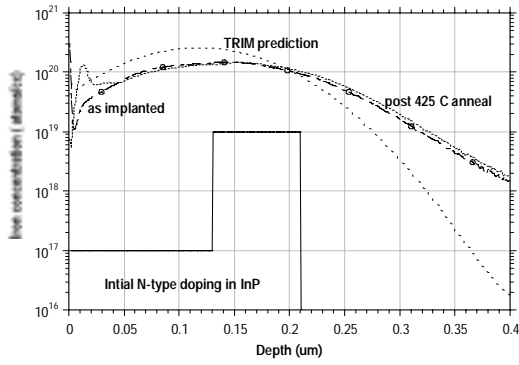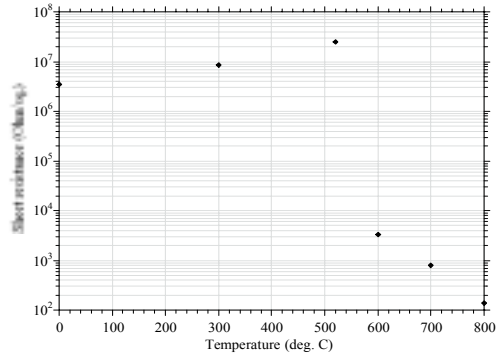
Figure 1: Iron concentration profile

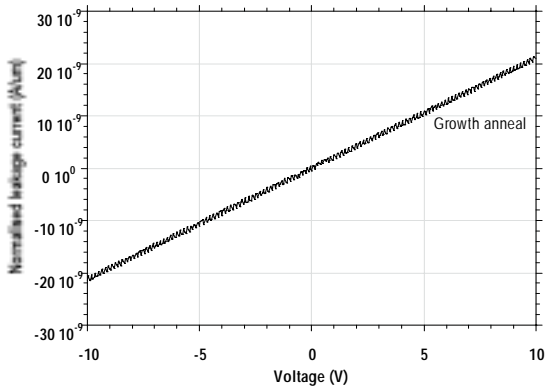Figure 2: Iron isolation sheet resistance
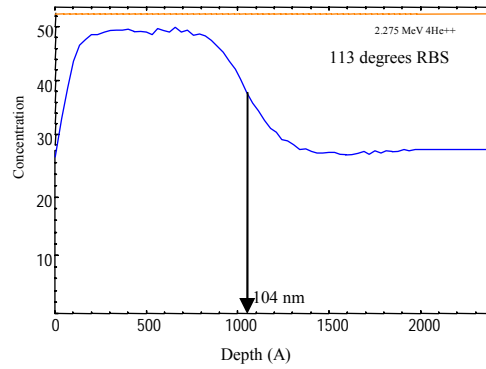

Figure 3: Isolation leakage

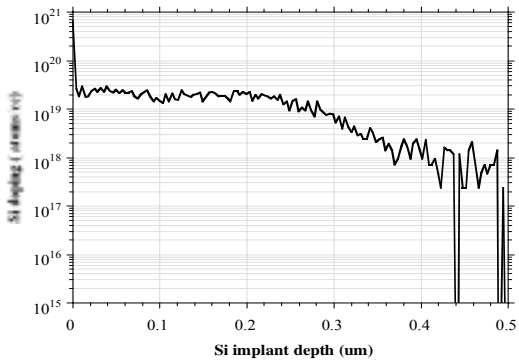Figure 4: RBS plot after 425°C anneal,
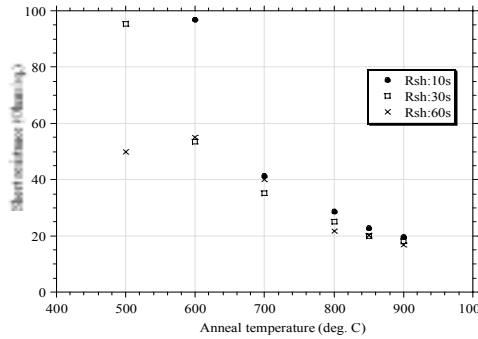

Figure 5: Si concentration profile after implant

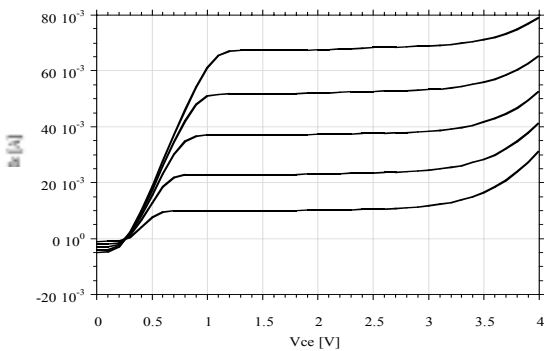Figure 6: Sheet resistance of N^{++} InP after Si implant

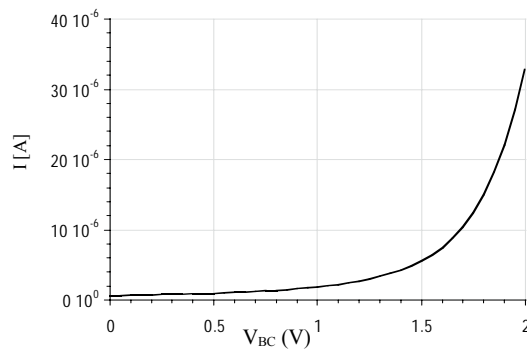Figure 7: DC I-V characteristics of HBT with implanted subcollector, A_E :60x60μm^2, β~12

Figure 8: Reverse base collector leakage