InGaAs–InP Metamorphic DHBTs Grown on GaAs With Lattice-Matched Device Performance and f_τ, $f_{\max} > 268$ GHz

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***Abstract*—InP–$In_{0.53}Ga_{0.47}$As–InP double heterojunction bipolar transistors (DHBTs) were grown on a GaAs substrate using a metamorphic buffer layer and then fabricated. The metamorphic buffer layer is InP—employed because of its high thermal conductivity to minimize device heating. An f_τ and $f_{\max}$ of 268 and 339 GHz were measured, respectively—both records for metamorphic DHBTs. A 70-nm SiO_2 dielectric sidewall was deposited on the emitter contact to permit a longer InP emitter wet etch for increased device yield and reduced base leakage current. The dc current gain β is $\approx$35 and $V_{BR,CEO} = 5.7$ V. The collector leakage current I_{cbo} is 90 pA at $V_{cb} = 0.3$ V. These values of f_τ, $f_{\max}$, I_{cbo}, and β are consistent with InP based DHBTs of the same layer structure grown on a lattice-matched InP substrate.**

***Index Terms*—Heterojunction bipolar transistor (HBT), lattice matched, metamorphic growth.**

I. Introduction

InP–based double heterojunction bipolar transistors (DHBTs) have been aggressively pursued because of their superior material transport properties over SiGe and GaAs [1]. This is demonstrated by the increased value of small signal unity current gain f_τ, unity power gain $f_{\max}$, and higher operating current density J_e that InP devices possess at a given scaling generation [2], [3]. However, compared to SiGe and GaAs, InP substrates are much more expensive and fragile—often breaking during semiconductor manufacturing. In recent years, metamorphic growth of InP-based DHBTs on GaAs substrates has been investigated as a means of accessing the properties of InP in a GaAs manufacturing environment with lowered costs. For these devices to be useful in high speed circuit applications, a low C_{cb}/I_c ratio (high J_e) is necessary [4]—this requires the device operating temperature be addressed during device design [5]. Because the metamorphic buffer layer can have a significant impact on the thermal resistance of the HBT, InP is used for its higher thermal conductivity [6]. Here, we report InP-based metamorphic DHBTs (mHBT) with a 268 GHz f_τ and 339 GHz $f_{\max}$, and low collector leakage current I_{cbo} of 90 pA at $V_{cb} = 0.3$ V [7]. Previous mHBT results from our laboratory produced a 216 GHz f_τ, 284 GHz $f_{\max}$ and $I_{cbo} = 1.2$ nA at $V_{cb} = 0.3$ V [8]. The improvements in performance reported here are mostly attributed to increased device scaling, process changes, and the use of benzocyclobutene (BCB) as the passivation dielectric.

TABLE I
mHBT Layer Composition

Thickness (nm)	Material	Doping cm^{-3}	Description
10	InAs	3E19 : Si	Emitter Cap
30	$In_{0.53}Ga_{0.47}$ As	3E19 : Si	Emitter Cap
80	InP	3E19 : Si	Emitter
10	InP	8E17 : Si	Emitter
30	InP	3E17 : Si	Emitter
30	$In_{0.53}Ga_{0.47}$ As	4E19 : C	Base
20	$In_{0.53}Ga_{0.47}$ As	2E16 : Si	Setback
24	InGaAlAs	2E16 : Si	Base-Col Grade
3	InP	3E18 : Si	Delta doping
153	InP	2E16 : Si	Collector
25	$In_{0.53}Ga_{0.47}$ As	2E19 : Si	Sub Collector
375	InP	3E19 : Si	Sub Collector
20	InP	undoped	Buffer
20	InAlAs	undoped	Current blocking layer
1500	InP	undoped	Metamorphic buffer
Substrate	SI : GaAs		

II. Growth

InP–$In_{0.53}Ga_{0.47}$As–InP DHBTs were grown on a GaAs substrate using a Varian Gen II molecular beam epitaxy (MBE) system. Growth was initiated with a 100-nm undoped GaAs buffer layer, followed by growth at 470 °C of a 1.5 μm undoped InP metamorphic buffer layer. The remaining DHBT layers were then grown (Table I). Details of the base-collector grade design can be found in [9].

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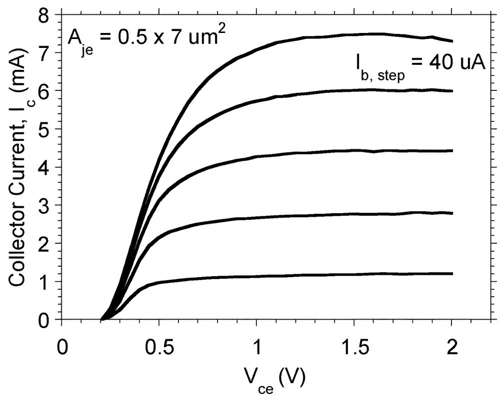

Fig. 1. Common-emitter *I–V* characteristics of mHBT.

III. Fabrication

After emitter contacts were put down, 80 nm of SiO_2 was deposited on the wafer by plasma-enhanced chemical vapor deposition and subsequently etched back by reactive ion etching anisotropically to leave a dielectric sidewall of 70 nm around the contact. This was done to permit a longer wet-etch of the InP emitter semiconductor prior to self-aligned base contact deposition. The remaining device fabrication is similar to that reported in [3], [7], and the devices are passivated with BCB. The metal interconnects are 50-Ω coplanar waveguide transmission-lines.

IV. Measurements and Results

Standard transmission line measurements show the base $\rho_s \approx 814\ \Omega$ and $\rho_c \approx 14\ \Omega \cdot \mu\text{m}^2$, and the emitter $\rho_c \approx 20 - 24\ \Omega \cdot \mu\text{m}^2$. The mHBTs have a dc current gain β of 32–37 and a common-emitter breakdown voltage $V_{\text{BR,CEO}} \approx 5.7$ V. A plot of the common emitter current–voltage characteristics is shown in Fig. 1. HBT Gummel characteristics of the mHBT device and a LM-DHBT device are shown in Fig. 2. The collector and base current ideality factors n_c and n_b for the mHBT are 1.24 and 1.68, respectively. The increased n_b is because of residual n^- InAsP or InGaAsP surrounding the emitter mesa creating a small leakage path. Once the base–emitter junction is turned on ($V_{\text{be}} > 0.8$ V, $I_c > 100\ \mu$A), the n_b of the mHBT is similar to the LM-DHBT. The collector leakage current I_{cbo} is 90 pA at $V_{\text{cb}} = 0.3$ V offset. The I_{cbo} current reduction compared to [8] can be attributed to the use of BCB for both device passivation (compared to polyimide) and isolation of the interconnects from the substrate.

While metamorphic buffer layers are capable of removing the strain associated with the 3.8% lattice mismatch between GaAs and InP, InP buffers cannot suppress defects in the growth of the device layers to the low levels observed with graded ternary buffers [10]. There is a defect density per unit length emitter of 5–6/μm for the devices reported here [11], which results in $\approx$35–45 defects for a $0.5 \times 7\ \mu\text{m}^2$ mHBT. Despite this, the transistor yield is >90%—similar to that observed for LM-HBTs fabricated in our laboratory. Thus, our present data does not support the conclusion that the defect density from the InP metamorphic buffer impacts transistor performance or yield. The thermal resistance of mHBTs using low thermally conductive ternary buffer layers (InP = 68 W/K-m, InAlAs = 9.9 W/K-m, and InGaP = 15 W/K-m) is such that these devices when biased at current densities required for high bandwidth would exhibit several 100 °C self-heating [12].

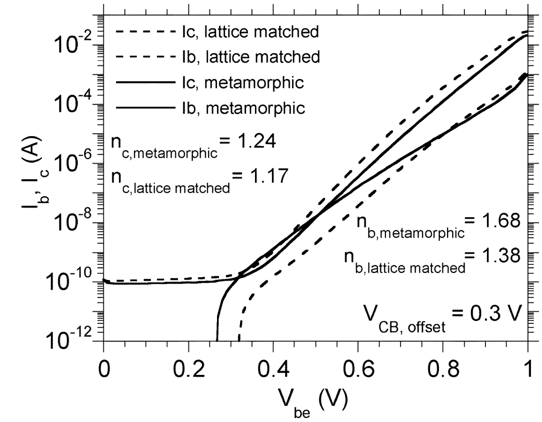

Fig. 2. Gummel characteristics of DHBTs grown metamorphically on a GaAs substrate and on a lattice matched InP substrate.

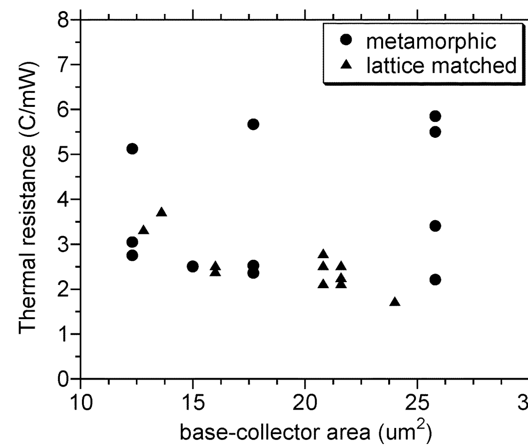

Fig. 3. Comparison of thermal resistance between lattice matched and metamorphically grown DHBTs with identical layer structures.

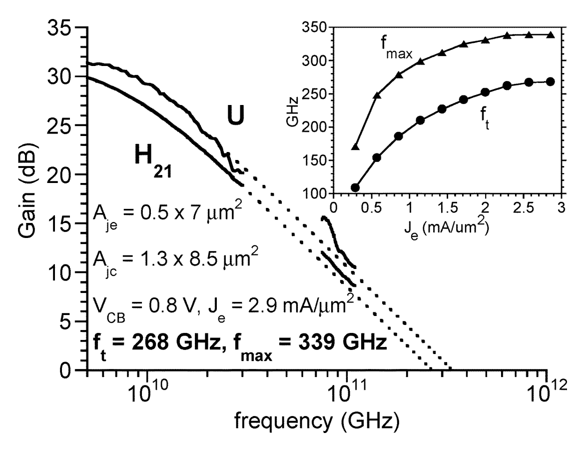

Fig. 4. Measured microwave gains.

Thermal resistance θ_{JA} and device junction temperature were measured using the method of Liu [13] for both mHBTs and LM-DHBTs with identical device layer structures with varying base-collector area (Fig. 3). The average θ_{JA} for the mHBTs and LM-DHBTs is ≈ 2.7 °C/mW and 2.2 °C/mW, respectively [14].

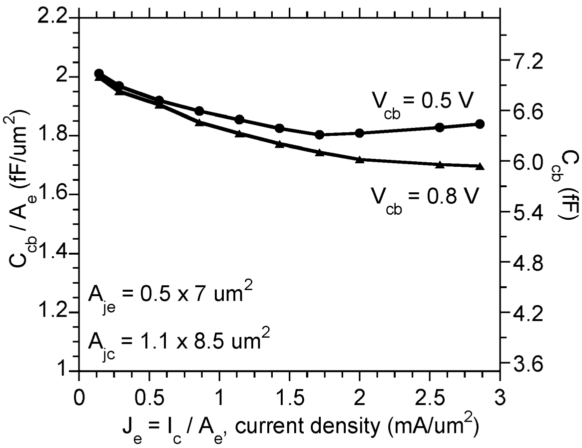

Fig. 5. Variation of base-collector capacitance $C_{\rm cb}$ under bias.

5–30 and 75–110 GHz RF measurements were performed using on wafer thru-reflect-line calibration structures. All calibrations resulted in a $|S_{21}| \ll 0.1$ dB for a zero-effective length transmission line. The mHBT exhibited a maximum 268 GHz f_τ and 339 GHz $f_{\max}$ (Fig. 4) at $I_c = 10$ mA and $V_{\rm ce} = 1.75$ V ($J_e = 2.9$ mA/μm^2, $V_{\rm cb} = 0.8$ V). This device has a 0.5×7 μm^2 emitter junction and 0.35 μm base ohmic contact width—1.3 μm measured base mesa width. The normalized thermal resistance $R_{\rm th} \approx 10.1\,^\circ\mathrm{C}\cdot\mu\mathrm{m}^2/\mathrm{mW}$ and the device experiences an emitter junction to ambient temperature increase $\Delta T \approx 51\,^\circ$C when biased at peak f_τ, $f_{\max}$. The base-collector capacitance $C_{\rm cb}$ was extracted from the device *Y*-parameters ($C_{\rm cbi} + C_{\rm cbx} \cong imag(Y_{12})/\omega$) and is shown in Fig. 5. Peak f_τ and $f_{\max}$ occurs when biased between $J_e = 2.5 - 3.0$ mA/μm^2 at $V_{\rm cb} = 0.8$ V for different HBT on the wafer.

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