An Ultra Low-Power ($\leq$13.6 mW/latch) Static Frequency Divider in an InP/InGaAs DHBT Technology

Zach Griffith*, Navin Parthasarathy*, and Mark J.W. Rodwell*
*Dept. of Electrical and Computer Engineering
University of California, Santa Barbara, CA 93106-9560
Phone: 805-893-5999, E-mail: griffith@ece.ucsb.edu

Miguel Urteaga†, Keisuke Shinohara†, Petra Rowell†, Richard Pierson†, and Bobby Brar†
†Rockwell Scientific Corporation
1049 Camino Dos Rios, Thousand Oaks, CA 91360

Abstract—**An ultra-low power static frequency divider with a maximum clock frequency $>$ 61 GHz was designed and fabricated into a 500 nm InP/In$_{0.53}$Ga$_{47}$As/InP double heterojunction bipolar transistor (DHBT) technology utilizing a collector pedestal process for reduced base-collector capacitance C_{cb}. This is the first reported digital circuit in this material system employing such C_{cb} reduction techniques. The divider operation is fully static, operating from f_{clk} = 4 GHz to 61.2 GHz while dissipating $\leq$ 27.1 mW of power in the flip-flop from a single -2.30 V supply. The power-delay product of this circuit is 113.0 fJ/latch if all devices in the latch are considered, and 63.2 fJ/latch if the power associated with the voltage level-shifting emitter followers is not included in the power-delay calculation. By either method of calculation, this is a record low power-delay product for an InP DHBT-based static frequency divider; more than 2$\times$ lower than has been previously reported. The circuit employs the current mode logic (CML) topology and inductive peaking.**

Index Terms—**Static frequency divider, InP heterojunction bipolar transistor**

I. INTRODUCTION

In recent years, efforts to aggressively scale InP HBTs to submicron features vertically and laterally has resulted in processes intended to produce high-yield circuits having many thousands of devices [1]–[3], where the f_τ and f_{max} of these HBTs is approaching $\sim$ 400 GHz. Applications for these devices include mixed signal ICs for digital radar and advanced communication systems [4]. While the HBT figures-of-merit f_τ and f_{max} describe the maximum bandwidth attainable for a single device, they are of limited value in predicting the speed of logic, mixed-signal, or optical transmission ICs. A regularly cited digital figure-of-merit for a device technology is a static frequency divider. It is a master-slave (M-S) flip-flop consisting of two series connected latches that are clocked out of phase 180°. To generate the $f_{clk}/2$ frequency division, the differential output of the flip-flop is inverted and connected to the input such that the circuit changes state on the rising edge of the clock cycle. Because M-S flip-flops are utilized as retiming elements for data synchronization,

their maximum toggle rate often sets a limit for circuit bandwidth. Amongst the aforementioned processes, static frequency dividers with an operating $f_{clk} >$ 150 GHz [2], [3], [5], [6] have been demonstrated. The flip-flop operating power associated with these circuits varies from 400 to 600 mW, with a corresponding power-delay product of $\sim$ 800 fJ/latch.

In this work, current mode logic (CML) designs were pursued with the intent of reducing to a minimum the required supply voltage and operating currents within the circuit, and investigating the maximum divider toggle rate associated with this bias. Circuits were fabricated employing regular mesa HBTs, as well as collector pedestal HBTs for reduced base-collector capacitance C_{cb} and hence increased circuit bandwidth. From these designs, a pedestal-HBT based divide-by-2 static frequency divider has been demonstrated, operating from f_{clk} = 4 GHz to $f_{clk,max}$ = 61.2 GHz while dissipating 27.1 mW of power in the flip-flop from a single -2.30 V supply. The power-delay product of this circuit is 113.0 fJ/latch if all devices in the latch are considered (Fig. 1, Q$_1$-Q$_4$), and 63.2 fJ/latch if the power associated with the voltage level-shifting emitter followers is not included in the power-delay calculation (Fig. 1, Q$_1$-Q$_3$ only). The same circuit employing regular mesa HBTs demonstrated only an $f_{clk,max}$ = 51.0 GHz, a bandwidth difference of 20%. By either method of calculation, this is a record low power-delay product for an InP DHBT-based static frequency divider; more than 2$\times$ lower than has been previously reported [7]. The circuits reported here employ the current mode logic (CML) topology and inductive peaking. Note, that as reported in [7], the total power measured for the three flip-flops of the divide-by-8 circuit is averaged; however, the input divider operating at the highest frequency consumes 30% more power than the subsequent stages. Furthermore, [7] does not include the voltage level-shifting emitter followers Q$_4$ as part of the flip-flops' power – instead this power is considered as a separate level-shifter, not part of the flip-flop, where 80 mW is consumed amongst the three flip-flops of
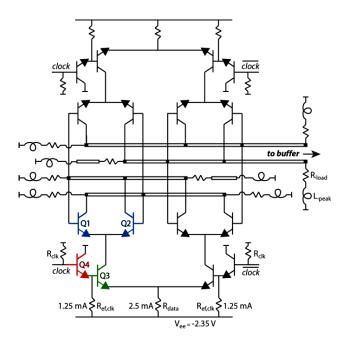
Fig. 1. Schematic of the static frequency divider, w/ bias conditions ΔV_{logic} = 250 mV, R_L = 100 Ω, and L_{peak} = 62 pH

	units	Q1, Q2	Q3	Q4
A_{je}	μm^2	0.5 $\times$ 2	0.5 $\times$ 2	0.5 $\times$ 2
I_c	mA	2.5	2.5	1.25
V_{cb}	V	-0.25	0.0	0.4
C_{cb}/I_c	ps/V	3.40 / 3.08	2.17 / 1.97	3.74 / 3.58
f_τ	GHz	164 / 242	225 / 291	179 / 233
f_{max}	GHz	142 / 201	225 / 310	220 / 337

in [1], while details of the collector pedestal process have been reported in [8], [9]. Thin-film dielectric (Benzocyclobutene, 3 μm thick) microstrip wiring is employed for its predictable characteristics, controlled impedance, and ability to maintain signal integrity at high frequencies within dense mixed-signal ICs. The ground plane formed from the top most layer of metal also eliminates signal coupling through on-wafer ground-return inductance.
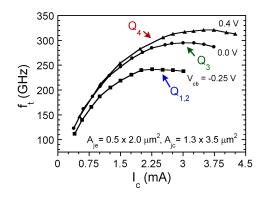
III. DEVICE AND CIRCUIT MEASUREMENTS

RF device measurements were performed on the same sized HBT (regular mesa and collector pedestal) employed in the circuits (Fig. 1), and the results are summarized in Table I – listing the respective operating I_c, V_{cb}, C_{cb}/I_c, f_τ, and f_{max} for the devices. Figures 2 and 3 show the variation of f_τ and f_{max}, and C_{cb} with I_c and V_{cb}, respectively. The device data shows that the HBTs from the circuit Q_1, Q_2, and Q_3 operate at a bias close to peak bandwidth and minimum C_{cb}/I_c ratio. Device Q_4 however is operated at a much lower I_c because its current does not directly contribute to the logic operation.
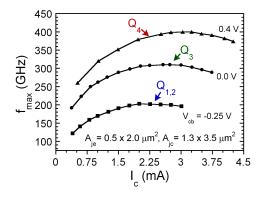
Divide-by-2 circuit measurements for clock frequencies ranging from 4.0 to 61.2 GHz were performed at room temperature, 25°C. At low frequencies, a DC-40 GHz frequency synthesizer directly drives the clock input without the use of an input differential driver. The dividers were clocked as low as 4 GHz to demonstrate that they are fully static in nature. For higher frequency measurements, the synthesizer drives a 50-75 GHz frequency tripler whose output is delivered on-wafer with a WR-15 wafer probe.

For both the regular mesa and collector pedestal HBT divider circuits, as the toggle rate approaches $f_{clk,max}$ (the maximum toggle rate), the emitter followers Q_4 have begun operating into cutoff – $I_{Q4} \sim 0$ mA for half the clock cycle. Consequently, the bias must be adjusted to increase I_{Q4} in order to increase the circuit bandwidth a bit further to $f_{clk,max}$.

The maximum clock rate achievable by the regular mesa HBT divider is 51.0 GHz. At this toggle rate, the flip-flop consumes 29.2 mW (the signal restoration buffers are

the divide-by-8. Based on this data reported within the manuscript text of [7], the claims made by the authors here of a 2× lower power-delay product compared to [7] are accurate.

II. DESIGN AND FABRICATION

A circuit diagram of the CML divider is shown in Figure 1. The logic signal on the data bus ΔV_{logic} is 250 mV and the effective loading resistance R_{load} is 100 Ω, (200 Ω∥200 Ω) – I_{data} = 2.5 mA. Peaking inductance L_{peak} = 62 pH is utilized in series with R_{load} to shorten the data transition time on the interconnect bus. In order for the divider to simulate accurately, the voltage level-shift emitter follower devices (Fig. 1, Q_4) required a minimum I_{Q4} = 1.25 mA. This current is responsible for biasing Q_4 as well as providing current to Q_3 during switching (stored charge and capacitive current). For the given circuit bandwidth that is desired, if I_{Q4} is not made large enough, then cutoff operation of Q_4 will limit divider bandwidth, not delays associated with the data bus. The HBTs within the circuit are sized to the smallest yieldable emitter junction dimensions 0.5 $\times$ 2.0 μm^2; consequently, the HBTs at the data level (Q_1, Q_2, Q_3) are operated at a bias near their peak bandwidth.

Devices from the collector pedestal HBT wafer and regular mesa HBT wafer employ a 120 and 150 nm thick collector respectively, and they are formed utilizing advanced fabrication techniques intended to yield circuits in this material system having > 10,000 devices. Details of the process from Rockwell Scientific have been reported

(a) Variation of f_τ with I_c and V_{cb}

(b) Variation of f_{max} with I_c and V_{cb}

Fig. 2. f_τ and f_{max} of the HBTs within the 61.2 GHz divider

(a) Variation of C_{cb} for the regular mesa HBTs, employed by the 51.0 GHz divider

(b) Variation of C_{cb} for the pedestal HBTs, employed by the 61.2 GHz divider

Fig. 3.   Variation of C_{cb} with I_c and V_{cb} bias, labeled to show the corresponding device switching endpoints within the CML divider schematic (Fig. 1). Lines connecting the switching endpoints have been superimposed to act as a guide.

Fig. 4.   Output waveform of the collector pedestal HBT based divide by 2 circuit at 30.6 GHz, $f_{clk,max}$ = 61.2 GHz.
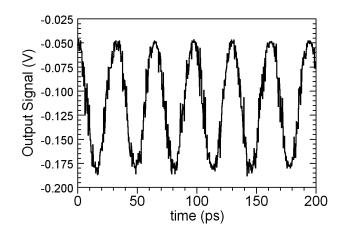
not included), corresponding to a power delay product of 143.0 fJ/latch if all devices in the latch (Q_1 - Q_4) are considered, and 77.9 fJ/latch if the power associated with the voltage level-shifting emitter followers (Q_4) is not included in the power-delay calculation. Table II summarizes the bias conditions and power-delay product as the divide-by-2 approaches $f_{clk,max}$.

The maximum clock rate achievable by the collector pedestal HBT divider is 61.2 GHz (fig. 4). At this toggle rate, the flip-flop consumes 27.1 mW (the signal restoration buffers are not included), corresponding to a power delay product of 113.0 fJ/latch if all devices in the latch (Q_1 - Q_4) are considered, and 63.2 fJ/latch if the power associated with the voltage level-shifting emitter followers (Q_4) is not included in the power-delay calculation. Table III summarizes the bias conditions and power-delay product as the divide-by-2 approaches $f_{clk,max}$. Note, for all of the bias conditions listed in Tables II and III, the dividers are operational from $f_{clk,max}$ down to 4 GHz.
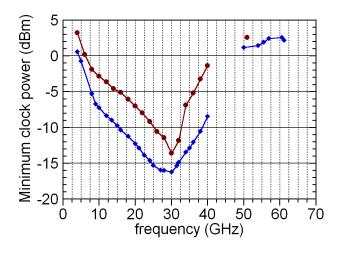
Fig. 5. Variation of input power sensitivity w/ frequency for the 61.2 GHz collector pedestal (diamonds) and 51.0 GHz regular mesa (circles) CML static dividers. The self-oscillation frequency for both circuits is 30 GHz.

TABLE II

SUMMARY OF THE BIAS CONDITIONS AND POWER-DELAY-PRODUCT (PDP) AS THE REGULAR MESA HBT BASED DIVIDE-BY-2 APPROACHES $f_{clk,max}$

clk	V_{ee}, V	I_{tot}, mA	I_{latch}, mA	PDP/latch, fJ
48.0	-2.385	34.2	4.95 / 2.15	123.0 / 53.4
50.1	-2.373	34.9	5.30 / 2.50	125.5 / 59.2
51.0	-2.371	36.6	6.15 / 3.35	143.0 / 77.9
GHz	—-	—	Q_1-Q_4/Q_1-Q_3	Q_1-Q_4/Q_1-Q_3

IV. CONCLUSION

Static frequency dividers operating from 4.0 to 61.2 GHz while only consuming $\sim$ 27.1 mW of power have been demonstrated in an InP/InGaAs DHBT technology utilizing C_{cb} reduction techniques, through the use of a collector pedestal process. This is the first digital circuit reported employing such C_{cb} reductions techniques in this material system and they are responsible for the observed 20% increase in maximum toggle rate compared to the same circuit employing a regular mesa HBT structure. The power-delay product of this circuit is 113 fJ/latch; more than 2× lower than has been previously reported by such circuits employing InP DHBTs. The circuit performance reported here is limited not by delays from the data bus, but more so due to the small value of current used to bias the voltage level-shifting emitter followers Q_4 and them operating into cutoff at $f_{clk,max}$.

ACKNOWLEDGMENT

TABLE III

SUMMARY OF THE BIAS CONDITIONS AND POWER-DELAY-PRODUCT (PDP) AS THE COLLECTOR-PEDESTAL HBT BASED DIVIDE-BY-2 APPROACHES $f_{clk,max}$

clk	V_{ee}, V	I_{tot}, mA	I_{latch}, mA	PDP/latch, fJ
60.0	-2.195	29.9	4.95 / 2.40	90.5 / 43.9
60.6	-2.273	31.5	5.25 / 2.65	99.4 / 50.2
61.2	-2.299	32.8	5.90 / 3.30	113.0 / 63.2
GHz	—-	—	Q_1-Q_4/Q_1-Q_3	Q_1-Q_4/Q_1-Q_3

REFERENCES

[1] M. Urteaga, P. Rowell, R. Pierson, B. Brar, M. Dahlström, Z. Griffith, M. J. W. Rodwell, S. Lee, N. Nguyen, and C. Nguyen, "Deep submicron InP DHBT technology with electroplated emitter and base contacts", *Proc. Device Research Conference*, Notre Dame, IN, pp. 239-240, June 21-23, 2004.

[2] D. Sawdai, P.C. Chang, V. Gambin, X. Zeng, J. Wang, M. Barsky, B. Chan, B. Oyama, A. Gutierrez-Aitken, and A. Oki, "Veritcal scaling of planarized InP/InGaAs heterojunction bipolar transistors with $f_\tau > 350$ GHz and $f_{max} > 500$ GHz", *Proc. IEEE Int. Conf. on Indium Phosphide and Related Materials*, Glasgow, Scotland, pp. 335-338, May 8-13, 2005.

[3] M. Le, G. He, R. Hess, P. Partyka, B. Li, R. Bryie, S. Rustomji, G. Kim, R. Lee, J. Pepper, M. Helix, R. Milano, R. Elder, D. Jansen, F. Stroili, J.-W. Lai, M. Feng, "Self-aligned InP DHBTs for 150 GHz digital and mixed signal circuits" *Proc. IEEE Int. Conf. Indium Phosphide and Related Materials*, Glasgow, Scotland, pp. 325-330, May 8-13, 2005.

[4] J. Zolper, "Challenges and opportunities for InP HBT mixed signal circuit technology", *Proc. IEEE Int. Conf. Indium Phosphide and Related Materials*, Santa Barbara, CA, pp. 8-11, May 12-16, 2003.

[5] Z. Griffith, M. Dahlström, M. J. W. Rodwell, M. Urteaga, R. Pierson, P. Rowell, B. Brar, S. Lee, N. Nguyen, and C. Nguyen, "Ultra high frequency static dividers > 150 GHz in a narrow mesa InGaAs/InP DHBT technology", *IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, Montreal, Canada, pp. 176-179, September 13-14 , 2004.

[6] D.A. Hitko, T. Hussain, J.F. Jensen, Y. Royter, S. Morton, D.S. Matthews, R.D. Rajavel, I. Milosavljevic, C.H. Fields, S. Thomas III, A. Kurdoghlian, Z. Lao, K. Elliott, M. Sokolich, "A low power (45 mW/latch) static 150 GHz CML divider", *Proc. IEEE Compound Semiconductor Integrated Circuit Symposium*, Monterey, CA, October 24-27, 2004.

[7] T. Hussain, D.A. Hitko, Y. Royter, R.D. Rajavel, K. Elliot, K. Mc-Calla, M. Madhav, and M. Sokolich, "Low power (51 mW per flip-flop) CML static divider implemented in scaled 0.25 μm emitter-width InP DHBTs", *Proc. IEEE Int. Conf. Indium Phosphide and Related Materials*, Glasgow, Scotland, pp. 347-350, May 8-12, 2005.

[8] Y. Dong, Z. Griffith, M. Dahlstrm, and M.J.W. Rodwell, "C_{cb} Reduction in InP Heterojunction Bipolar Transistor with Selectively Implanted Collector Pedesta", *Proc. IEEE Device Research Conference*, Notre Dame, IN, pp. 67-68, June 21-23, 2004.

[9] N. Partharasarathy, Z. Griffith, C. Kadow, U. Singisetti, M.J.W. Rodwell, X.-M Fang, D. Loubychev, Y. Wu, J.M. Fastenau, and W.K. Liu, "Collector-pedestal InGaAs/InP DHBTs fabricated in a single-growth, triple-implant process", *IEEE Electron Device Letters*, vol. 27, no. 5, May 2006.