Regrown-Emitter InP HBTs

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ABSTRACT

We present the MBE growth and the DC device performance of the first fully epitaxial regrown-emitter InP HBTs. Here the emitter layers are regrown by MBE onto a patterned base-collector template. This process is aimed at reducing the emitter resistance, a key parameter for scaling high speed logic circuits. Emitter resistance is reduced because the emitter contact is formed to an extrinsic emitter larger than the base-emitter junction. SEM images demonstrate controlled, uniform etching to the intrinsic base layer, high-quality epitaxial MBE growth onto the patterned surface, and good sidewall coverage. HBTs with base-emitter junctions ranging from 48x48 μm^2 to 2.5x2.5 μm^2 have DC current gains between 5.0 and 7.5. Comparison to regular HBTs shows that the DC current gains are limited by base leakage currents. The contributions to the base leakage currents are discussed. TLM measurements show that low emitter resistance and low base resistance are feasible in this regrown-emitter HBT technology.

I. INTRODUCTION

Continued transistor scaling is needed for increased bandwidth of high clock-rate logic and high-frequency analog applications [1, 2]. Emitter-regrowth may provide a solution to the present limits associated with scaling InP HBTs to 0.25 µm base-emitter junctions and simultaneously reducing the emitter resistance R_{ex}. Excessive R_{ex} degrades digital circuit performance because a fraction of the logic swing drops across R_{ex}. When HBTs are scaled to operate at twice their bandwidth at the same bias current, the base-emitter junction area needs to be reduced by a factor of four and R_{ex} needs to stay constant [2]. Hence the specific emitter resistance, ρ_{ex}, needs to be reduced by a factor of four. Presently R_{ex} is dominated by the contact resistance $\rho_{ec} \approx 10\ \Omega\text{-}\mu m^2$. This value is twice as large as permissible for 200 GHz clock rate logic. Emitter-regrowth reduces R_{ex} by forming an emitter contact wider than the emitter-base junction as schematically shown in Figure 1.

Emitter regrowth techniques have been demonstrated in GaAs HBTs to address scaling limits [3]. In SiGe HBT technology epitaxial regrowth techniques are also used to deposit the emitter layers onto patterned substrates [4]. For InP HBTs, the only prior work on emitter regrowth has focused on polycrystalline InAs [5, 6, 7]. Here we present the first fully epitaxial regrown-emitter InP HBTs.

II. TRANSISTOR DESIGN

Figure 1 shows a schematic cross-section of the regrown-emitter HBT. The layer structure is given in Table I. The base-collector template is grown first (layers 5 to 18 in Table I). The 150 nm InP collector and the 30 nm intrinsic InGaAs base are similar to previous designs with proven RF performance [8, 9]. Two new layers, the extrinsic base and the current barrier layer,

are grown on top of the intrinsic base layer. The extrinsic base serves as a highly conductive link between the intrinsic base and the base contact. Heavy p-type doping is desirable to allow for low extrinsic base sheet resistance and for low base contact resistance. In this initial work both extrinsic and intrinsic base were doped at N_A = 3x10^{19} cm^{-3}. The current barrier layer provides electrical isolation between the extrinsic base and the emitter. An InP/InAlAs multilayer was used to simultaneously block hole injection from the base into the emitter by the valence band offset of 370 meV between InP and InGaAs, and electron injection from the emitter into the base by the conduction band offset of 270 meV between InP and InAlAs. After growth of the base-collector template, the emitter window is etched through the current barrier and the extrinsic base layers. The emitter window etch defines the base-emitter junction width, W_E. In the second growth step, the emitter layers are grown onto this patterned substrate (Layer 1 to 4 in Table I). Removing the surface oxide is critical for the nucleation of epitaxial regrowth. The InGaAs cap of the base-collector template provides the same surfaces on top of the intrinsic InGaAs base and on top of the current barrier. Because one cannot rely on thermally desorbing the oxide on InAlAs, the base-collector template was designed such that InAlAs is only exposed on the sidewall of the emitter window. An abrupt InP emitter with an InGaAs cap similar to previous designs was chosen [8, 9]. The use of the binary compound InP simplifies the initial stages of the regrowth. After emitter-regrowth the transistor fabrication proceeds in the usual manner.

As mentioned earlier, the R_{ex} reduction in this structure is due to reducing the emitter contact resistance by forming an emitter contact wider than the base-emitter junction. To take full advantage of the wider emitter contact, the sheet resistance in the emitter layers, ρ_{esh}, needs to be so low that the transfer length, W_T, exceeds the width of the wing regions, W_L: $W_T = \sqrt{\rho_{ec}/\rho_{esh}} >> W_L$. Because the emitter regrowth is fully epitaxial, highly conductive

materials such as n^{++} InP and n^{++} InGaAs are available in contrast to our previous work on polycrystalline emitter regrowth [7]. For doping levels of $N_D = 2\text{x}10^{19}$ cm^{-3} in InGaAs and InP, Hall measurements on separate samples show electron mobilities of 1,900 cm^2/V-s and 600 cm^2/V-s, respectively. Therefore $\rho_{esh} = 20$ Ω/sq. is expected in this layer structure. With $\rho_{ec} =$ 10 Ω-μm^2, $W_T = 0.7$ µm.

In addition to lowering R_{ex}, regrown-emitter HBTs have the following advantages: Higher millimeter-wave power-gain is expected because the base resistance, R_{bb}, is low due to the thick extrinsic base. Integration of emitter regrowth into standard HBT circuit fabrication is possible because after emitter mesas are formed, device fabrication can proceed in the usual fashion. The wide emitter contact allows to use today's emitter interconnect schemes for narrow emitter-base junction. Improved yield and reliability are expected from the fully buried base-emitter junction. Device failures from base-collector shorts due to the base contact metal diffusing through the base are avoided by the thick extrinsic base.

III. DEVICE FABRICATION

Both the base-collector template and the emitter were grown at UCSB on the same Gen III MBE reactor. During growth the RHEED pattern and the temperature were monitored. The temperature was measured with a pyrometer facing the wafer. The base-collector template was grown on a semi-insulating Fe-doped InP substrate. After oxide desorption, layers 5 to 18 in Table I were deposited. All layers were grown at 480°C.

The InGaAs cap, the InAlAs/InP current barrier and the InGaAs extrinsic base were removed by a series of selective wet etches in the emitter windows. Wet-chemical etching rather than dry etching was used to avoid damage to the exposed surfaces. Part (a) of Figure 2 shows an SEM

image of a cleaved cross-section through a process test sample. The etch depth is uniform across the emitter window. During etching of the extrinsic base, the current barrier was undercut laterally by 100 nm, the thickness of the extrinsic base, resulting in the formation of a ledge. On the top of the ledge, the InGaAs cap layer was removed during etching and the InP layer underneath was exposed. The lateral extend of the emitter window edge was below 200 nm. A narrow edge region improves the quality of the regrowth and is needed for submicron scaling. After loading the samples into the MBE reactor, the surface oxide was desorbed by heating the sample to 490°C. Then the emitter layers in Table I were grown at 480°C. The RHEED pattern was streaky before the initiation of growth. Upon nucleation of InP, the RHEED pattern became spotty, indicating roughness. The pattern became streaky again within the first 50 Å of growth. After emitter regrowth transistors were fabricated by wet-etching the emitter mesa, wet-etching the base-collector mesa and finally depositing one Pd/Ti/Pd/Au metal layer. The metal layer was used for ohmic contacts to the three transistor terminals and for probe pads.

The SEM image in part (b) of Figure 2 shows a cleaved cross-section through a device with a 2.5 μm wide base-emitter junction. In the SEM images, InGaAs and InAlAs appear light gray and InP appears dark gray. The contact metal appears white. In the center of the image are the intrinsic HBT layers. The thickness of the intrinsic base is uniform across the transistor. The regrown emitter layers appear to be of high quality. The extrinsic base and the current barrier can be seen as well. The sidewalls of the emitter window are covered very well by the regrown emitter layers. The undercut is filled completely by the regrown material. The dark spot on the current barrier layer is believed to be a small void due to oxidized InAlAs. Such small voids were observed in half of the device cross-sections. In about 5% of the SEM images larger voids were seen. These larger voids extend from the sidewall of the emitter window upwards to the top

of the emitter. We believe these extended voids are only formed if the top of the InAlAs layer (Layer 7 in Table I) is not covered by the InP layer above it. We expect to eliminate the large voids by improved emitter window etching.

IV. DEVICE PERFORMANCE

DC common-emitter measurements were performed on devices with square-shaped emitter junctions with side length between 48 µm and 2.5 µm. All transistors had 60x60 μm^2 emitter mesas and 54x54 μm^2 emitter contacts. All measured devices were functional with DC current gains, β, between 5.0 and 7.5. Output characteristics for a 5x5 μm^2 base-emitter junction are shown in Figure 3. Gummel data of this device is shown in Figure 4. The collector current, I_c, exceeds the base current, I_b, for base-emitter voltages, V_{be}, greater than 0.5 V. The maximum β for this device was 7.5. The ideality factor for the collector current is $n_c = 1.1$. The base current anomalies at low V_{be} are discussed below. Regular mesa HBTs were grown and fabricated for comparison. These HBTs have the same active device layers as the regrown-emitter HBTs in the intrinsic region. Figure 4 also shows Gummel data of the regular HBT. In the regular HBT, I_b was smaller than I_c at all V_{be} in contrast to the regrown-emitter HBT. The maximum β was 70. Base and collector ideality factors were $n_b = 1.3$ and $n_c = 1.1$, respectively.

The lower current gain of the regrown-emitter HBT is due to high base leakage currents. At V_{be} below 0.2 V we observe a negative differential resistance. At V_{be} above 0.2 V, I_b first varies exponentially with an ideality factor $n_b = 2.4$, then layout-related base resistance limits I_b. Potential leakage mechanisms unique to the regrown-emitter HBTs include: leakage through the current barrier layer, lateral injection into the extrinsic base, and defect-related currents due to the regrown interface. To evaluate leakage through the current barrier layer, base-emitter

junctions without an emitter window were fabricated on the sample. Figure 5 compares data for one of these junctions to a base-emitter with a 40x40 μm^2 emitter window. Under operating conditions, 0.5 V < V_{be} < 1.2 V, the current density in the junction without an emitter window is at least a factor of 500 smaller than in the junction with an emitter window. This demonstrates the effectiveness of the current barrier layer and rules out leakage through the current barrier as the primary leakage mechanism. Injection into the extrinsic base has not yet been addressed experimentally. In future devices we intend to generate an energy barrier to injection into the extrinsic base by doping the extrinsic base more heavily than the intrinsic base. Because the valence band is degenerately doped, the higher doping of the extrinsic base results in a later turn-on of the extrinsic base emitter junction than the intrinsic base emitter junction. For doping levels of $N_A = 1x10^{20}$ cm^{-3} in the extrinsic base and for $N_A = 3x10^{19}$ cm^{-3} in the intrinsic base, we expect an energy barrier of 84 meV. Assuming a slope of 60 mV/dec, we predict the current density injected into the extrinsic base will be 26 times smaller than the current density injected into the intrinsic base.

The fabricated devices are too large to measure R_{ex}. In agreement with the design, TLM measurements show that the emitter contact resistance, ρ_{ec} equals 10 Ω-μm^2, the emitter sheet resistance, ρ_{esh} equals 22 Ω/sq. and that the transfer length, W_T equals 0.7 µm. Hence with this layer structure and $W_L = W_E = 0.25$ µm, a threefold reduction to the emitter contact resistance is feasible.

In a separate experiment, base-collector templates with a more complex base doping profile were grown by IQE, Inc.: The doping of the 1000 Å InGaAs extrinsic base was $N_A = 1x10^{20}$ cm^{-3}. The doping of the 300 Å InGaAs intrinsic base was graded from $N_A = 4.5x10^{19}$ to $1.5x10^{19}$ cm^{-3}. Base TLM measurements on this sample show that the sheet resistance of the entire base, extrinsic and

intrinsic base in parallel, is 130 Ω/sq. This is an eightfold improvement over the sheet resistance of a 300 Å InGaAs base doped at $3x10^{19}$ cm^{-3}.

V. SUMMARY

In conclusion, we have experimentally demonstrated the first fully epitaxial regrown-emitter InP HBTs. SEM images show a controlled and uniform etch to the intrinsic base and high-quality epitaxial regrowth onto the patterned substrate with good sidewall coverage. Transistors with base-emitter junctions ranging from 48x48 μm^2 to 2.5x2.5 μm^2 were measured. These devices were functional and showed DC current gains between 5.0 and 7.5. Comparison to regular HBTs show that base leakage currents limit the DC current gain of the regrown-emitter HBTs. Leakage through the current barrier was ruled out because under operating conditions the current density flowing through the current barrier is at least 500 times smaller than the current density flowing across the intrinsic base-emitter junction. Emitter TLM data show that a threefold reduction of the effective emitter contact resistance is feasible for a 0.25 μm base-emitter junction with a 0.75 μm wide emitter contact. Base TLM data on separate samples show that intrinsic and extrinsic base regions with sheet resistances as low as 130 Ω/sq. are feasible.

VI. ACKNOWLEDGEMENTS

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REFERENCES

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[1] J. Zolper, Proc. IEEE International Conference on Indium Phosphide and Related Materials, Santa Barbara, CA, 12 (2003)

[2] M.J.W. Rodwell et al., Int. J. High-Speed Electron. Syst. 11, 159 (2001)

[3] S.H. Park, T.P.Chin, Q.Z. Liu, S.L. Fu, Nakamura, P.K., P.K.L. Yu, and P.M. Asbeck, IEEE Electron Device Lett. 19, 118 (1998).

[4] B. Jagannathan et al., IEEE Electron Device Lett. 23, 258 (2002).

[5] D.W. Scott, Y. Wei, Y. Dong, A.C. Gossard, and M.J. Rodwell, IEEE Electron Device Lett. 25, 360 (2004).

[6] Y. Wei, D.W. Scott, Y. Dong, A.C. Gossard, and M.J. Rodwell, IEEE Electron Device Lett. 25, 232 (2004).

[7] D.W. Scott, C. Kadow, Y. Dong, Y. Wei, A.C. Gossard, and M.J.W. Rodwell, J. Crystal Growth 267, 35 (2004).

[8] Z. Griffith, M. Dahlström, M. Urteaga, M.J.W. Rodwell, X.-M. Fang, D. Lubyshev, Y. Wu, J.M. Fastenau, and W.K. Liu, IEEE Electron Device Lett 25, 250 (2004).

[9] Z. Griffith, M. Dahlström, M.J.W. Rodwell, X.-M. Fang, D. Lubyshev, Y. Wu, J.M. Fastenau, and W.K. Liu, submitted to IEEE Electron Device Lett.

TABLE AND FIGURE CAPTIONS

Table I: Layer structure of the regrown-emitter InP HBT. Layers 5 to 18 are the base-collector template. Layers 5 to 10 are removed in the intrinsic HBT by the emitter window etch. Layers 1 to 4 are regrown onto the patterned substrate. The InGaAs and InAlAs layers are lattice-matched to InP.

FIG. 1: Schematic cross-section through a regrown-emitter InP HBT. The detailed layer structure is given in Table I. In this structure R_{ex} is reduced because the emitter contact is $2 \cdot W_L$ wider than the base emitter junction width W_E.

FIG 2: (a) SEM image of a cleaved cross-section through the emitter window. The sample is a process test sample viewed at an angle of 60°. (b) SEM image of a cleaved cross-section through the regrown-emitter HBT. InP appears dark gray; InGaAs and InAlAs appear light gray. The emitter contact metal appears white.

FIG 3: Common-emitter output characteristics of a regrown-emitter HBT with a base-emitter junction area of 5x5 μm^2.

FIG 4: Comparison of the Gummel characteristics of the same regrown-emitter HBT as in Figure 4 to a regular HBT. The current axes are offset by two orders magnitude for clarity; I_b and I_c of the regrown-emitter HBT (circles) are on the left axis; I_b and I_c of the regular HBT (triangles) on the right axis.

FIG 5: Comparison of the base-emitter currents for two devices, one without an emitter window and the other with a 40x40 μm^2 emitter window. Both mesas are 60x60 μm^2. The current through the current barrier is 2 to 3 orders of magnitude smaller than the current through the emitter window for V_{be} between 0.0 V and 1.2 V.

TABLE I

Layer Number	Thickness [Å]	Material	Doping [cm^{-3}]	Description
1.	400	InGaAs	2E19:Si	Emitter
2.	1400	InP	2E19:Si	Emitter
3.	200	InP	8E17:Si	Emitter
4.	500	InP	5E17:Si	Emitter
5.	100	InGaAs	undoped	Cap
6.	100	InP	undoped	Current Barrier
7.	400	InAlAs	undoped	Current Barrier
8.	100	InP	undoped	Current Barrier
9.	1000	InGaAs	3E19:C	Extrinsic Base
10.	20	InAlAs	3E19:C	Etch Stop
11.	300	InGaAs	3E19:C	Intrinsic Base
12.	200	InGaAs	5E16:Si	Setback
13.	240	InGaAs/ InAlAs	5E16:Si	Base-Collector Grade
14.	30	InP	3E18:Si	Delta doping
15.	1030	InP	5E16:Si	Collector
16.	100	InP	2E19:Si	Subcollector
17.	100	InGaAs	2E19:Si	Subcollector
18.	3000	InP	2E19:Si	Subcollector
	Substrate	Fe-doped InP		

FIGURE 1

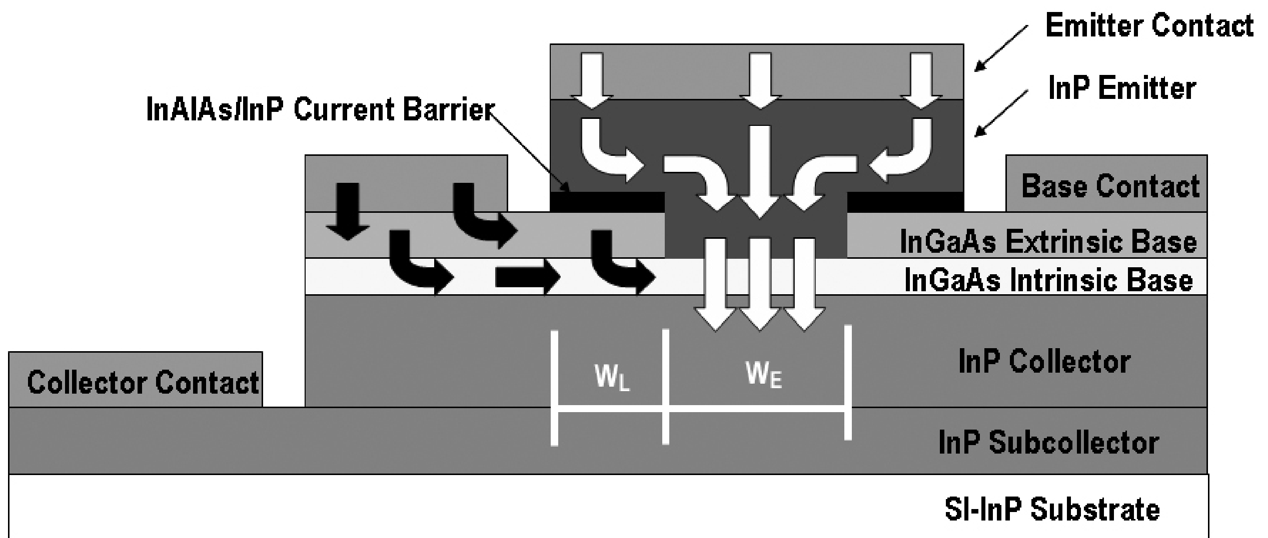

FIGURE 2

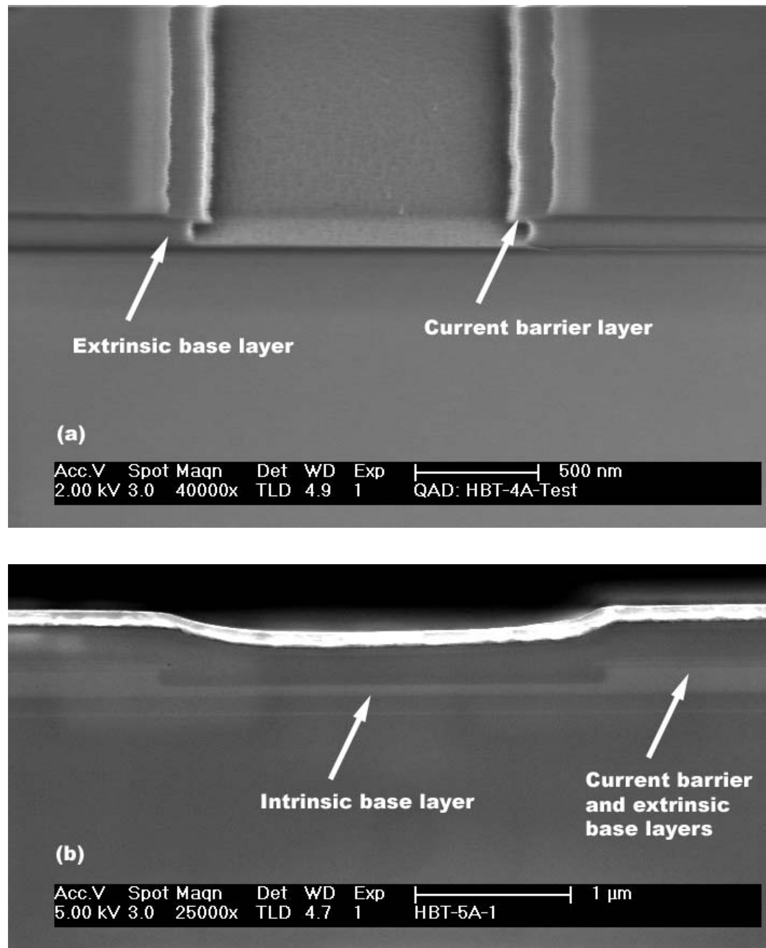

FIGURE 3

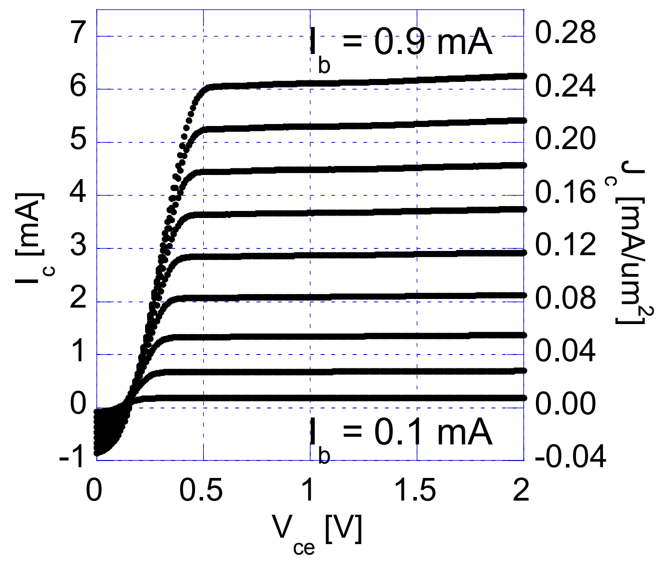

FIGURE 4

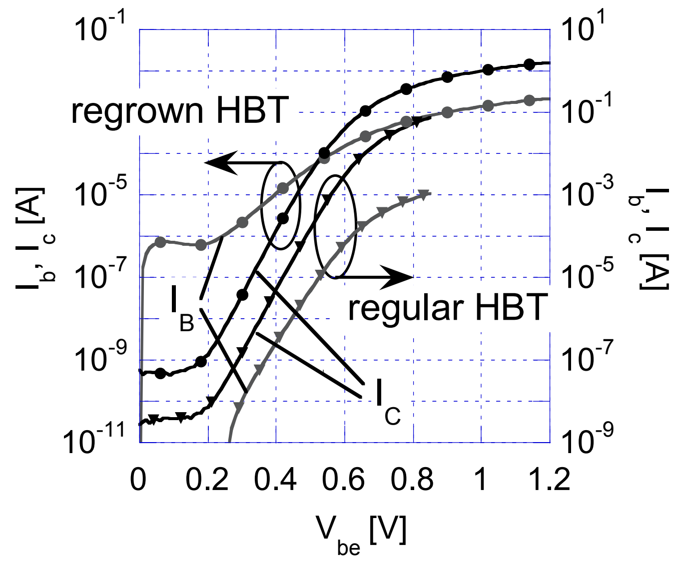

FIGURE 5