An 8-GHz Continuous-Time Σ–Δ Analog–Digital Converter in an InP-Based HBT Technology

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***Abstract*—We report an 8-GHz clock-rate, second-order continuous-time Σ–Δ analog–digital converter (ADC) that achieves 57.4-, 51.7-, and 40.2-dB SNR at signal sampling rates of 125, 250, and 500 Ms/s, respectively. The integrated circuit occupied 1.45-mm^2 die area, contains 76 transistors, is fabricated in an InP-based HBT technology, and dissipates $\sim$ 1.8 W. We also study the effect of excess delay on modulator performance, and show that excess delay does not affect performance as long as the centroid-in-time of the digital–analog converter pulse remains stationary.**

***Index Terms*—Analog-to-digital converter (ADC), continuous time, delta–sigma, HBTs, InP.**

I. Introduction

HIGH-SPEED analog-to-digital converters (ADCs) find widespread applications in wide-band communications and radar receivers. When high sampling rates are feasible, oversampling architectures can be used to obtain high resolution ($>$ 10 bit) at signal sampling rates exceeding 100 Ms/s. One such architecture, based on Σ–Δ modulation achieves high SNR without requiring high precision in component values or device matching.

The SNR of a Σ–Δ modulator depends on the order of the loop filter and the oversampling ratio (OSR) [1]. In order to avoid the stability problems that make the design of higher order ($>$2) loop-filters difficult, and to minimize design-complexity, we use a second-order loop filter in our design. To obtain high resolution, we seek as high a clock rate as is feasible in the technology.

InP-based HBTs have achieved very high device bandwidths [2], permitting very high-speed digital integrated circuits (ICs) [3]. In bipolar processes, fast low-offset switches are difficult to implement, and the continuous-time architecture [4] is more readily implemented than the discrete-time switched-capacitor architecture prevalent in CMOS Σ–Δ ADCs. Continuous-time Σ–Δ modulators have been reported with clock rates as high as 4 [7] and 5 GHz [6]. We had earlier reported a modulator with a clock rate of 18 GHz [14]. This design, though, did not exhibit spectral shaping of the noise for frequencies below 1 GHz. Post-measurement full-loop SPICE simulations revealed that the quantizer output did not rise quickly enough, resulting in a digital–analog converter (DAC) pulse that was in error. This effect manifested itself in the output power spectrum as a whitening of the noise floor at low frequencies [14].

In order to minimize such metastability errors in the quantizer, we have used an additional stage of regeneration [5]. This additional stage introduces excess delay in the loop, and the effect of this delay on ADC resolution is well known [9]–[11] and has been studied in detail [8]. In [8], Cherry and Snelgrove studied the effect of excess delay by considering the equivalence between continuous- and discrete-time Σ–Δ ADCs. Using such an approach, they were able to predict SNR degradation in the presence of excess delay and propose solutions to compensate for the loss in performance. Here, we provide an alternate analysis of SNR degradation in the presence of excess delay. We compare the linear additive-white-noise model's predictions with full-loop MATLAB simulations to show that the simple linear model cannot be used to explain the dynamics of an ADC with a 1-bit internal quantizer. We then proceed to show that the problem can be understood using timing diagrams, and that the loss in SNR can be recovered by monitoring the centroid in time of the DAC pulse, and ensuring that it remains stationary. It is further shown that this can be achieved by using a return-to-zero (RTZ) DAC. We conclude by comparing the measured results of two designs: one with no compensation for excess delay and the other where an RTZ DAC is used to compensate for the excess delay. The ADCs are clocked at 8 GHz.

II. Device Technology

The circuits are fabricated in a triple-mesa process. A description of the HBT process can be found in [2]. Here, we will limit ourselves to a discussion on the wiring environment alone. To realize complex mixed-signal ICs, a wiring environment that maintains control of signal integrity and has predictable characteristics to enable robust computer-aided design (CAD) is required. Thin-film dielectric microstrip wiring provides controlled-impedance interconnects within dense mixed-signal ICs. The associated ground plane eliminates signal coupling through on-wafer ground-return inductance. Such a wiring environment is added to the process with the addition of a dielectric layer and ground plane above the IC top-surface wiring planes. We have implemented this by spin casting a 5-μm-thick benzocyclobutene (BCB) polymer film, etching vias in BCB, and depositing the top ground plane by electroplating. Figs. 1 and 2

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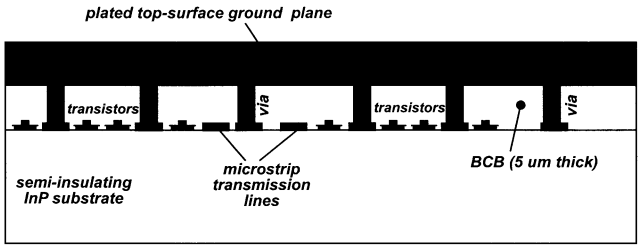

Fig. 1. Cross-sectional view of the microstrip wiring environment.

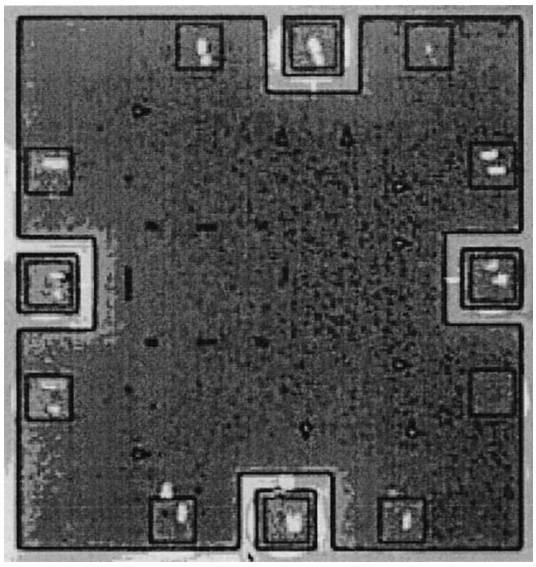

Fig. 2. Top view of the microstrip wiring environment: M–S latch after plating the ground plane.

shows a cross-sectional view of the wiring environment, and an IC micrograph of a master–slave (M–S) latch after ground-plane plating, respectively.

In such a wiring environment, 8- and 3-μm width conductors have controlled 50- and 80-Ω impedances, respectively. Since the dielectric is thin, ground-via inductance is greatly reduced. Interconnects are not significantly coupled for line spacings greater than 10 μm. Ground vias can be closely spaced, as is required in complex ICs. The disadvantage of such a technique is the increase in skin loss compared to a conventional microstrip of similar impedance.

The HBTs are characterized for their dc and RF performance. A device with 0.7×8 μm^2 emitter mask and 1.7×12 μm^2 collector mask dimensions exhibits f_τ, $f_{\max}$, and BV_{CEO} of 205 GHz, 210 GHz, and 6 V, respectively at a current density $J_c = 2.5 \times 10^5$ A/cm^2 and at a bias voltage $\text{V}_{ce} = 1.2$ V.

III. Choice of Σ–Δ Architecture: The Problem of Excess Delay

The most common design procedure for continuous-time Σ–Δ modulators is to start with a discrete-time transfer function that will provide maximum baseband attenuation of quantization noise. The discrete-time transfer function is then transformed to the continuous-time domain to obtain a continuous-time transfer function. For a second-order system,

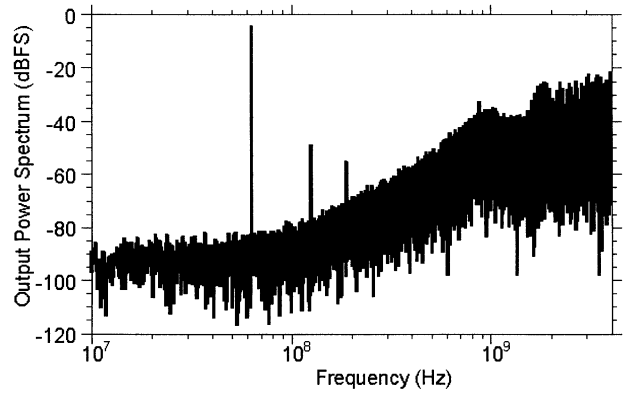

Fig. 3. Linear model in the presence of excess delay in the loop.

it can be shown that the equivalent continuous-time transfer function for the discrete-time filter is given by [8]

$$G(s) = \frac{1 + 1.5sT_s}{s^2 T_s^2} \tag{1}$$

where $T_s = 1/f_s$ represents the sampling time. Any excess delay τ can be represented as $e^{-j\omega\tau}$ in the frequency domain and is simply a multiplying factor in the loop transfer function (Fig. 3).

The noise transfer function in the frequency domain $N(j\omega)$ is given by

$$N(j\omega) = \frac{Y(j\omega)}{E(j\omega)} = \frac{1}{1 + G(j\omega) \cdot e^{-j\omega\tau}}. \tag{2}$$

$|N(j\omega)|^2$ can be simplified to

$$|N(j\omega)|^2 = \frac{\omega^4 \cdot T_s^4}{\left(\omega^2 \cdot T_s^2 \cdot \left(\frac{1-1.5\tau}{T_s}\right) - 1\right)^2 + \omega^2 \cdot (1.5T_s - \tau)^2}. \tag{3}$$

Consider the effect of τ on $|N(j\omega)|^2$ at low frequencies or, in other words, the effect of excess delay on the in-band noise suppression. At low frequencies, the denominator of $|N(j\omega)|^2$ simplifies to its constant term, in this case, unity. Hence, $|N(j\omega)|^2$ simplifies as

$$|N(j\omega)|^2 = \omega^4 \cdot T_s^4 \tag{4}$$

an expression that is independent of the excess delay τ. Hence, a linearized-model-based analysis predicts that excess delay has no effect on the in-band suppression of the quantization noise at low frequencies and, consequently, on the resolution of the ADC at high OSRs. Further, since it is possible to compensate for the excess delay over a wide range of frequencies by introducing a zero with a time constant τ in the loop, one would expect that excess delay would have little or no effect on the SNR over a wide range of signal sampling rates. To verify this, we performed MATLAB simulations on the two circuits, i.e., an ADC with an M–S latch-based quantizer and an ADC with a master–slave–slave (M–S–S) latch-based quantizer, but with the location of the zeros altered to compensate for the excess delay. The circuit block diagram is shown in Fig. 4. The additional stage of regeneration introduces an extra delay of one-half clock

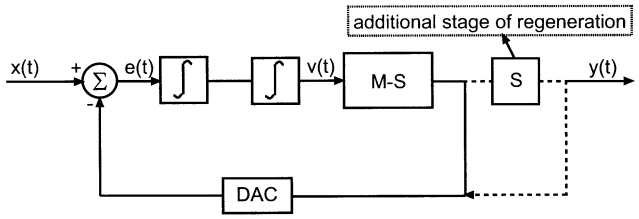

Fig. 4. Circuit block diagram for simulating the effect of excess delay using MATLAB.

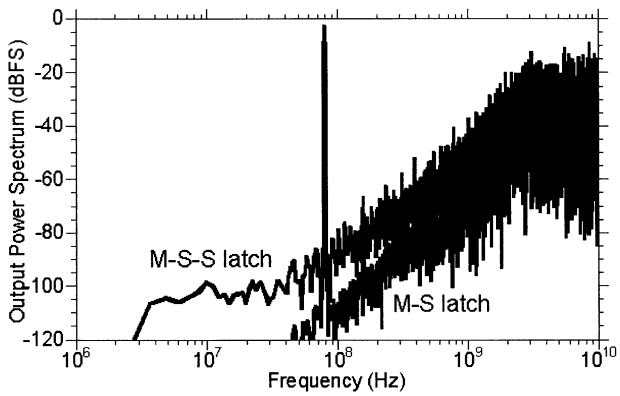

Fig. 5. Simulation result: a comparison of the FFT of the output bit-stream for a MATLAB simulation of a second-order Σ–Δ ADC with an M–S latch-based 1-bit quantizer and a MATLAB simulation of a second-order Σ–Δ ADC with an M–S–S latch-based 1-bit quantizer. $f_{\rm clock} = 20$ GHz, $f_{\rm signal} = 78.125$ MHz, 1.22-MHz FFT bin (resolution).

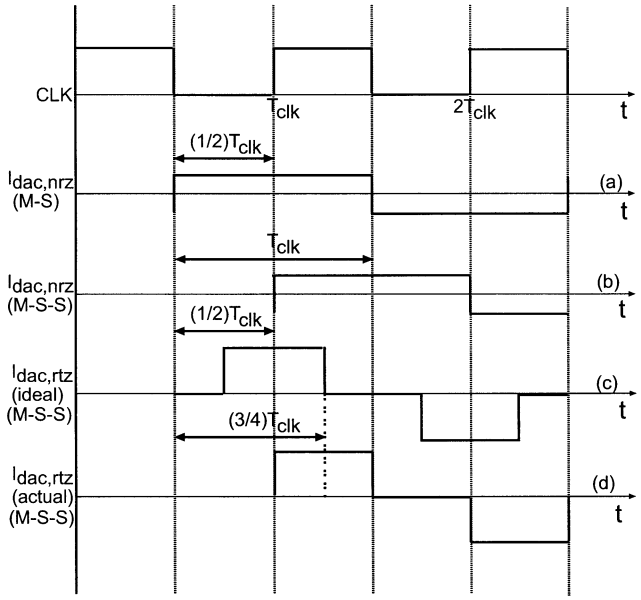

Fig. 6. Variation of the centroid in time of the DAC with choice of quantizer and the nature of the DAC.

cycle (25 ps for a 20-GHz clock) and the zero location in the latter case was chosen to compensate for this excess delay. Fig. 5 compares the results of a full-loop MATLAB simulation for the two cases. The results of the full-loop simulation are inconsistent with the linear model predictions. We observe considerable degradation in SNR in the presence of excess delay in spite of introducing a zero in the loop. For instance, at an OSR of 128, we see $>$ 15 dB SNR degradation between the two cases.

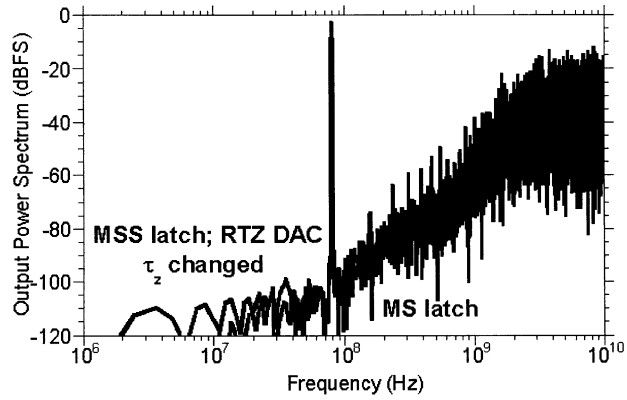

Fig. 7. Simulation result: a comparison of the FFT of the output bit stream of a MATLAB simulation of a second-order Σ–Δ ADC with an M–S latch and an NRZ DAC and a MATLAB simulation of a second-order Σ–Δ ADC with an M–S–S latch and a RTZ DAC with the zero location altered suitably. In both cases, $f_{\rm clock} = 20$ GHz, $f_{\rm signal} = 78.125$ MHz, 1.22-MHz FFT bin (resolution).

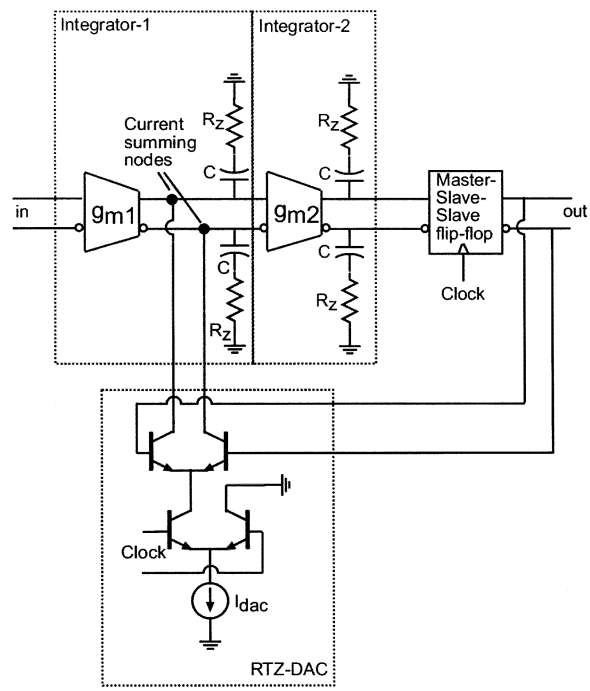

Fig. 8. Simplified block diagram of a second-order continuous time Σ–Δ ADC.

Given the inconsistency between the linear model's prediction and the MATLAB simulation, and the fact that the additive white-noise approximation does not hold for a 1-bit quantizer, we conclude that the linear model cannot be used to explain the dynamics of a modulator with a 1-bit internal quantizer. Instead, we propose a timing-diagram-based approach. Since the quantizer's output depends on its input at the sampling instants, it should be possible to recover the loss in SNR by restoring the quantizer inputs to their original values (i.e., the case where the additional stage of regeneration is absent) at the clock transition. The input to the quantizer at the sampling instant depends on the amount of charge fed back in a given clock cycle and, hence, we will observe no degradation as long as the same amount of charge is fed back in the two cases. Since the clock period is the

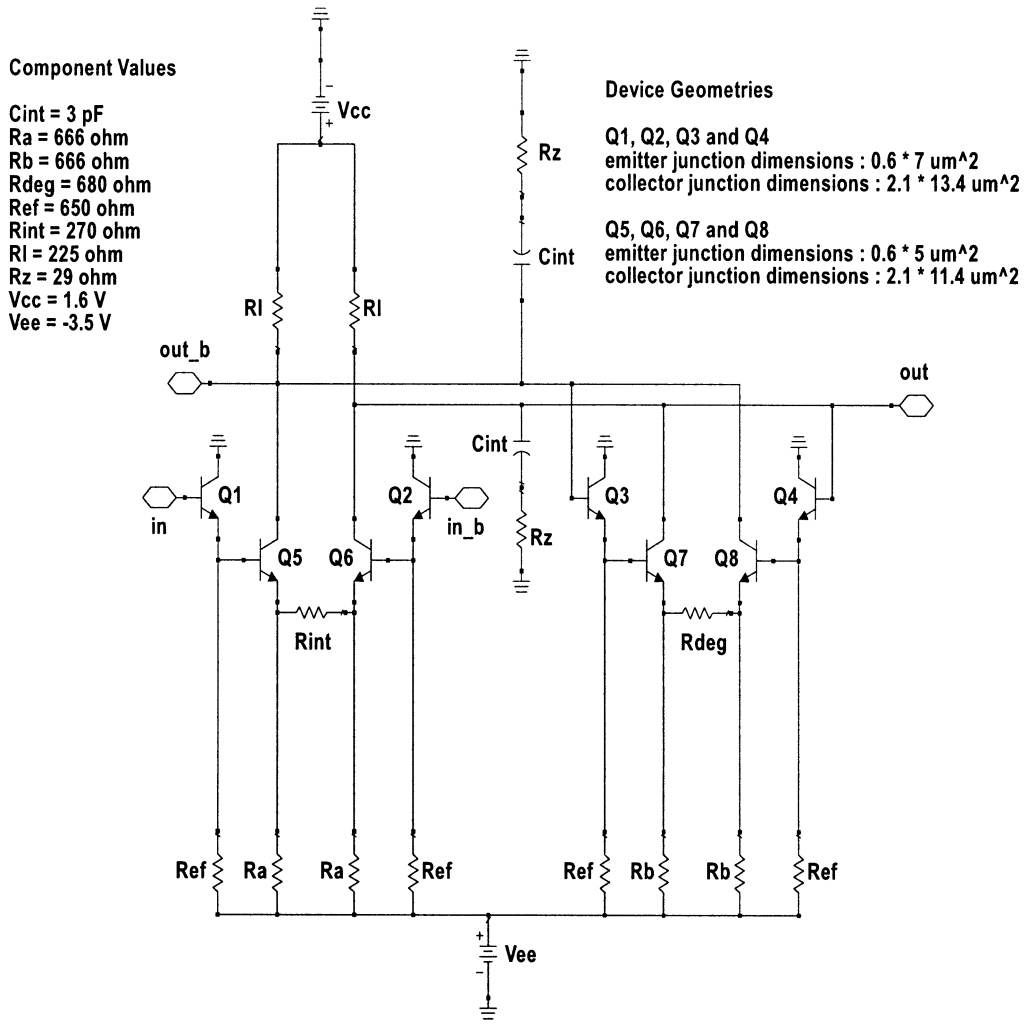

Fig. 9. Circuit schematic of the first integrator.

same in the two cases, this can be achieved by ensuring that the centroid in time of the DAC current pulse is stationary.

Consider the timing diagram shown in Fig. 6. We will use the falling edge of the clock as our reference point and compare the centroids in time for the different cases relative to it. With an M–S latch-based quantizer [see Fig. 6(a)] and a nonreturn to zero (NRZ) DAC, the centroid in time is $T_{\rm clk}/2$ away from the clock transition. With an M–S–S latch-based quantizer [see Fig. 6(b)] and an NRZ DAC, the centroid is $T_{\rm clk}$ from the clock transition. If our arguments hold, we should be able to recover any loss in SNR between cases (a) and (b) using the DAC pulse shown in Fig. 6(c). Such a DAC pulse, though, cannot be realized with an M–S–S latch-based quantizer. With an M–S–S latch-based quantizer, the DAC pulse will have to be a delta function (at $\Delta T = T_{\rm clk}/2$) to maintain the position of its centroid-in-time constant (This observation is consistent with the results obtained in [8].) In order to obtain a reasonable compromise between excess delay and circuit realizability, we use an RTZ DAC [see Fig. 6(d)] whose centroid in time is $3T_{\rm clk}/4$ away from the clock transition. We find that the new relative excess delay of $T_{\rm clk}/4$ [relative to case (a)] can be neutralized by changing the location of the zero in the transfer function. Excellent agreement is observed between the output power spectra in the two cases (Fig. 7).

Based on these observations, two ADCs were designed in the mesa-HBT technology. Both designs use an M–S–S latch as the internal quantizer. While one design uses an NRZ DAC, the other uses an RTZ DAC to compensate for the excess delay introduced by the additional stage of regeneration. Section IV discusses some of the circuit-design aspects of the ADC.

IV. Circuit Design

Fig. 8 shows a simplified block diagram of the IC. Clock buffers are used to convert the single-ended clock signal available from the synthesizer to differential form. This differential clock signal feeds the comparator and the RTZ DAC.

The circuit schematic for the first integrator is shown in Fig. 9. Transistors Q3, Q4, Q7, and Q8, in association with the degeneration resistance $R{\rm deg}$ produce a negative resistance to compensate for the effect of the load resistance Rl. As a result, the dc gain of the integrator is greatly increased

Since it is outside the loop, the linearity of the input stage impacts the dynamic range of the Σ–Δ ADC. It is thus critical

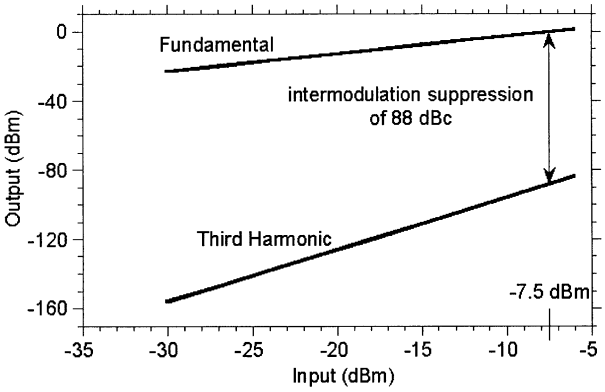

Fig. 10. Simulation result: SPICE simulation of the linearity of the integrator. We observe an intermodulation suppression of 88 dBc at an input power of −7.5 dBm.

that the input transconductance cell be highly linear with minimal distortion. To achieve this, Jensen *et al.* [5] use a linearized input g_m stage based on the Caprio's cell [13]. In our designs, to minimize circuit complexity, we make the bias current of the transconductance cell much larger than the current fed back by the DAC. This results in a situation where the Σ–Δ loop overloads before the input transconductance cell. Hence, high linearity and minimal distortion are achieved in the input stage at the cost of increased dc power. Fig. 10 shows the variation of the fundamental and third-order tones with input power. At an input power of −7.5 dBm, we observe an intermodulation suppression of 88 dBc.

In addition, the input stage contributes thermal and shot noise, and can limit the SNR. Using a calculation similar to that shown in [14], we estimate the input-noise limited SNR to be 153 dB (1 Hz).

The circuit schematic of the second integrator is similar to the first integrator. The quantizer is an 87-GHz [3] M–S–S flip-flop. While the NRZ DAC is a simple current-switching pair, the RTZ DAC has two levels of switching, one for the data and one for the clock. To maintain the charge fed back by the DAC constant in the two cases, the RTZ DAC uses a bias current four times higher than the NRZ DAC. The error signal is generated by current summing at the output nodes of the first transconductance cell. Section V describes the measurement setup and the measured results.

V. Measurement and Results

The IC micrograph of the RTZ-DAC-based ADC is shown in Fig. 11. The design consists of 76 transistors and dissipates 1.8 W.

Fig. 12 compares the output power spectrum, as viewed on a spectrum analyzer, for the two circuits. In agreement with our simulations, the RTZ-DAC-based ADC exhibits better resolution than the NRZ-DAC-based ADC and is likely due to its lower loop delay. In addition, the noise level for the RTZ-DAC-based ADC is constant at the lower end of the spectrum. Digital acquisition of the bit stream is necessary to ensure that we are not limited by the dynamic range of the spectrum analyzer and, if so, to predict the performance of the RTZ-DAC-based ADC correctly. We now discuss the results of such logic analyzer-based digital acquisition measurements. For the remainder of this section, the term ADC will refer to the RTZ-DAC-based ADC unless otherwise mentioned.

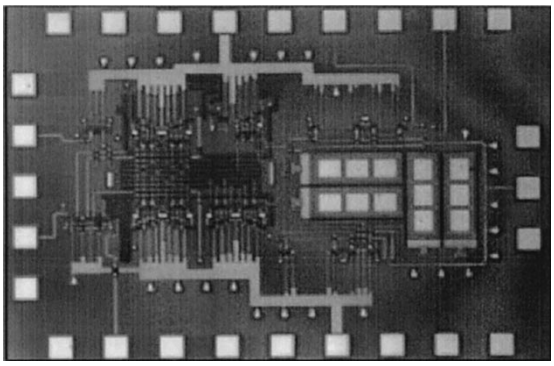

Fig. 11. IC micrograph of the RTZ-DAC-based ADC.

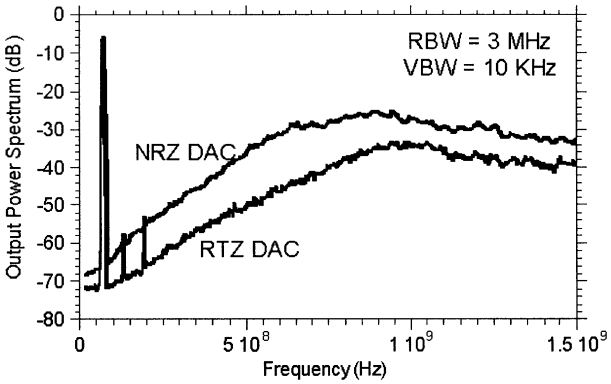

Fig. 12. Comparison of the output power spectra of the NRZ-DAC-based ADC and the RTZ-DAC-based ADC as measured on an analog spectrum analyzer.

We capture the digital data stream by first demultiplexing it into 16 channels of 500 Ms/s each using a commercial 10-G DEMUX. The data from the 16 channels is then read into a logic analyzer and transferred to a computer. The original 8-Gb/s waveform is then reconstructed in software and a MATLAB-based program is used to perform a fast Fourier transform (FFT) on this reconstructed waveform. We perform a 131 072-point FFT for both one- and two-tone measurements.

Fig. 13 plots the calculated 131 072-point FFT spectrum for 62.5-MHz input. The OSR is 64 and the input power is 3 dBm. For single-tone measurements, SNR, and effective number of bits (ENOB) of resolution for a Nyquist-rate ADC are related by the expression [15]

$$\mathrm{ENOB} = \frac{(\mathrm{SNR} - 1.76)}{6.02}.$$

We have calculated the SNR and ENOB using the noise power integrated over the signal bandwidth. The results are presented in Table I at different signal frequencies.

The loop does not show ideal behavior for high OSRs (>= 32). For example, the SNR for an ideal 8-GHz clock rate second-order Σ–Δ modulator, at an OSR of 32, is 51 dB if the SNR is calculated using the noise power measured on the upper band edge. The measured ADC exhibits an SNR of 48 dB at this OSR.

We believe that the nonideal behavior at low frequencies is due to a couple of reasons, namely, residual metastability errors

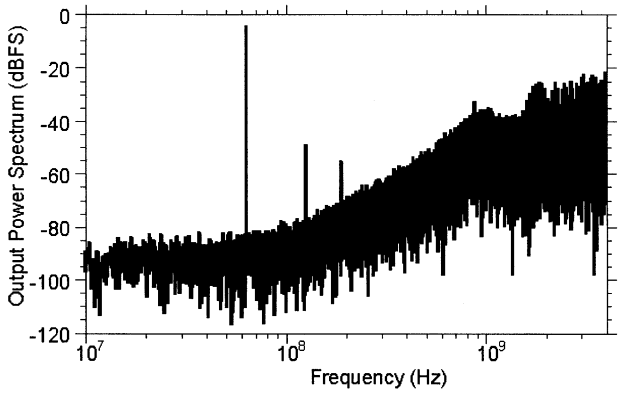

Fig. 13. Output power spectrum of the ADC obtained by a 131 072-point FFT performed on digital data acquired at 8 Gb/s.

TABLE I
SNR AND ENOB USING NOISE POWER INTEGRATED OVER SIGNAL BANDWIDTH

Signal Frequency	Equivalent Sampling rate	SNR, dB 61 kHz	SNR, dB 1Hz	SNR, dB Nyquist	ENOB
62.5 MHz	125 Ms/s	87.54	135.39	57.4	9.25
125 MHz	250 Ms/s	84.8	132.65	51.7	8.29
250 MHz	500 Ms/s	76.3	124.15	40.2	6.38

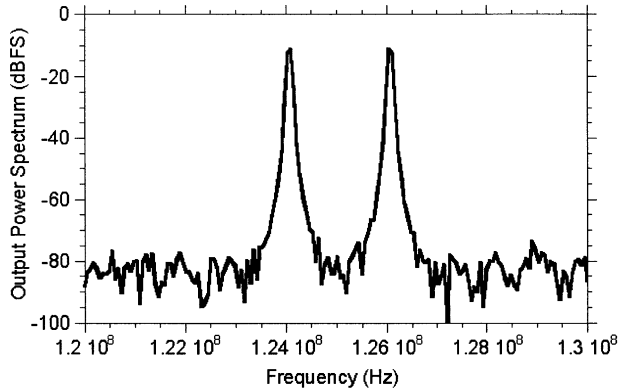

Fig. 14. Third-order distortion for a two-tone input at 124 and 126 MHz. The intermodulation products are below the noise floor and, hence, are not visible.

in the quantizer, and to delays associated with latch latency. We performed post-measurement simulations on the ADC where we delayed the clock to the RTZ DAC relative to the M–S–S latch by 3 ps. In such a scenario, spurious glitches are produced in the DAC pulse, and this manifests itself in the output power spectrum as a whitening of the noise-floor at low frequencies. In fact, the SNR at 250 Ms/s was degraded by almost 10 dB in such a scenario. Hence, even a mismatch in line-length of the order of tens of micrometers is sufficient to degrade the SNR at low frequencies by a few decibels.

In addition, we were also able to control the noise-floor level at low frequencies by changing the comparator bias. The comparator bias controls the speed of the comparator and, hence, the metastability errors in the quantizer. Based on this, we conclude that a faster quantizer would have resulted in lesser metastability errors in the quantizer and, hence, in a more ideal output power spectrum.

To investigate the linearity of the input transconductance stage, we performed two-tone measurements on the ADC.

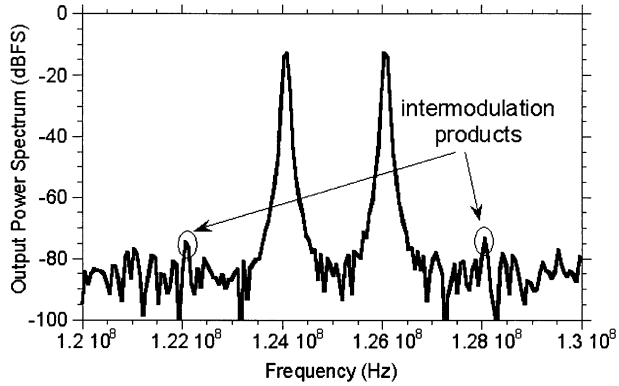

Fig. 15. Third-order distortion for a two-tone input at 124 and 126 MHz; the comparator is biased for maximum speed.

Fig. 14 shows the output power spectrum for two tones at 124 and 126 MHz. We observe $>$ 80 dBc suppression of the two-tone intermodulation products. For this measurement, the comparator was not biased for maximum speed. Due to a design oversight, we do not use separate voltage sources for the integrator, comparator, and DAC. For this reason, the bias current in the DAC increases at a much faster rate than the bias current in the integrator, when the supply voltage is increased. Hence, we observe only 70-dBc suppression of the two-tone intermodulation products at the best bias point (Fig. 15).

Based on these results, we conclude that, at the cost of increased dc power, sufficient intermodulation suppression can be achieved by ensuring that the input stage overloads well after loop overload occurs.

VI. CONCLUSIONS

We have demonstrated an 8-GHz clock-rate second-order continuous-time Σ–Δ ADC in an InP-based mesa-HBT technology. The ADC achieves SNR of 57.4, 51.7, and 40.2 dB, corresponding to 9.25, 8.29, and 6.38 effective bits at signal sampling rates of 125, 250, and 500 Ms/s, respectively. The IC occupies a die area of 1.45 mm^2, contains 76 transistors and dissipates 1.8 W of power. In addition, we have also proposed, given the inability of a linear additive white-noise model to explain the dynamics of a 1-bit internal quantizer, a centroid-in-time-based approach to neutralize the effect of excess delay on modulator performance.

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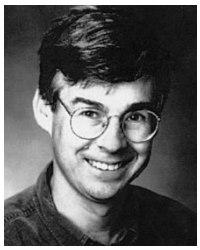

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