

250 nm InGaAs/InP DHBTs w/ 650 GHz f_{max} and 420 GHz f_{τ} , operating above 30 mW/ μm^2

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We report a 250 nm InP/In_{0.53}Ga_{0.47}As/InP double heterostructure bipolar transistor (DHBT), exhibiting a record 650 GHz f_{max} with simultaneous 420 GHz f_{τ} . This is to our knowledge the highest f_{max} reported for a DHBT. The emitter junction width has been scaled to ~ 250 nm, substantial improvement has been made to the base and emitter Ohmic contacts, and the InGaAs subcollector has been thinned to increase the HBT thermal conductivity. The devices show excellent power handling, operating at power densities in excess of 30 mW/ μm^2 . Critically, unlike many previously reported DHBTs, the high power density associated with the devices here permits the HBTs to be biased simultaneously at high bias voltages and high current densities J_e ; an attribute as important as the breakdown voltage in determining the useful voltage capability of a transistor technology. Previous 0.6 μm emitter InP DHBTs from UCSB utilizing a 150 nm collector displayed a 390 GHz f_{τ} and 505 GHz f_{max} , at $J_e = 5.17$ mA/ μm^2 [1]. Prior to this work the highest reported f_{max} DHBT was 519 GHz with simultaneous 252 GHz f_{τ} [2].

Development of high speed digital and mixed-signal systems having increased bandwidths requires improved HBT performance. For example, projected 160 Gb/s systems require > 400 GHz f/f_{max} , and low collector base capacitance ($C_{cb}/I_c < 0.5$ ps) [3]. By lateral scaling at a fixed vertical geometry, substantial improvement of f_{max} can be achieved due to the reduced C_{cb} and R_{bb} [4]. For sub-mm-wave amplifiers, an HBT having high f_{max} , high breakdown voltages, as well as an ability to operate at high power densities is required.

The DHBTs presented in this work were fabricated in an all-wet-etch, triple mesa process. All device features were defined by I-line stepper lithography. An SEM of a completed device is shown in figure 1. The epitaxial material (Table 1) was grown by IQE Inc. The InGaAs base is 30-nm thick employing graded carbon doping from $7\text{-}4 \times 10^{19}$ cm⁻³ that in-turn introduces $\Delta E_c \cong 50$ meV of conduction band grading. To suppress any current blocking effects originating from the conduction band discontinuity between the InGaAs base and InP collector ($\Delta E_c \approx 0.26$ eV), the collector utilizes a 15-nm InGaAs setback layer followed by a 24-nm InAlAs/InGaAs chirped super-lattice grade and appropriate pulse-doping so as to provide a continuous conduction band between In_{0.53}Ga_{0.47}As and InP. The emitter contact metal is 390 nm wide and SEM inspection shows 70 nm of lateral undercut during the mesa formation, making the emitter-base junction width 250 nm. To eliminate C_{cb} underneath the base pad, the semiconductor associated with this area is etched away. The devices are passivated with and planarized using benzocyclobutene BCB.

Transmission line measurements (TLM) show a base contact resistance $\rho_c < 5$ $\Omega \cdot \mu\text{m}^2$ and a base sheet resistance $\rho_s = 630$ Ω , and the collector $\rho_c = 11$ $\Omega \cdot \mu\text{m}^2$ and $\rho_s = 12.5$ Ω . The emitter $\rho_c = 5.3$ $\Omega \cdot \mu\text{m}^2$ was extracted from RF-parameter fitting. Compared to [1], this is $\sim 50\%$ reduction in both the emitter and base Ohmic contact resistance. The HBTs show $\beta = 25\text{-}30$ and a BV_{ceo} 4.5-5 V at 1 kA/cm². Breakdown measured at $I_c = 1$ mA exceeds 7 V. A plot of the common-emitter current-voltage and Gummel characteristics are shown in figures 2 and 3. In addition, figure 2 demonstrates the effectiveness of the base-collector grade with no evidence of current blocking until $J_e \geq 16$ mA/ μm^2 at $V_{ce} = 2.0$ V. The devices can further operate with a power density up to 30 mW/ μm^2 , without showing strong effects (output conductance, current gain modulation) due to self-heating.

DC-67 GHz RF characterization was conducted after performing an off-wafer LRRM calibration to an Agilent E8361A PNA. On-wafer open and short circuit pad structures identical to the ones used by the devices were measured after calibration in order to de-embed their associated parasitics from the device measurements. A maximum 420 GHz f_{τ} and 650 GHz f_{max} (fig. 4, 5) at $I_c = 9$ mA and $V_{ce} = 1.58$ V ($V_{cb} = 0.6$ V, $J_e = 12$ mA/ μm^2 , $C_{cb}/I_c = 0.34$ ps/V) was measured, obtained from $|H_{21}|$ and Mason's unilateral gain U by extrapolating at -20 dB/decade using a single pole fit to the measured data. A small-signal hybrid- π model of the HBT at this bias is shown in figure 6. This device had an emitter-base junction area $A_{je} = 0.25 \times 3$ μm^2 , and a base-collector area associated with the base contact $A_{jc} = 0.95 \times 5$ μm^2 . The trend in C_{cb} with V_{cb} and J_e is shown in figure 7. Compared to [1] the current density for highest f_{max} for the HBTs here increased over 2:1. We attribute this to the increased effect of current spreading associated with narrower emitters, reduced emitter ρ_c and greatly reduced self heating.

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3. T. Enoki et al., *International Journal of High Speed Electronics and Systems*, Vol. 11, No. 1, pp. 137-158, 2001
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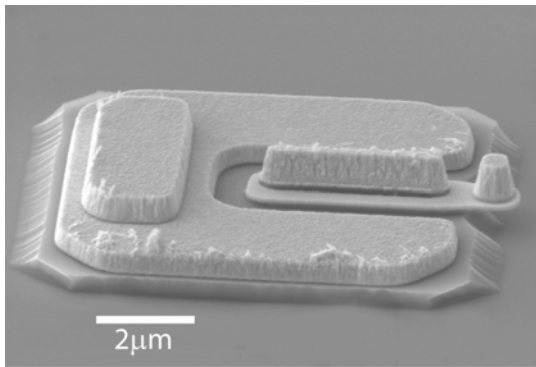


Figure 1. SEM image of DHBT

Thickness	Material	Doping	Comment
30 nm	InGaAs	$4-7 \times 10^{19} : \text{C}$	Base
15 nm	InGaAs	$3.5 \times 10^{16} : \text{Si}$	Setback
24 nm	InGaAs/InAlAs	$3.5 \times 10^{16} : \text{Si}$	Grade
3 nm	InP	$2.8 \times 10^{18} : \text{Si}$	Δ -doping
108 nm	InP	$3.5 \times 10^{16} : \text{Si}$	Collector
5 nm	InP	$1.0 \times 10^{19} : \text{Si}$	Subcollector
5 nm	InGaAs	$2.0 \times 10^{19} : \text{Si}$	Subcollector
300 nm	InP	$2.0 \times 10^{19} : \text{Si}$	Subcollector
	InP	S.I.	Substrate

Table 1. DHBT layer structure

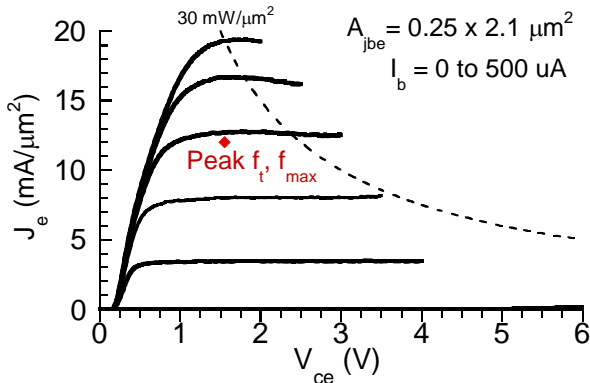


Figure 2. Common emitter I-V characteristics

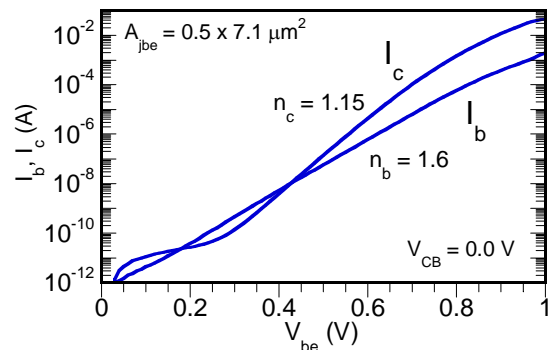


Fig. 3. Gummel characteristics

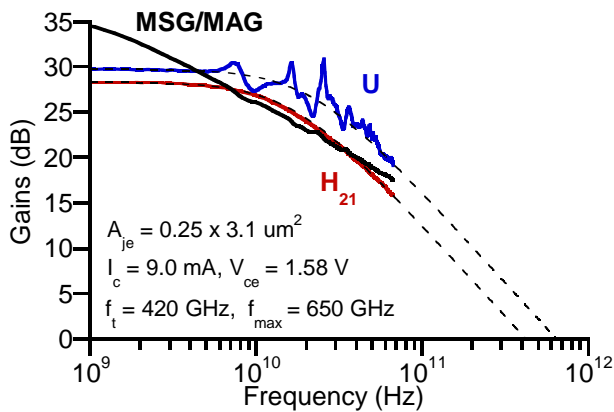


Figure 4. Microwave gains at peak f_t and f_{max}

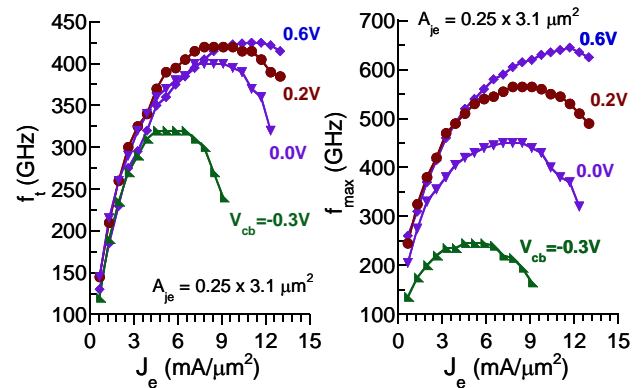


Figure 5. f_t and f_{max} vs. J_e and V_{cb}

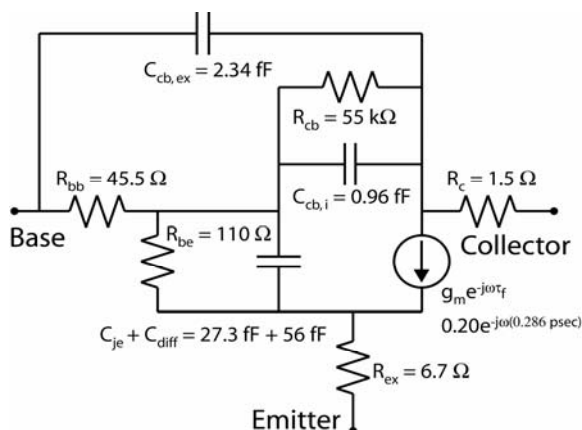


Figure 6. Small signal hybrid- π equivalent circuit

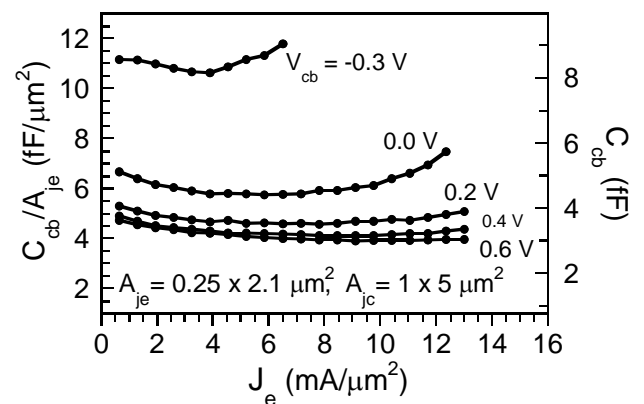


Figure 7. C_{cb} variation with bias

