

# High resolution 20 GHz wideband delay generator

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A digitally-programmable method for linearly controlling signal delay over a wide frequency and delay range has been developed. Circuits were fabricated in the HRL's G2+ InP HBT technology. Test results at 20 GHz confirm simulation results, showing a 5 ps range in delay, ramped in 16 steps to provide a 0.3 ps resolution step. Larger delay ranges are possible by combining several of the delay cells in series.

**Introduction:** In high resolution beamsteering applications, a delay generator is required to have a resolution better than 0.25 ps over a range of several picoseconds of phase shift on a 10–40 GHz signal. This has not been achieved yet for current systems. Dawson and Rogerson [1] and Schmidt and Rein [2] published analogue phase shifters with analogue control inputs. They used emitter degeneration resistors to increase the linearity of the phase-shifting response. Their circuits resulted in resolutions of about 2 ps at 11 ps of shift for a signal of 1.8 GHz. In 1989, Otsuji and Narumi [3] fabricated delay lines for delay generation, using digital switching to select the appropriate time delay. They reported achieving 8 ps of resolution with  $\pm 2$  ps of linearity error at 700 MHz. In 1991, Nitta *et al.* [4] created a variable delay generator using a fully digital circuit with ramp generation and a voltage comparator for delay control. They used a DAC to control the voltage input and achieved 29 ps of resolution in the range of 0–1.8 ns of delay. Their circuit was fully digital. In 1998, Chua and Martin [5] used a DAC to control the currents through an analogue delay cell, controlling the circuit gain with the DAC output. The best published results were those of the first set of authors [1, 2], but they are still far from the resolutions and frequencies required by current beamsteering applications. Coy [6] applied digital programming to his delay circuit, but the way that the delay cell was designed gave it an inherently nonlinear delay response.

**Circuit design:** The novel delay generator configuration that has been developed is shown in Fig. 1. In traditional implementations [2] there is a single analogue control signal controlling the current through the differential pairs. Emitter degeneration or pre- or post-distortion techniques usually are needed to linearise the relationship between voltage and delay. The current in the delay generator is dependent on the noise at the analogue control input, likely resulting in a higher phase noise at the output of the circuit. To address the linearity and phase noise problems of the traditional analogue delay cell, the mixing current in the proposed circuit is generated by driving the emitters of the two mixing differential pairs with a current-mode digital-to-analogue converter instead of with an analogue voltage. One advantage of using a digital control input is that the current against digital input relationship will be linear. This is due to the removal of the lower nonlinear differential pair. More importantly, since the control input is digital, noise on that input will not induce added phase noise.

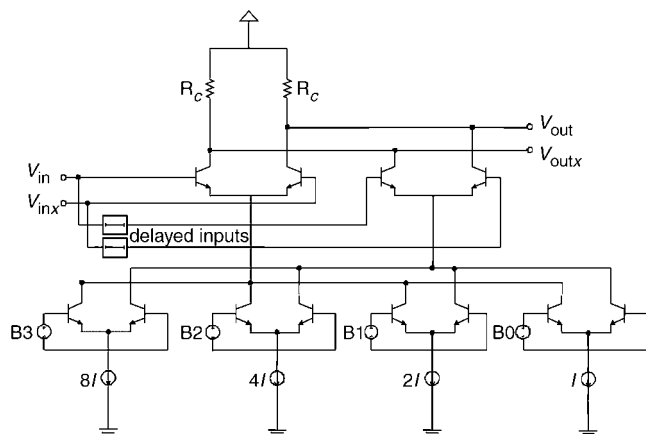


Fig. 1 Conceptual schematic of improved digital delay generator with 4-bit current DAC implementation

**Method and results of delay measurements:** To facilitate measurement of the delay of the circuits to be tested, the test circuit shown in Fig. 2 was designed and fabricated. The RF input was a 0 dBm, 1–20 GHz sine wave controlled by an HP83650L CW generator. The input signal was split, with half going to the delay circuit and the other half through an ARRA 9428B broadband phase shifter. The phase shifter was adjusted to produce quadrature between the two input signals to the phase detector. This on-chip phase detector demodulated the delay generator output, facilitating delay and phase noise measurement. To measure the delay operation of the circuit, the output of the phase detector was connected directly to an oscilloscope. The signal was monitored while an HP 80000 data generator system controlled the delay using a 4-bit digitally-programmed ramp at a 4 MHz repetition rate. The phase detector output against ramp time is shown in Fig. 3. Each step corresponds to a change in the 4-bit digital input ramp. Fig. 4 shows the delay against digital input results obtained from Fig. 3; these results are plotted with the simulation results for comparison. The deviation from linear was 0.25 ps in the experimental results. A larger chip was designed with a combination of Fig. 1 delay cells in series (data not shown). Maximum delay ranges of 60–80 ps were measured from these extended delay chips. This range represents over 360° of shift at 20 GHz. Maximum deviation from linearity was less than 8% of full scale. Typical power dissipation was 200 mW for the single delay cell and 900 mW for the higher delay range chip.

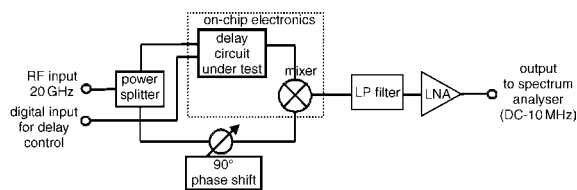


Fig. 2 Delay measurement setup, with delay generator and phase detector on-chip

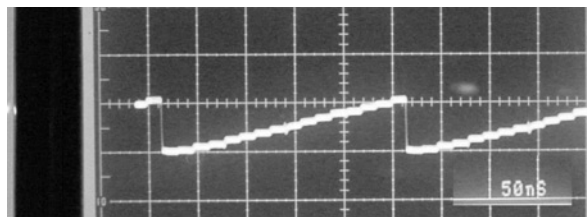


Fig. 3 Phase detector output against time in response to digitally-ramped control input to delay cell

Repetition rate of ramp was 4 MHz

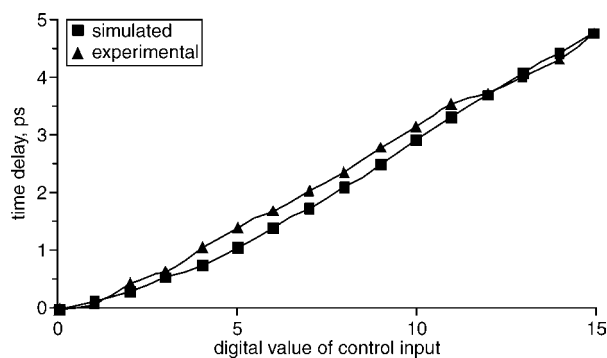


Fig. 4 Delay against digital control input value, simulated and experimental results

**Conclusions:** We have demonstrated 20 GHz, wideband, delay circuits in the InP HBT G2+ process at HRL Laboratories. Best performance was demonstrated by the digitally-controlled delay circuits with resolutions as fine as 0.1 ps over a 5 ps range. Ranges of up to 60–80 ps were demonstrated using serial combinations of the single delay cell.

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#### References

- 1 Dawson, P.A., and Rogerson, S.P.: 'An undersea fiber-optic regenerator using an integral-substrate package and flip-chip SAW mounting', *J. Lightwave Technol.*, 1984, **2**, (6), pp. 926–932
- 2 Schmidt, L., and Rein, H.: 'Continuously variable gigahertz phase-shifter IC covering more than one frequency decade', *IEEE J. Solid-State Circuits*, 1992, **27**, (6), pp. 854–862
- 3 Otsuji, T., and Narumi, N.: 'A 10-ps resolution, process-insensitive timing generator IC', *IEEE J. Solid-State Circuits*, 1989, **24**, (5), pp. 1412–1417
- 4 Nitta, S., *et al.*: 'A variable delay generator for DESKEW IC using ECL gate array'. Symp. VLSI Circuits, Oiso, Japan, 1991, pp. 55–56
- 5 Chua, M., and Martin, K.W.: '1 GHz programmable analog phase shifter for adaptive antennas'. IEEE Customised IC Conf., Santa Clara, CA, USA, 1998, p. 71
- 6 Coy, B.H.: 'Analog Delay Circuit'. US Patent 5,945,863, 31 August, 1999