Transistor and Circuit Design for 100-200 GHz ICs

M. Rodwell, Z. Griffith, D. Scott, Y. Wei, Y. Dong, V. Paidi, M. Dahlström, N. Parthasarathy, C. Kadow, ECE Department, University of California, Santa Barbara, 93106, USA, rodwell@ece.ucsb.edu

M. Urteaga , R. Pierson, P. Rowell, B. Brar, Rockwell Scientific Company, Thousand Oaks, CA 91360, USA

S. Lee, N. Nguyen, and C. Nguyen, Global Communication Semiconductors, Torrance, CA,

***Abstract* — Compared to SiGe, InP HBTs offer superior electron transport but inferior scaling and parasitic reduction. Figures of merit for mixed-signal ICs are developed and HBT scaling laws for improved circuit speed are introduced. Device and circuit results are summarized, including 390 GHz f_τ / 500 GHz f_{max} DHBTs, 174 GHz amplifiers, and 150 GHz static frequency dividers. To compete with 100 nm SiGe processes, InP must be similarly scaled, and high process yields are imperative. We describe several process modules in development, including emitter regrowth, emitter-base dielectric sidewall processes, and a collector pedestal implant process.**

I. Introduction

Despite formidable progress in CMOS, bipolar transistors are competitive due to the larger breakdown voltages obtainable and the larger lithographic feature sizes required for a transistor of a specified bandwidth. SiGe HBTs have demonstrated simultaneous > 300 GHz f_τ and f_{max} and 96 GHz static dividers, while InP DHBTs have obtained ~400 GHz f_τ and ~500 GHz f_{max}, > 150 GHz static dividers, and 176 GHz power amplifiers. Compared to SiGe, InP HBTs have ~3.5:1 better collector electron velocity and ~10:1 better base electron diffusivity. Consequently, given the same junction dimensions, an InP HBT would have ~3:1 greater bandwidth than a SiGe HBT. Today, SiGe HBTs are fabricated with much narrower junctions and much smaller extrinsic parasitics. Consequently, the two technologies today have comparable bandwidth, while SiGe offers much higher integration scales. Continued progress with InP HBTs therefore requires close attention to scaling laws and scaling limits. Requirements placed upon transistor design for wideband circuits must be clearly understood. Fabrication processes must provide high yield at 100 nm scaling.

II. HBT Performance Metrics

f_τ and f_{max} are of limited value in predicting the speed of logic, mixed-signal, or optical transmission ICs. As representative case, the maximum clock frequency $f_{clock,max}$ of an ECL master-slave latch[1] is $T_{gate} = 1/2f_{clock,max} = \Sigma a_{ij} R_i C_j$; Table 1 gives the delay coefficients a_{ij} and the components of T_{gate} for an HBT with target 260 GHz $f_{clock,max}$. In terms of resistances, 82% of T_{gate} arises from the load resistance $\Delta V_L / I_c$. High current density is essential. Since the logic voltage swing ΔV_L must be at least $4(kT + R_{EX} I_E)$, increased current density much be accompanied by reduced emitter resistance, so as to maintain low ΔV_L. In terms of capacitances, 58% of T_{gate} arises from the depletion capacitances $C_{cb} + C_{je}$, and only 18% with τ_f, even

..	C_{je}	C_{cbx}	C_{cbi}	$\tau_f I_E / \Delta V_L$	$\tau_W I_E / \Delta V_L$
$\Delta V_L / I_E$	1	6	6	1	1
kT / qI_E	0.5	1	1	0.5	0
R_{EX}	-0.3	0.5	0.5	0.5	0
R_{bb}	0.5	0	1	0.5	0

..	C_{je}	C_{cbx}	C_{cbi}	$\tau_f I_E / \Delta V_L$	$\tau_W I_E / \Delta V_L$	sum
$\Delta V_L / I_E$	11%	16%	22%			49%
$\Delta V_L / I_E$				15%	18%	33%
kT/qI_E				1%		1%
R_{EX}	-1%			1%		0%
R_{bb}	5%		3%	7%		15%
sum	16%	16%	25%	24%	18%	100%
		42%				

Table. 1: (top) Delay coefficients a_{ij} for an ECL M-S latch, where $T_{gate} = 1/2f_{clock,max} = \Sigma a_{ij} R_i C_j$. (bottom) Proportions of T_{gate} for a 300-nm scaling-generation HBT with target 260 GHz clock rate. C_{je} is the emitter depletion capacitance, C_{cbx} and C_{cbi} the extrinsic and intrinsic collector base capacitances, $\tau_f = \tau_b + \tau_c$ the forward transit time, τ_W the wiring delay, I_E the emitter current, ΔV_L the logic voltage swing, and R_{ex} and R_{bb} the parasitic emitter and base resistances. R_{ex} influences $f_{clock,max}$ *indirectly* through increased ΔV_L.

Parameter	Gen. 1	Gen. 2	Gen. 3
MS-DFF speed	60 GHz	121 GHz	260 GHz
Emitter Width	1 μm	0.8 μm	0.3 μm
Parasitic Resistivity	50 Ω-μm^2	20 Ω-μm^2	5 Ω-μm^2
Base Thickness	400Å	400Å	300 Å
Doping	5 10^{19}/cm^2	7 10^{19}/cm^2	7 10^{19}/cm^2
Sheet resistance	750 Ω	700 Ω	700 Ω
Contact resistance	150 Ω-μm^2	20 Ω-μm^2	20 Ω-μm^2
Collector Width	3 μm	1.6 μm	0.7 μm
Collector Thickness	3000 Å	2000 Å	1000 Å
Current Density	1 mA/μm^2	2.3 mA/μm^2	12 mA/μm^2
$A_{collector}/A_{emitter}$	4.55	2.6	2.9
f_τ	170 GHz	248 GHz	570 GHz
f_{max}	170 GHz	411 GHz	680 GHz
I_E / L_E	1 mA/μm	1.9 mA/μm	3.7 mA/μm
τ_f	0.67 ps	0.50 ps	0.22 ps
C_{cb} / I_c	1.7 ps/V	0.62 ps/V	0.26 ps/V
$C_{cb}\Delta V_{logic} / I_c$	0.5 ps	0.19 ps	0.09 ps
$R_{bb} / (\Delta V_{logic} / I_c)$	0.8	0.68	0.99
$C_{je}(\Delta V_{logic} / I_C)$	1.7 ps	0.72 ps	0.15 ps
$R_{ex} / (\Delta V_{logic} / I_c)$	0.1	0.15	0.17

Table. 2: Technology roadmaps for 40, 80, and 160 Gb/s ICs. Master-slave latch delay includes 10% interconnect delay.

given the assumed transistor design having small C/I ratios.

nFor logic and mixed-signal ICs, low $C_{cb}\Delta V_L / I_E$ and $C_{je}\Delta V_L / I_E$ charging times are critical, necessitating very high current density, minimal excess collector junction area, and very low emitter access resistance. Transit delay plays a smaller role; at a given scaling generation, an HBT can be designed for highest feasible f_τ while sacrificing both $f_{\max}$ and logic speed. Such transistors, regularly reported in the literature, have limited value.

II. Scaling: Laws, Limitations, & Roadmaps

Consider scaling laws[1]. For a 2:1 speed increase in all circuits, all device capacitances and transit delays must be reduced 2:1 while maintaining constant I_C, g_m, and all parasitic resistances. This is accomplished by thinning the collector depletion layer 2:1, thinning the base $\sqrt{2}$:1, reducing the emitter and collector junction areas 4:1 and widths ~4:1, reducing the emitter resistance per unit area 4:1, and increasing the current density 4:1. Thinning the collector 2:1 increases the collector capacitance per unit area 2:1 but increases the Kirk-effect-limited current density 4:1; C_{cb}/I_C is thus reduced 2:1. If the base Ohmic contacts lie above the collector junction, their width must be reduced 2:1, necessitating a ~4:1 reduction in contact resistivity; if the contacts do not lie above the junction, their resistivity can remain unscaled.

Emitter and base contact resistivity, thermal resistance, and fabrication yield are the key barriers to scaling. Typically the collector-base junction lies below the full width of the base contact, hence narrow collector junctions demand narrow base contacts. This demands low base contact resistance ($\sim 15\,\Omega - \mu\text{m}^2$), low base metal sheet resistance, and tight alignment tolerances or self-aligned processes. Emitter contact resistivity is critical, as very low values ($\sim 5\ \Omega - \mu\text{m}^2$) are required for 200 GHz clock speed. Current density must be very high (10-15 $\text{mA}/\mu\text{m}^2$) hence thermal resistance also must be low[2], $< 5\,\text{K}\cdot\mu\text{m}^2/\text{mW}$. Indeed, because current density increases in proportion to the bandwidth squared, maximum reliable power density $J_E V_{CE}$ is a more serious practical limit to applied voltage than the breakdown voltage $V_{br,ceo}$. Table 2 shows a scaling roadmap.

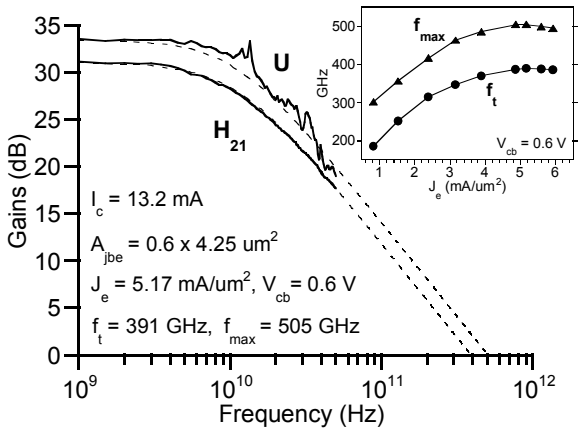

Figure 1: RF gains; 600-nm emitter-width InP mesa DHBT.

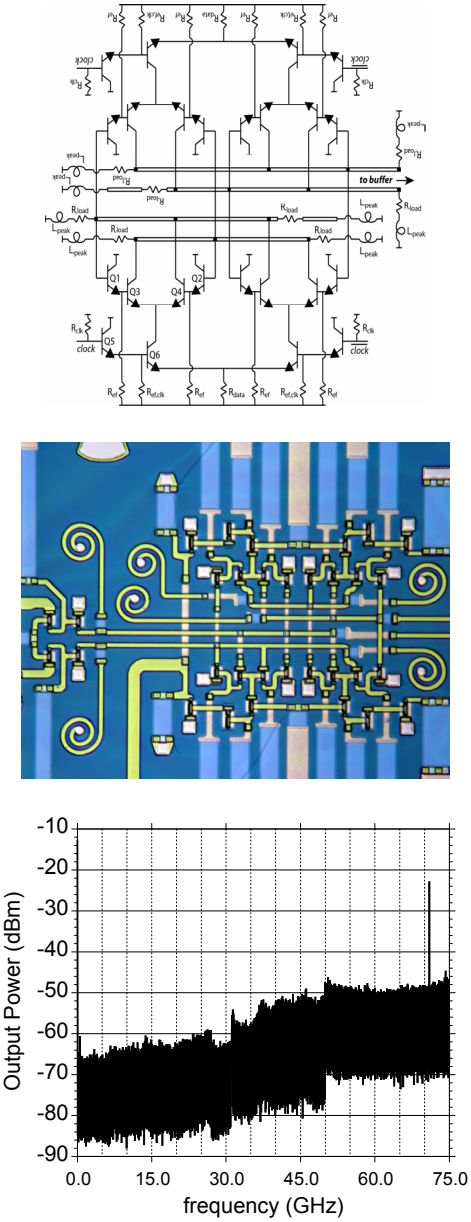

Figure 2: UCSB-built 142-GHz static divider using the HBT of figure 1; circuit diagram, photograph, and output spectrum

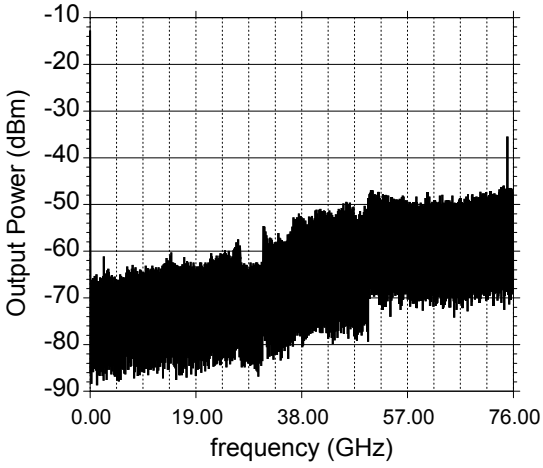

Figure 3: Output spectrum of GCS-built static divider at 150 GHz clock frequency.

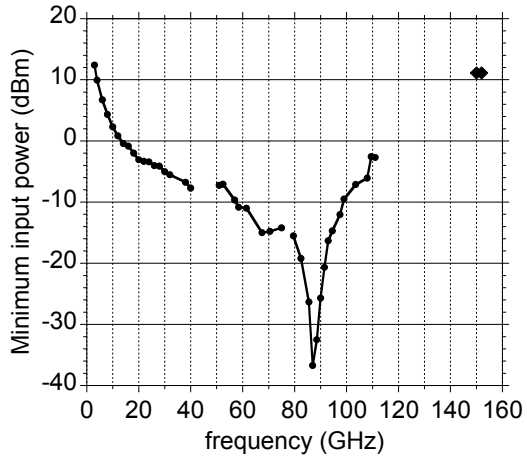

Figure 4: Sensitivity of the GCS-built static frequency divider.

	units	data current steering	data emitter followers	clock current steering	clock emitter followers
size	μm^2	0.5 x 3.5	0.5 x 4.5	0.5 x 4.5	0.5 x 5.5
current density	$mA/\mu m^2$	6.9	4.4	4.4	4.4
C_{cb}/I_c	psec / V	0.59	0.99	0.74	0.86
V_{cb}	V	0.6	0	0.6	1.7
f_t	GHz	301	260	301	280
f_{max}	GHz	358	268	358	280

Table III: Key parameters of the GCS-built static divider.

II. Transistor & IC Results For Mesa HBTs

UCSB's Mesa DHBTs[3] at ~500 nm emitter width (fig. 1) obtain 390 GHz f_τ and 500 $f_{\max}$, $C_{cb}/I_c = 0.51$ ps/V, and $V_{br,ceo} > 5$ V; with these we have demonstrated 142 GHz static dividers. Similar static dividers fabricated at GCS operated at >150 GHz[4]. Fig. 5 shows a 172 GHz amplifier in a similar process.

II. Advanced InP HBT Fabrication Processes

Such mesa HBTs suffer limited yield from the self-aligned emitter-base etch/liftoff process. Further, doubling circuit speed requires $\sim 5\,\Omega-\mu m^2$ emitter contacts and narrow 200 nm base contacts. Dielectric sidewall spacer processes[5] (fig. 6, 7) eliminate the need for a self-aligned base emitter undercut process. Eliminating liftoff not only eliminates short-circuits associated with liftoff failures but also allows a very thin emitter semiconductor for minimal etch undercut[6]. Such processes give high yield at 250 nm emitter width, and allow ~300 GHz f_τ and $f_{\max}$, and $C_{cb}/I_c < 0.55$ ps/V.

Dielectric sidewall processes address neither base nor emitter contact resistivity scaling limits. Closely following the SiGe device structure, we have developed an HBT process flow in which a low-resistivity polycrystalline InAs regrowth[7] (fig. 5) forms a T-shaped emitter whose Ohmic contact is much larger than the emitter junction for reduced R_{ex}. Such reduction of emitter resistance through an increased contact/junction area ratio is an alternative to materials engineering for reduced emitter access resistance. Recall that ~5 $\Omega-\mu m^2$ emitter resistivity is targeted for 260 GHz clock rate, a resistivity ~2:1 better than the best results thus far obtained in our laboratory. The emitter regrowth process also permits an extrinsic base region of $>10^{20}/cm^3$ doping and ~100 nm thickness for reduced R_{bb}. Self-aligned refractory base Ohmic contacts lie under the extrinsic emitter regions. We have demonstrated 280 GHz f_τ in such processes (figs. 8, 9, 10). Presently, device performance is limited by both difficulties in emitter regrowth over the edges of the emitter etch window, and by partial passivation of the base doping by hydrogen associated with the PECVD Si_3N_4 passivation. The fabrication process is now being substantially revised.

At the 300 nm (emitter width) scaling generation, a significant challenge is maintaining an acceptably small collector/emitter junction area ratio. While the base contact transfer length is 200 nm for 20 $\Omega-\mu m^2$ contacts to a 500 Ω/square base, 200-nm-width base contacts present challenges in process design for high yield and in base contact metal sheet resistance. Again, closely following SiGe, an implanted N+ collector pedestal[8] (fig. 11) reduces the capacitance under the base contacts, permitting somewhat higher contact resistivities and wider contacts at a given level of device performance. The pedestal also substantially reduces the C_{cb} associated with the base pad area. Pedestals can be used with mesa, dielectric-sidewall, or regrown emitter-base junctions. With pedestal implants, we observe (figs. 12, 13) both significantly reduced C_{cb} and moderately increased breakdown (5 V for a 100-nm-thick collector). The latter effect is due to the buried-junction device, surface breakdown in InP DHBTs being reduced by the $\sim 10^{12}/cm^2$ (N-type) surface state density typical of ill-passivated InP surfaces.

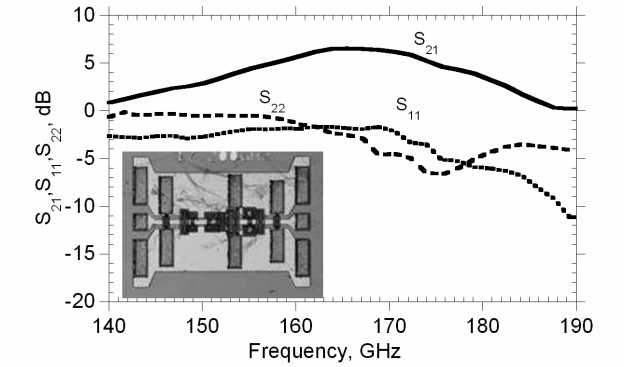

Figure 5: 172 GHz InP HBT amplifier; 8.2 dBm output power

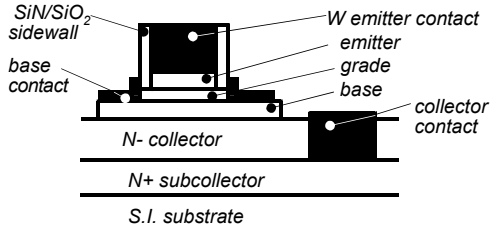

Figure 6: Dielectric-sidewall-spacer emitter-base process; process schematic.

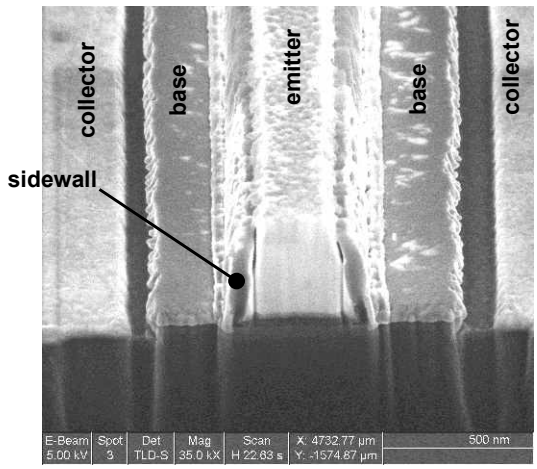

Figure 7: Dielectric-sidewall-spacer emitter-base process: SEM.

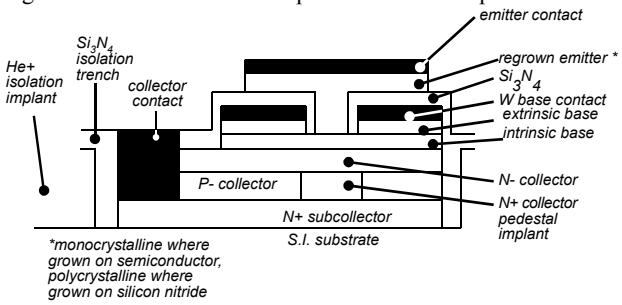

Figure 8: Polycrystalline extrinsic emitter regrowth HBT: process schematic.

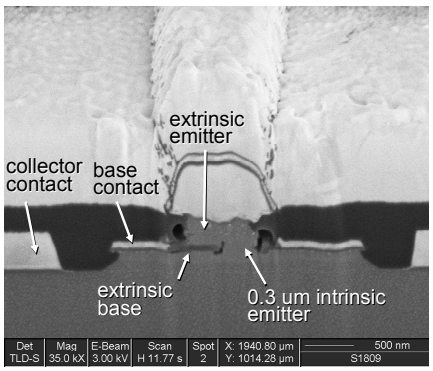

Figure. 9: Regrown emitter HBT: SEM cross-section.

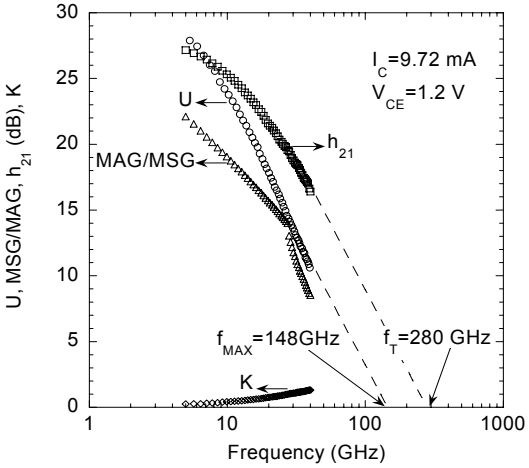

Figure. 10: Regrown emitter HBT: RF performance.

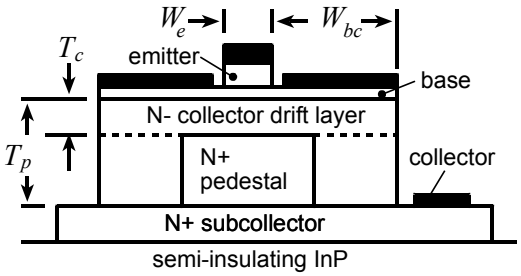

Figure. 11: Collector pedestal implant for reduced Ccb.

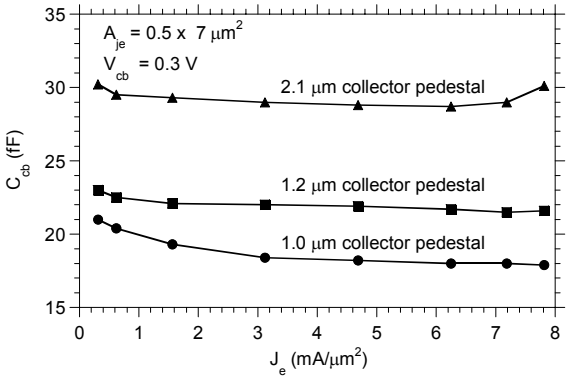

Figure. 12: Collector pedestal HBT: measured Ccb.

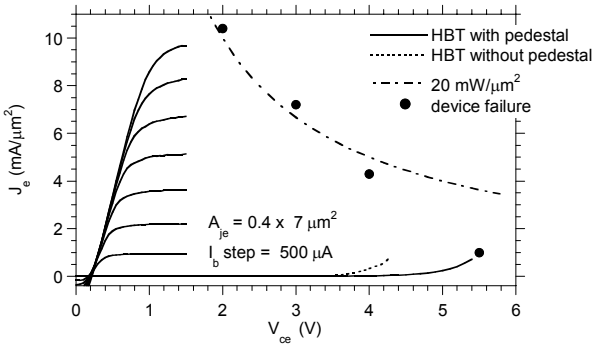

Figure. 13: Collector pedestal HBT: measured DC parameters

ACKNOWLEDGEMENT

UCSB work supported by the DARPA TFAST Program, and by the U.S. ONR under N00014-04-1-0071, N00014-01-1-0024, N0014-99-1-0041, and by a JPL President's fund. RSC work was sponsored by the DARPA TFAST program.

REFERENCES

[1]M. Rodwell *et al*, International Journal of High Speed Electronics and Systems, Vol. 11, No. 1, pp. 159-215.
[2]I. Harrison *et al,* 2003 IEEE Indium Phosphide and Related Materials Conference, May, Santa Barbara, CA. .
[3]Z. Griffith *et al*, Submitted to IEEE Electron Device Letters
[4]Z. Griffith *et al,* 2004 IEEE BCTM, September, Montreal.
[5]S. Oka *et al*, International Journal of High Speed Electronics and Systems, Vol. 11, No. 1, pp. 115-136.
[6]M. Urteaga *et al,* 2004 IEEE Device Research Conference, June, Notre Dame, Ind.
[7]Y. Wei *et al,* 2004 IEEE Device Research Conference, June, Notre Dame, Ind.
[8]Y. Dong *et al*, 2004 IEEE Device Research Conference, June, Notre Dame, Ind.