Frequency Limits of InP-based Integrated Circuits

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***Abstract*—We examine the limits in scaling of InP-based bipolar and field effect transistors for increased device bandwidth. With InP-based HBTs, emitter and base contact resistivities and IC thermal resistance are the major limits to increased device bandwidth; devices with 1-1.5 THz simultaneous f_τ and f_{max} are feasible. Major challenges faced in developing either InGaAs HEMTs having THz cutoff frequencies or InGaAs-channel MOSFETs having drive current consistent with the 22 nm ITRS objectives include the low two-dimensional effective density of states and the high bound state energies in narrow quantum wells.**

I. INTRODUCTION

HIGH -frequency integrated circuit technologies face relentless pressure from CMOS. 90 nm Silicon CMOS processes exhibit ~450 GHz power-gain cutoff frequencies ($f_{\max}$) [1]. 45 nm processes, to be released into production this summer [2], will employ metal gates and high-K gate dielectrics, features which benefit both VLSI digital circuit performance and mm-wave amplification. Given the anticipated dates of introduction of 32 nm and 22 nm processes [2], it is likely that Si CMOS IC processes will provide transistors with >1 THz f_τ and $f_{\max}$ within the next four years. This places Si CMOS as a formidable competitive threat, not only to InP bipolar and field-effect transistors, but also to SiGe bipolar transistors.

Despite this rapid improvement in CMOS bandwidth, bipolar and InP processes retain significant advantages over Si MOS in analog/mixed-signal and microwave/mm-wave circuits. The high output conductance, limited g_m, low breakdown voltage, and variable DC parameters of sub-90 nm Si MOSFETs makes precision mixed-signal design difficult [3]; bipolar transistors have high g_m, low g_{out}, high breakdown voltage, and precisely-controlled DC parameters, and consequently are attractive for precision mixed-signal ICs.

InP transistors obtain high bandwidths with less aggressive scaling and with simpler fabrication processes than are required for Si devices of comparable bandwidths. This is a advantage for low-volume fabrication of small-scale high-performance circuits. InP HBTs obtain significantly larger breakdown voltage that SiGe HBTs of a comparable bandwidth; their breakdown is much larger than that of highly scaled MOSFETs. This is an advantage for both mixed-signal ICs and mm-wave power amplifiers.

Consequently, despite the competitive pressure from CMOS, InP IC processes may survive in high-performance applications having low integration scales, much as the GaAs HBT remains the dominant device for cellular telephone power amplifiers. Further, InP HBTs appear to be far from their scaling limits, and cutoff frequencies beyond 1.5 THz appear to be feasible; this suggests new potential applications at sub-mm-wave frequencies.

Much broader markets may be found for InP-based electronics. Given the present understanding of the difficulties faced in scaling Si MOSFETs to < 22 nm gate length L_g, alternative channel materials --including InGaAs [4,5,6,7] -- are being considered for using in future MOS transistors in very-large scale ICs. The transport advantages of InGaAs channels --high mobilities and high carrier velocities-- are offset by several scaling difficulties associated with the low electron effective mass. Examining these scaling limits is relevant to the potential application of InGaAs to VLSI MOSFETs, and is equally relevant to the scaling potential of < 35 nm L_g InGaAs HEMTs.

II. InP BIPOLAR TRANSISTORS

InP HBTs have potential application in high-resolution ADCs and DACs with sampling rates in the range of 1-10 GS/s, in ~100 GHz gain-bandwidth product operational amplifiers for microwave signal processing, and in mm-wave and sub-mm-wave ICs, particularly power amplifiers. Present transistors [8] with 250 nm minimum feature size have attained 780 GHz power-gain cutoff frequencies ($f_{\max}$) simultaneous with 424 GHz current-gain cutoff frequencies (f_τ) ; devices at the 65 nm generation should attain cutoff frequencies well above 1 THz. This would enable e.g. digital ICs at ~450 GHz clock rate, 750 GHz monolithic power amplifiers, and compact ICs for sub-mm-wave frequency synthesis.

HBT bandwidths are increased by scaling [9,10,11]; both the scaling laws and a scaling roadmap are summarized in Table 1. It is worthwhile to review the underlying simplicity of these scaling laws. If we wish to improve by 2:1 the bandwidth of *any* circuit employing the HBT, we must reduce by 2:1 all transit delays and capacitances while retaining constant all resistances, all bias and signal voltages, and all bias and signal currents. The ratios of junction widths do not change with scaling (Figure 1); for brevity we omit the short discussion required to justify this point. Thinning the

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collector depletion layer by 2:1 will reduce the collector depletion-layer transit time by the required proportion but doubles junction capacitances per unit area; the collector and emitter junction areas must therefore also be reduced 4:1 so as to obtain the required 2:1 reduction in depletion capacitances. The emitter junction area has decreased 4:1; yet the emitter current and the emitter access resistance must both remain constant. Both the emitter current density and the emitter specific access resistivity (resistance normalized to the contact area) must both be reduced 4:1. The 4:1 required increase in current density is consistent with the space-charge-limited current density (the Kirk effect) as this varies as the inverse square of depletion layer thickness.

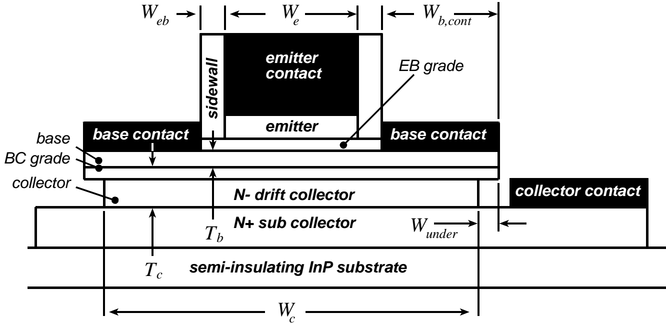

Figure 1: HBT cross-section and critical dimensions. The emitter stripe extends a distance L_e perpendicular to the figure. W_e is the emitter junction width, W_{eb} the base-emitter sidewall spacer thickness, $W_{b,cont}$ the width of the base Ohmic contact, and W_{under} the undercut of the collector junction under the base contacts.

In submicron InP HBTs, base access resistance is *dominated* by the Ohmic contact, the contact width is much less than the contact transfer length, and consequently the base resistance is approximately the base specific contact resistivity divided by the base Ohmic contact area. With a 4:1 reduction in junction areas, the base specific contact resistivity must thus be reduced 4:1.

HBT lithographic scaling laws are now primarily driven by thermal constraints. Approximating heat flow as half-cylindrical at radii $r < L_E/2$ and as hemispherical at greater distances the junction temperature rise of an isolated HBT on a thick substrate is

$$\Delta T \approx \frac{P}{\pi K_{InP} L_E} \ln\left(\frac{L_E}{W_E}\right) + \frac{1}{\pi K_{InP} L_E}. \qquad (1)$$

K_{InP} is the substrate thermal conductivity and P the dissipated power. We must reduce the emitter junction area $L_E W_E$ by 4:1; maintaining constant emitter stripe length L_E while reducing the stripe width W_E by 4:1 results in only a moderate (logarithmic) increase in junction temperature with scaling.

We have now found the requirements for HBT scaling; the full scaling laws are shown in Table 1. The table shows not only transistor cutoff frequencies (f_τ, $f_{\max}$) but also key time constants (e.g. $C_{cb}\Delta V_{\text{logic}}/I_c$) associated with digital gate delay [10]. Transistors for mm-wave amplification are designed for highest $f_{\max}$ and for $f_\tau > f_{\max}/2$, while HBTs for mixed-signal ICs are designed for minimum ECL gate delay [10]; transistors designed for highest feasible f_τ but having $f_{\max} << f_\tau$ are of extremely limited utility in circuits.

Table 1: Bipolar transistor scaling laws and InP HBT scaling roadmap.

Parameter	scaling law	Gen. 2 (500 nm)	Gen. 3 (250 nm)	Gen. 4 (125 nm)	Gen 5 (62.5nm)
MS-DFF speed	γ^1	150 GHz	240 GHz	330 GHz	440 GHz
Amplifier center frequency	γ^1	245 GHz	430 GHz	660 GHz	750 GHz
Emitter Width	$1/\gamma^2$	500 nm	250 nm	125 nm	62.5 nm
Resistivity	$1/\gamma^2$	16 Ω-μm²	8 Ω-μm²	4 Ω-μm²	2 Ω-μm²
Base Thickness	$1/\gamma^{1/2}$	300Å	250 Å	212 Å	180 Å
Contact width	$1/\gamma^2$	300 nm	175 nm	120 nm	70 nm
Doping	γ^0	7 10¹⁹ /cm²	7 10¹⁹ /cm²	7 10¹⁹ /cm²	7 10¹⁹ /cm²
Sheet resistance	$\gamma^{1/2}$	500 Ω	600 Ω	708 Ω	830 Ω
Contact ρ	$1/\gamma^2$	20 Ω-μm²	10 Ω-μm²	5 Ω-μm²	5 Ω-μm²
Collector Width	$1/\gamma^2$	1.2 μm	0.60 μm	0.36 μm	0.20 μm
Thickness	$1/\gamma$	1500 Å	1060 Å	750 Å	530 Å
Current Density	γ^2	4.5 mA/μm²	9 mA/μm²	18 mA/μm²	36 mA/μm²
$A_{\text{collector}}/A_{\text{emitter}}$	γ^0	2.4	2.4	2.9	2.8
f_τ	γ^1	370 GHz	520 GHz	730 GHz	1.0 THz
$f_{\max}$	γ^1	490 GHz	850 GHz	1.30 THz	1.5 THz
$V_{BR,CEO}$		4.9 V	4.0 V	3.3 V	2.75 V
I_E/L_E	γ^0	2.3 mA/μm	2.3 mA/μm	2.3 mA/μm	2.3 mA/μm
τ_f	$1/\gamma$	340 fs	240 fs	180 fs	130 fs
C_{cb}/I_c	$1/\gamma$	400 fs/V	280 fs/V	240 fs/V	190 fs/V
$C_{cb}\Delta V_{\text{logic}}/I_c$	$1/\gamma$	120 fs	85 fs	74 fs	57 fs
$R_{bb}/(\Delta V_{\text{logic}}/I_c)$	γ^0	0.76	0.47	0.34	0.39
$C_{je}(\Delta V_{\text{logic}}/I_C)$	$1/\gamma^{3/2}$	380 fs	180 fs	94 fs	50 fs
$R_{ex}/(\Delta V_{\text{logic}}/I_c)$	γ^0	0.24	0.24	0.24	0.24

Contact and thermal resistivities are presently the most serious barriers to scaling. Let us first consider thermal constraints. On large mixed-signal ICs, IC thermal resistance places perhaps the most severe scaling constraint. On an IC, transistor spacings D are small and must scale in inverse proportion to circuit bandwidth in order to scale wiring delays. Heat flow is then approximately half-cylindrical at radii $r < L_E/2$, hemispherical at radii $L_E/2 < r < D/2$, and planar at radii $D/2 < r < T_{sub}$, where T_{sub} is the substrate thickness. The substrate temperature rise is then

$$\Delta T_{InP} \sim \Delta T_{\text{cylindrical}} + \Delta T_{\text{hemisperical}} + \Delta T_{\text{planar}}$$
$$= \left(\frac{P}{\pi K_{InP} L_E}\right) \ln\left(\frac{L_e}{W_e}\right) + \left(\frac{P}{\pi K_{InP}}\right)\left(\frac{1}{L_E} - \frac{1}{D}\right) \qquad (2)$$
$$+ \left(\frac{P}{K_{InP}}\right) \frac{T_{sub} - D/2}{D^2}$$

In addition to the logarithmic temperature increase arising from narrow emitters, at fixed T_{sub} scaling causes ΔT_{planar} to scale in proportion to the square of circuit bandwidth. The planar term can be reduced by extreme thinning of the substrate using wafer lapping or thermal vias [12].

Given a square IC of linear dimensions W_{chip} on a large copper heat sink, the package thermal resistance is approximated by planar and spherical regions, giving $\Delta T_{package} \cong (1/2 + 1/\pi)(P_{chip}/K_{Cu} W_{chip})$. Because transistor

spacings vary as the inverse of IC bandwidth, W_{chip} must vary by the same law, and $\Delta T_{package}$ therefore increases in direct proportion to increases in circuit bandwidth with scaling.

Using these thermal relationships, and scaling from an existing UCSB/Teledyne 150 GHz IC design the dissipation, wire lengths, transistor parameters, and circuit bandwidths, we can project (Figure 2) the resulting total junction temperature rise of a 2048-HBT CML digital integrated circuit as a function of digital clock rate. The substrate is thinned aggressively with the assumed use of thermal vias: $T_{sub} = 40\ \mu\text{m} \cdot (150\,\text{GHz} / f_{clock})$ to obtain these results.

IC design constraints are application specific, hence Figure 2 only illustrates ΔT calculation. It appears however that 450 GHz f_{clock} is thermally feasible in 2000-transistor ICs, an integration scale typical of many ADCs and DACs. Higher clock rates than indicated in Figure 2 may be thermally feasible given improved circuit design. Present CML & ECL ICs must operate with a logic voltage swing $\Delta V_{\text{logic}} \cong 12 \cdot kT / q \cong 300$ mV in order to provide adequate voltage noise margin and operate with an interconnect characteristic impedance of $Z_o \cong 75\ \Omega$. This stipulates a minimum switched current of $\Delta V_{\text{logic}} / Z_o$ =4 mA per HBT. Low-voltage-swing-logic techniques, such as transimpedance input termination [13] can reduce the required HBT switched current and hence the IC dissipation.

Now let us consider scaling limits associated with contact resistivities. These must decrease in proportion to the inverse *square* of circuit bandwidth; 5 $\Omega - \mu\text{m}^2$ base $\rho_{v,b}$ contact resistivity and 2 $\Omega - \mu\text{m}^2$ emitter ρ_{ex} access resistivity are required for the 62 nm generation (440 GHz digital clock rate). In addition to the effects of doping and barrier potential, resistivity of *ex-situ* deposited contacts is strongly influenced by surface oxides and cleaning procedures. For the base contacts, we observe the lowest resistivity with Pd solid-phase-reaction contacts [14], which penetrate oxides.

On recently reported HBTs [15,16], we measured 5 $\Omega - \mu\text{m}^2$ for the emitter resistivity and < 5 $\Omega - \mu\text{m}^2$ for the base resistivity. The emitter thus presents the more serious challenge. Therefore, we have recently investigated methods to reduce the emitter contact resistivity. Details will be reported elsewhere [17] ; several processes have been developed which provide between 0.5 and 1.0 $\Omega - \mu\text{m}^2$ contact resistivity to N+ InGaAs layers. Electron degeneracy in the emitter-base depletion layer contributes an effective increase in the aggregate emitter resistance, proportional to $1/m^*_{InP}$, of ~1.0 $\Omega - \mu\text{m}^2$.

Including the effects of emitter-base degeneracy, the emitter and base contact resistivities now achieved at UCSB are sufficient to meet the requirements for both the 125 nm and 65 nm scaling generations. Junction widths must be reduced and epitaxial layers thinned, but this simply requires efforts, albeit extensive, in development of the necessary device fabrication processes. Transistors with simultaneous 1.0 THz f_τ and 1.5 THz $f_{\max}$ appear to be feasible. Such transistors would enable 450 GHz digital clock rates and 750 GHz power amplifiers. In the short term, our efforts now focus on realizing the 125 nm scaling generation device of Table 1. In the longer term, further efforts on base and emitter contact resistivity will likely have sufficient success to meet the requirements for the 31 nm scaling generation, a device $\sqrt{2}:1$ faster than the 62 nm device of Table 1. Note that the scaling requirements for sub-mm-wave amplification are somewhat less challenging than for high-speed digital ICs. In particular, integration scales are lower and hence IC thermal dissipation is a less serious challenge. Further, mm-wave power amplifiers can tolerate higher emitter access resistivities than ECL digital circuits; the scaling roadmap of Table 1 reflects digital circuit requirements for R_{ex}.

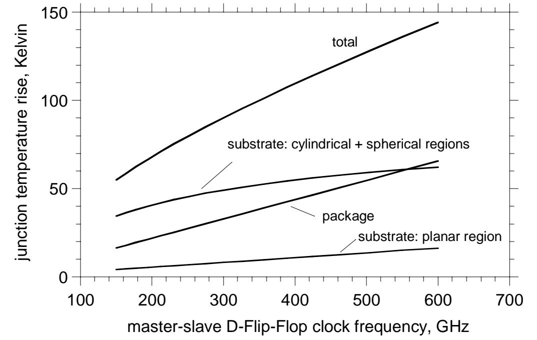

Figure 2: Calculated package and substrate temperatures rise, as a function of digital clock rate, for a 2048-HBT CML integrated circuit.

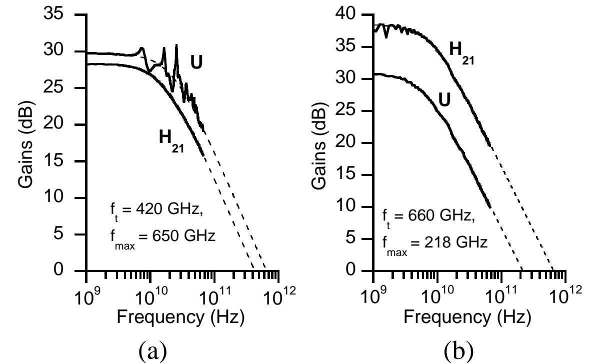

Figure 3: Measured microwave gains of representative mesa DHBTs. (a) Gains of a DHBT having T_c=150 nm, T_b=30 nm, and W_e=250 nm, biased at J_e=12 mA/μm^2. (b) Gains of a DHBT having T_c=60 nm, T_b=14 nm, and W_e=400 nm, biased at J_e=13 mA/μm^2. Griffith *et al* will report an HBT with 780 GHz $f_{\max}$ at this conference.

III. InP Field-Effect Transistors

Given recent interest in the use of III-V materials in future MOSFETs in VLSI [4,5,6,7], we examine several challenges faced in scaling these devices to meet the 22 nm ITRS performance goals. These scaling difficulties must also be addressed to enable development of > 1-THz-f_τ InGaAs Schottky-barrier field-effect transistors (HEMTs). Such devices would enable low-noise preamplifiers for sub-mm-wave radio receivers in the 50-500 GHz range.

Silicon MOSFETs were until recently mobility-limited, and significantly improved FET drive currents [18] were obtained through strain-induced increases in channel mobility. Investigation of high-mobility channel materials for VLSI was consequently motivated by the potential for further improved drive current (I_d / W_g) and decreased digital delay ($C_{total} \Delta V / I_d$). Yet, the high mobility of InGaAs arises from a

low electron effective mass m_e^*, and low m_e^* introduces numerous scaling difficulties. Further, short-channel InGaAs FETs have nearly-velocity-limited transconductance, and the benefit of high channel mobility is thus somewhat unclear. Finally, it has taken the past 17 years to double the bandwidth of InGaAs HEMTs [19, 20, 21], which suggests that serious scaling difficulties are already present.

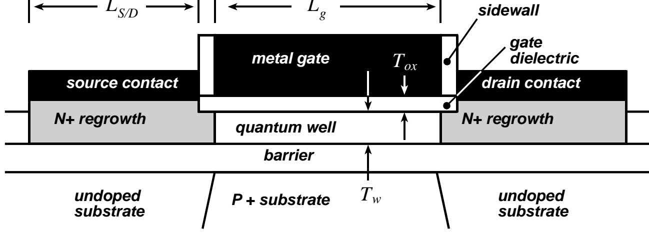

Figure 4: Cross-section of InP-based MOSFET or HEMT with regrown extrinsic N+ InGaAs/InAs source and drain regions. The gate stripe extends a distance W_g perpendicular to the figure. L_g is the gate length, T_{ox} the gate dielectric thickness, and T_w the thickness of the InGaAs quantum well.

For application in VLSI, low-surface-state-density gate dielectric formation, III-V growth on Si, tunneling leakage currents, and development of wideband P-channel devices are all serious challenges, but are beyond the scope of this discussion.

First consider idealized FET scaling laws [22] in the high-mobility (velocity-limited) regime, assuming the structure of Figure 4. The device transconductance is $g_m \sim c_{eq} v_{exit} W_g$, where $1/c_{eq} \approx T_{ox}/\varepsilon_{ox} + T_w/2\varepsilon_{well}$ and v_{exit}, the velocity at which carriers exit from the inversion layer into the high-field gate-drain depletion region, is $\sim (kT/m_e^*)^{1/2} = 3.3 \cdot 10^7$ cm/s for low 2DEG carrier concentrations but increases towards the Fermi velocity in the limit of highly degenerate 2DEG concentrations. Assuming negligible source and drain overlap with the gate, and including fringing capacitances [23] , $C_{gs} \approx C_{gso} + C_{gs,\text{fringing}}$, where $C_{gso} = c_{eq} L_g W_g$ and $C_{gs,\text{fringing}} \approx 3\varepsilon_{ox}/8 \approx C_{gd}$. HEMTs have a parasitic source-drain capacitance $C_{ds} \approx \varepsilon_{InGaAs} W_g$, while MOSFETs with doped substrates have source & drain capacitances to the substrate of $C_{s-b} = C_{d-b} \approx \varepsilon_{InGaAs} W_g L_{S/D} / T_{depletion}$. It is critical to note that only C_{gso} varies in proportion to L_g. If the N+ source and drain regrowths have sheet resistances ρ_{N+} and specific contact resistivities ρ_c, then (given wide contacts) the source and drain resistances are $R_s = R_d = (\rho_{N+} \rho_c)^{0.5} / W_g$; if $L_{S/D}$ is small, then $R_s = R_d = \rho_c / W_g L_{S/D}$.

Let us now scale this device for 2:1 increased bandwidth. As with bipolar transistor scaling, we seek a 2:1 reduction of all capacitances while maintaining constant g_m, constant R_s and R_d, constant DC current, and constant DC voltages. Because C_{gso} is the only capacitance dependent upon the gate length, it is not sufficient to reduce L_g by 2:1 with fixed T_{ox} and fixed T_w. Instead, L_g, T_{ox}, T_w, and W_g must all be reduced 2:1. Further, IC density constraints will force a 2:1 reduction in $L_{S/D}$ and process constraints a similar reduction in $T_{depletion}$. To maintain constant R_s and R_d, ρ_c must be reduced 4:1 ; contact resistivities face the same scaling requirements in both field-effect and bipolar transistors. With these geometric changes, all device capacitances are reduced 2:1, while g_m, R_s and R_d remain constant. Maintaining a constant g_m/g_{ds} ratio also demands that T_{ox} and T_w scale in proportion to L_g.

InGaAs FETs with ~22-35 nm L_g cannot easily follow these laws, and device bandwidth consequently fails to increase in inverse proportion to the scaled dimensions. First, the low effective mass of high-mobility materials substantially reduces the 2-dimensional density of states [24] and consequently the transconductance. Inclusive of this effect $1/c_{eq} \approx T_{ox}/\varepsilon_{ox} + T_w/2\varepsilon_{well} + 1/c_{DOS}$, where the density of states equivalent capacitance is $c_{DOS} = q^2 m_e^* / \pi\hbar^2$. Unlike Si, in InGaAs, c_{DOS} is small. A 2:1 reduction in T_{ox} and T_w consequently increases g_m/W_g by less than 2:1. In the limit of thin gate dielectics, c_{DOS} becomes the dominant component of c_{eq}, g_m/W_g no longer increases with scaling, and the time constants $C_{gs,fringing}/g_m$, C_{gd}/g_m, C_{ds}/g_m, C_{d-b}/g_m, and C_{s-b}/g_m remain constant; the transistor bandwidth is then limited by these parasitic capacitances.

While the well thickness T_w should scale in proportion to L_g so as to both proportionally scale g_m/W_g and to maintain constant g_m/g_{ds}, thin wells present two difficulties. Thin wells show reduced channel mobility [25] due to interface roughness scattering. Further, with thin wells the combined effects of the high ground state energy ($E_{well} \sim \hbar^2\pi^2/2m_e^* T_w^2$ in the infinite-well approximation) and high electron density ($E_f - E_{well} \cong q^2 n_s / c_{DOS}$) can together raise the channel Fermi energy to that of the L valley minimum, populating these bands and greatly reducing mobility. The low electron effective mass therefore constrains both vertical scaling and the maximum useful channel carrier density.

Fortunately, very large channel mobility is not required. Because $I_d \approx c_{eq} v_{exit} W_g (V_{gs} - V_{th} - v_{exit} L_g / \mu_n)$ for $(V_{gs} - V_{th}) >> v_{exit} L_g / \mu_n$, it is sufficient to maintain a mobility $\mu_n >> v_{exit} L_g / (V_{gs} - V_{th})$. In particular, if $(V_{gs} - V_{th}) = 0.7$ V, $v_{exit} = 3.3 \cdot 10^7$ cm/s and $L_g = 22$ nm, $\mu_n = 1300$ cm^2/V·s results in I_d only 10% below that which would result from infinite mobility.

In our efforts to develop InGaAs-channel MOSFETs for the ITRS $L_g = 22$ nm generation, we seek $I_d/W_g > 3.5$ mA/μm at $(V_{gs} - V_{th}) = 0.7$ V and consequently require $g_m/W_g > 5$ mS/μm. Assuming $v_{exit} = 3.3 \cdot 10^7$ cm/s, this implies $N_s \cong 7 \cdot 10^{12}/\text{cm}^2$. Aspect ratio requirements stipulate that $T_w < 5$ nm. Assuming infinitely deep wells and parabolic bands, the L valleys will be populated for $N_s > 6 \cdot 10^{12}/\text{cm}^2$; under more realistic calculations this may not occur until N_s substantially exceeds $10^{13}/\text{cm}^2$. Regarding these requirements, preliminary mobility data from growth experiments is encouraging. At the target g_m/W_g, $R_s W_g$ should be below ~20 Ω-μm, well below that now achieved with InGaAs HEMTs [20]; we seek to achieve such low access resistivities using self-aligned N+ InGaAs regrown source-drain regions in combination with < 1 $\Omega-\mu\text{m}^2$ resistivity Ohmic contacts similar to those now employed at UCSB for emitter contacts to HBTs.

ACKNOWLEDGMENTS

Ongoing development of InGaAs/InP-channel MOSFETs at UCSB is a collaboration with UCSD, Stanford, U. Minnesota, and U. Massachusetts, and we acknowledge the contributions of Professors Yuan Taur, Paul McIntyre, Susanne Stemmer, Chris Palmstrøm, James Harris, Max Fischetti, Peter Asbeck, Andy Kummel, Chris Van de Walle, and of their students and postdoctoral researchers.

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