A Low Computation Adaptive Technique for Blind Correction of Mismatch Errors in Multichannel Time-Interleaved ADCs

Munkyo Seo, Mark J. W. Rodwell, and Upamanyu Madhow

Department of Electrical and Computer Engineering,
University of California, Santa Barbara, CA 93106 USA
Email: {mkseo, rodwell, madhow}@ece.ucsb.edu

Abstract—**A computationally efficient technique is introduced for the adaptive blind correction of *M*-channel time-interleaved analog-to-digital converters (TIADC). Under wide-sense stationary (WSS) input assumption, gain and timing errors are estimated by monitoring the shift-dependence of TIADC output autocorrelation. Sampling time mismatches are directly compensated by adjusting individual clock timing offsets in analog domain. All other signal processing including blind parameter adaptation is done in digital domain. This mixed-domain technique takes advantage of each domain to dramatically reduce computational requirement on the digital side. As a by-product, convergence is guaranteed under mild conditions with arbitrary number of channels. Minimum resolution and dynamic range of the sampling timing control circuitry are important, but other imperfections are not critical, due to the implicit feedback operation. Experimental demonstration is performed by a proof-of-concept, *M*=4 400-MSPS real-time setup. After 300 iterations, mismatch spurs are suppressed by more than 40-dB, down to ~80dB below the signal at ~171MHz. This is the first proposal and demonstration of low-computation blind technique with guaranteed convergence.**

I. INTRODUCTION

A time-interleaved analog-to-digital converter (TIADC) is a scalable architecture for high sampling rates. A number of sub-converters cyclically sample the input signal, and multiple outputs are combined to yield a single digital stream. The collective sampling rate is therefore proportional to the number of channels. It has been well known, however, that the spectral performance of a TIADC is limited by aliasing spectra due to mismatches in sub-converter gain, sampling time, etc [1], [11]. Currently known correction techniques can be categorized into training (foreground) [2], [11] and blind (background) methods [3]-[10], [12]-[13]. In this paper, we are interested in blind methods which are generally capable of uninterrupted operation and of tracking time-varying errors. There have been proposed a variety of blind methods with different accomplishments and limitations. Some perform error detection and correction entirely in digital domain [6]-[8], [12], while others use both analog and digital domain [3]-[5], [9]-[10].

Previous mixed-domain methods typically involve special analog signal processing (e.g. adding a known signal to the input) to facilitate mismatch estimation, which may potentially compromise input signal integrity. Purely digital techniques keep the analog path intact, but the computational cost is generally high, partly due to long fractional-delay filters for timing correction (including the calculation of their coefficients) and partly due to the complexity of the iterative algorithm. For both classes of techniques, special assumptions (e.g. reduced input bandwidth, limited number of TIADC channels, wide-sense stationarity, etc) are necessary to make the problem of *blind* estimation solvable.

We propose in this paper a new adaptive blind method under a wide-sense stationary (WSS) input assumption. This is along the same line as the authors' prior work [12]-[13], but our main focus here is to significantly reduce the computational complexity to enable very low-cost, real-time operation. This requires redefinition of the problem from the beginning. Noting that the digital filter correction of timing errors is costly, we propose direct tuning of sampling clock timing, leaving input analog signal path untouched. Several benefits follow from this. First, fractional-delay filters as well as their coefficient calculation are no longer necessary. Second, sampling time correction is now *ideal* up to full Nyquist input bandwidth, which is not possible with finitely long fractional-delay filters. Third, and most importantly, convergence is guaranteed by a simple iteration rule when combined with the autocorrelation-based blind estimation method. All other signal processing is implemented in the digital domain after the analog-to-digital (A/D) conversion. No restriction is put on the number of TIADC channels or input signal bandwidth, as long as it satisfies Nyquist sampling criterion.

II. SYSTEM CONFIGURATION

Fig. 1 shows a block diagram of the *M*=4 TIADC structure with the proposed mismatch correction scheme. Each of four sub-converters successively samples the analog input signal $x(t)$ every $4T_s$ such that the overall sampling rate is f_s (=1/T_s). Listed below are pertinent assumptions and clarifications with references to Fig.1.

- The input $x(t)$ is bandlimited to $\frac{1}{2}f_s$, zero-mean and WSS. No further information about $x(t)$ is known.
- Sub-converters' bit-resolution is high enough to ignore quantization effects.
- Sub-converter offset mismatch is independently corrected (e.g., first estimate channel offset by averaging each channel output and subtracting it out).
- The k-th sub-converter has *intrinsic* gain and sampling time error of (G^*_k, Δt^*_k), which is unknown.
- The *estimate* of intrinsic gain and timing error is ($\tilde{G}_k$, $\tilde{\Delta t}_k$), which is updated every iteration by observing the final TIADC output $z[n]$.
- Correction of intrinsic timing error, either complete or partial, is achieved by adjusting the timing offset of each channel's sampling clock according to the estimate $\tilde{\Delta t}_k$.
- Correction of intrinsic gain error is performed, either complete or partial, by directly dividing the sub-converter output by the gain estimate $\tilde{G}_k$.

- The *residual* mismatch error is, by definition, $(\tilde{G}_k - G^*_k, \Delta\tilde{t}_k - \Delta t^*_k)$, which is present at the final output $z[n]$.
- Finally, the magnitude of intrinsic mismatches are small. The precise interpretation will be made clear in the context.

The final per-channel output $z_k[n]$ is, therefore, a scaled, time-shifted, and under-sampled version of $x(t)$ given by

$$z_k[n] = \begin{cases} \dfrac{G^*_k}{\tilde{G}_k} x\!\left(nT_s + \Delta t^*_k - \Delta\tilde{t}_k\right), & \text{if } (n \bmod M) = k \\ 0, & \text{otherwise} \end{cases} \tag{1}$$

where M is the number of channels. The final reconstructed output $z[n]$ is obtained by summing all $z_k[n]$'s. It follows that zero residual error implies $z[n] = x(nT_s)$. Sub-converter digital output $y_k[n]$ is related to $z_k[n]$ by

$$y_k[n] = \tilde{G}_k z_k[n] \tag{2}$$

Note that $z_k[n]$'s and $y_k[n]$'s are both observable and carry the same information since $\tilde{G}_k$'s are known to the algorithm.

III. TIADC Output Autocorrelation Properties

Under the input WSS assumption, output autocorrelation plays the role of a mismatch indicator, which drives the iterative convergence process. Thus, the proposed technique can be best introduced by first examining the properties of output autocorrelation associated with intrinsic mismatches.

Since the input $x(t)$ is WSS, its autocorrelation is shift-independent, and depends only on the time lag between two time points. Thus, the autocorrelation of $x(t)$ is

$$R_x(\tau) = E[x(t+\tau)x(\tau)], \text{ for all } t. $$

If there are nonzero residual mismatches, the TIADC output $z[n]$ no longer satisfies WSS properties and its autocorrelation is shift-dependent. Specifically, we focus on the subset of TIADC output autocorrelation with zero and unit lag, referenced to each channel as follows.

$$R_{z,k}[0] = E\!\left[z_k^2[n]\right] \tag{3}$$

$$R_{z,k}[1] = E\!\left[z_k[n]z_{(k+1)\bmod M}[n+1]\right] \tag{4}$$

These can be rewritten in terms of the input autocorrelation $R_x(\tau)$, by using (1), as follows.

$$R_{z,k}[0] = \left(\frac{G^*_k}{\tilde{G}_k}\right)^2 R_x(0) \tag{5}$$

$$R_{z,k}[1] = \frac{G^*_k G^*_{(k+1)\bmod M}}{\tilde{G}_k \tilde{G}_{(k+1)\bmod M}}\left(R_x(T_s) + \left(\delta^*_k - \tilde{\delta}_k\right)\frac{dR_x}{d\tau}\bigg|_{\tau=T_s}\right) \tag{6}$$

where δ^*_k and $\tilde{\delta}_k$ is the intrinsic and estimated *adjacent-channel* timing offset between k-th and the next cyclic channel, respectively, defined by

$$\begin{aligned} \delta^*_k &\equiv \Delta t^*_k - \Delta t^*_{(k+1)\bmod M}, \\ \tilde{\delta}_k &\equiv \Delta\tilde{t}_k - \Delta\tilde{t}_{(k+1)\bmod M}. \end{aligned} \tag{7}$$

The first-order approximation in (6) is valid as long as the adjacent-channel timing offset error $|\delta^*_k - \tilde{\delta}_k|$ is small compared to T_s. Since the autocorrelation of bandlimited signals is smooth, its derivative in (6) is well-defined. We note that $R_{z,k}[m]$'s are available by measurement, but $R_x(\tau)$'s and its derivative are unknown. The following key observations are made from (5) and (6).

1) Residual gain mismatches affect both $R_{z,k}[0]$ and $R_{z,k}[1]$, but timing errors influence only $R_{z,k}[1]$.

2) No residual mismatch condition: If there is no residual gain and timing mismatch, all output autocorrelations are the same, i.e. $R_{z,0}[m] = R_{z,1}[m] = \ldots R_{z,M-1}[m]$ for $m=0$ and 1. In other words, $R_{z,k}[m]$'s are *equalized*, and *shift-independence* has been attained.

3) Equalized autocorrelation condition: If all $R_{z,k}[0]$'s and $R_{z,k}[1]$'s are made equal to some respective reference, gain estimates are equal to intrinsic ones up to a common scale factor, i.e. $\tilde{G}_0/G^*_0 = \tilde{G}_1/G^*_1 = \ldots \tilde{G}_{M-1}/G^*_{M-1}$. Furthermore, timing estimates are also equal to intrinsic ones up to a common shift, i.e. $\Delta\tilde{t}_0 - \Delta t^*_0 = \Delta\tilde{t}_1 - \Delta t^*_1 = \ldots \Delta\tilde{t}_{M-1} - \Delta t^*_{M-1}$.

The proof follows from (5)-(7) [14], but we reiterate the key assumption that *the input $x(t)$ is WSS and bandlimited to $\frac{1}{2}f_s$.* If we disregard common scaling and time-shifting which is linear time-invariant operation, *2)* and *3)* together establishes that *the attainment of equalization, or equivalently shift-independence, of $R_{z,k}[0]$'s and $R_{z,k}[1]$'s is a necessary and sufficient condition for perfect mismatch correction.*

IV. Algorithm description and Convergence Analysis

In light of the previous discussion, we now develop an iterative algorithm to achieve the equalization of zero-lag ($R_{z,k}[0]$) and unit-lag ($R_{z,k}[1]$) output autocorrelations. These correlations can be empirically obtained using (3) and (4) after replacing $E[\cdot]$ with time-averaging over N samples per channel (and per iteration),

$$R_{z,k}[0] = \frac{1}{N}\sum_{n=0}^{N-1} z_k[n]^2, \tag{8}$$

$$R_{z,k}[1] = \frac{1}{N-1}\sum_{n=0}^{N-2} z_k[n]z_{(k+1)\bmod M}[n+1]. \tag{9}$$

For the sake of simplicity, we will maintain same notations for autocorrelations regardless of whether statistical expectation (e.g. (3) and (4)) or time-averaging (e.g. (8) and (9)) is associated. The context will make it clear which operation is assumed.

A. Selection of Equalization Reference

One of the sensible choices of equalization reference is the following average autocorrelations,

$$R_{z,ref}[0] = \frac{1}{M}\sum_{k=0}^{M-1} \tilde{G}_k^2 R_{z,k}[0], \tag{10}$$

$$R_{z,ref}[1] = \frac{1}{M}\sum_{k=0}^{M-1} R_{z,k}[1] \tag{11}$$

where $R_{z,ref}[0]$ and $R_{z,ref}[1]$ is the equalization reference for $R_{z,k}[0]$'s and $R_{z,k}[1]$'s, respectively. Note that (10) is actually the average autocorrelation measured at sub-converter output $y_k[n]$'s, which is obtained from $R_{z,k}[0]$'s after moving the observation point using (2).

For convenience, we ignore common time delay and assume the following in further discussions.

$$G_{RMS}^* = 1, \quad \text{where} \quad G_{RMS}^* \equiv \sqrt{(1/M)\sum_{k=0}^{M-1} G_k^{*2}}. \tag{12}$$

It can be shown that the equalization of $R_{z,k}[0]$ to the reference (10) along with the above constraint leads to the steady-state gain estimate of $\tilde{G}_k = \pm G_k^*$ for all k. Since the polarity of intrinsic gain is known in practice, we can consider $\tilde{G}_k = G_k^*$ as the only pair of gain parameters which equalizes $R_{z,k}[0]$. The implicit normalization associated with (12) effectively amplifies the TIADC output by G_{RMS}^*. This will be acceptable, however, in most practical cases, especially under small mismatch regime. With (12) assumed, equalization reference in (10) and (11) can be rewritten in terms of the TIADC input autocorrelation by using (5) and (6) as follows.

$$R_{z,ref}[0] = R_x(0), \tag{13}$$

$$R_{z,ref}[1] = R_x(T_s), \quad \text{if no residual gain error.} \tag{14}$$

The relationship (14) is true only if there is no residual gain error. Note that (13) and (14) is useful for algorithm *analysis*, while (10) and (11) is for actual *implementation*.

B. Gain and Timing Estimate Recursion

Having defined $R_{z,ref}[0]$ and $R_{z,ref}[1]$, we will now set up iterative equalization process. Examination of (6) suggests that $\tilde{\delta}_k$ is more convenient to update than $\Delta\tilde{t}_k$, since this decouples timing update for each channel. Once $\tilde{\delta}_k$'s are updated, $\Delta\tilde{t}_k$'s can be retrieved from (7),

$$\Delta\tilde{t}_k = \sum_{n=0}^{k-1}\tilde{\delta}_n - \frac{1}{M}\sum_{m=0}^{M-2}(M-1-m)\tilde{\delta}_m, \tag{15}$$

where the following is assumed to uniquely determine $\Delta\tilde{t}_k$'s ($\tilde{\delta}_k$'s define only the timing offset error *between* adjacent converters, thus the common delay needs to be independently specified).

$$\sum_{k=1}^{M-1}\Delta\tilde{t}_k = 0. \tag{16}$$

Starting from a set of initial guesses $\tilde{G}_k^{(0)}$'s and $\tilde{\delta}_k^{(0)}$'s, estimation parameters are updated via the following recursion.

$$\tilde{G}_k^{(n+1)} = \tilde{G}_k^{(n)} + \beta_g\left(R_{z,k}^{(n)}[0] - R_{z,ref}^{(n)}[0]\right), \quad (\beta_g > 0) \tag{17}$$

$$\tilde{\delta}_k^{(n+1)} = \tilde{\delta}_k^{(n)} - \beta_t\left(R_{z,k}^{(n)}[1] - R_{z,ref}^{(n)}[1]\right), \quad (\beta_t > 0) \tag{18}$$

where $\tilde{G}_k^{(n)}$ and $\tilde{\delta}_k^{(n)}$ is the estimate of k-th channel gain and adjacent-channel timing error at n-th iteration, respectively. The superscript with autocorrelations suggests that they are obtained from n-th batch of data, using (8) and (9). Once $R_{z,k}[0]$'s and $R_{z,k}[1]$'s are all equalized to a respective reference, the driving term in the parenthesis in (17) and (18) is zero, convergence being achieved. The stability and speed of convergence is controlled by β_g and β_t which will be referred to as convergence parameters. Convergence analysis will follow soon, but for the present discussion it suffices to assume β_g and β_t are sufficiently small.

It can be proven that the gain update by (17) always decreases the magnitude of residual error [14]. For example, suppose $R_{z,k}^{(n)}[0] - R_{z,ref}^{(n)}[0] > 0$ for some k and n. This implies k-th channel intrinsic gain is underestimated as seen by comparing (5) and (13).

We can verify that the recursion (17) will correctly increase the current gain estimate.

Similar proof can be given regarding the timing estimate recursion (18) under gain-matched condition [14]. In this case, however, we must know the sign of $dR_x/d\tau$ to correctly decide whether to increase or decrease the current timing estimate. This can be seen by comparing (6) and (14) with perfect gain matching. If no such sign information is available, then we should rely on empirical methods such as finite-difference methods or general search algorithm [8], [12]-[13]. It turns out that if $x(t)$ is bandlimited to $\frac{1}{2}f_s$, $dR_x/d\tau$ is always negative [14]. This property let us make parameter adjustment with *a priori* known direction of decreasing error. Therefore, every recursion by (18) is guaranteed to decrease the magnitude of residual timing error, enabling simpler and more efficient minimization than general empirical methods. This benefit directly comes from the deliberate combination of techniques, i.e. error detection by looking at output autocorrelation and timing correction by adjusting sampling clock in analog domain, which is among the contributions of the present paper.

C. Convergence Analysis

Let $\gamma_k^{(n)} \equiv \tilde{G}_k^{(n)} - G_k^*$ and $\varepsilon_k^{(n)} \equiv \tilde{\delta}_k^{(n)} - \delta_k^*$ be the n-th iteration residual gain and adjacent timing offset error for k-th channel, respectively. We can show that under small mismatch condition $\gamma_k^{(n)}$ and $\varepsilon_k^{(n)}$ follows a geometric series [14],

$$\gamma_k^{(n)} = \left(1 - 2\beta_g R_x(0)\right)^n \gamma_k^{(0)}, \tag{19}$$

$$\varepsilon_k^{(n)} = \left(1 - \beta_t\left|\frac{dR_x}{d\tau}\right|_{\tau=T_s}\right)^n \varepsilon_k^{(0)}, \tag{20}$$

where perfect gain-matching is assumed in (20). For monotonous (as opposed to oscillatory) convergence, β_g and β_t must lie in the following range.

$$0 < \beta_g < \frac{1}{2R_x(0)}, \tag{21}$$

$$0 < \beta_t < \frac{1}{\left|\dfrac{dR_x}{d\tau}\right|_{\tau=T_s}}, \tag{22}$$

which implies that sufficiently small values of β_g and β_t will guarantee convergence. Also can be inferred is that large values of β_g and β_t will accelerate convergence as long as (21) and (22) are satisfied. This will, however, necessarily amplify noise in the driving term (the one in the parenthesis in (17) and (18)), making the steady-state estimate noisy. With same β_g and β_t, on the other hand, the gain and timing estimate will generally converge faster with higher input power and fast-changing input signal, respectively, since the geometric ratio in (19) and (20) becomes smaller.

D. Other Considerations

Previous analysis assumed perfect gain match when discussing timing estimate convergence for simplicity. Equation (6) suggests, however, that any nonzero residual gain error biases timing error estimation. It can be shown that timing convergence is still achieved, since gain estimate will independently converge anyway. The caveat is that there may be an unacceptable overshoot or undershoot in timing estimate trajectories, causing dynamic range problems in actual timing control circuitry. One practical remedy, effective with

slowly time-varying mismatches, would be to initiate separate cycles of gain or timing convergence such that residual gain error is sufficiently small whenever a new cycle for timing correction starts.

There are many factors which will make the parameter estimate noisy: A/D quantization noise, clock random jitter, autocorrelation estimation error due to finite observation, sampling clock quantization error, etc. Using small values of β_g and β_t or increasing batch size N generally decreases the contribution of these noises. However, sampling clock quantization error can only be reduced by increasing its resolution (or special techniques such as dithering may help). The minimum resolution of tunable sampling-time offset should be smaller than the allowed residual mismatch level. For example, 80-dB of spurious-free dynamic range requires ~$0.0001T_s$ of timing control resolution. The proposed algorithm is tolerant to other timing imperfections such as change of slope or shift of the curve, because these can be absorbed into β_t and Δt^*_k. Feedback action will track such variations if they are slower than the adaptation. As a final remark, we note that the recursion rule can be further simplified or more sophisticated. See e.g. [15].

V. EXPERIMENTAL RESULT

A proof-of-concept real-time demonstration has been done with a 4-channel experimental setup. Four 14-bit 100-MSPS commercial chips (AD6645 from Analog Devices, Inc.) are used to obtain 400-MSPS of aggregate sampling rate. An analog input signal is evenly distributed to each converter after anti-aliasing filtering. Fig.2 shows the four-phase sampling clock circuitry with voltage-controlled delay lines. Each tunable delay line consists of a single T-section (matched to 50-ohm) with reverse-biased varactor diodes (MV104 from ON Semiconductor). The delay line provides ~$0.25T_s$ of delay tuning range across 0~3V tuning voltage (T_s=2.5nsec). Sensitivity at the center is ~$0.06T_s$/V.

A logic analyzer first captures a single batch (N=4096) of digital output from each channel. The built-in computer then performs gain correction, autocorrelation estimation ((8), (9), (10) and (11)), and parameter recursion ((17) and (18)) followed by actual timing retrieval (15) (see also Fig.1). Updated timing estimate is latched into an external 10-bit D/A converter (LTC1660 from Linear Technology), which tunes delay lines. This completes a single iteration. Update speed of the current setup is ~1 sec/iteration and limited by logic analyzer arming and acquisition.

Fig.3 compares the TIADC output spectrum before and after applying the proposed algorithm with a 171.567MHz sinusoidal input. After 300 iterations, mismatch spurs marked with 'X' has been suppressed by more than 40dB. Offset spurs and signal harmonics are also shown. Fig.4 shows convergence plots of gain and timing estimate with β_g=0.2 and β_t≈0.25. For comparison, predicted learning curves by (19) and (20) are superimposed as dotted lines. Close agreement between real and predicted estimate is observed. Small discrepancy in timing convergence plot is due to the departure of the timing control curve from a straight line. Fig.5 and Fig.6 show equalization process of output autocorrelations. Equalization is achieved after 150 iterations. Finally, Fig.7 summarizes the improvement of signal-to-mismatch spur ratio as iteration proceeds. The steady-state residual errors can be further decreased, for example by increasing batch size N or improving timing control resolution. Wideband signals with up to ~$0.4f_s$ of bandwidth has also been tested and similar results were observed, in which case autocorrelation measurement error mostly dominates the steady-state error.

VI. CONCLUSION

We have presented a new adaptive technique of blindly correcting M-channel TIADC mismatches with experimental results. The analog-domain correction of timing mismatches, combined with autocorrelation-based error detection, dramatically reduces computational complexity while guaranteeing convergence. Specifically, empirical calculation of $2M$ output autocorrelation coefficients per iteration is practically all that is necessary. Iterative process enables tracking of time-varying mismatches as well as timing control imperfection. Fundamental assumption is that the input is WSS and bandlimited. More extensive discussion and analysis will be given in later publication [14].

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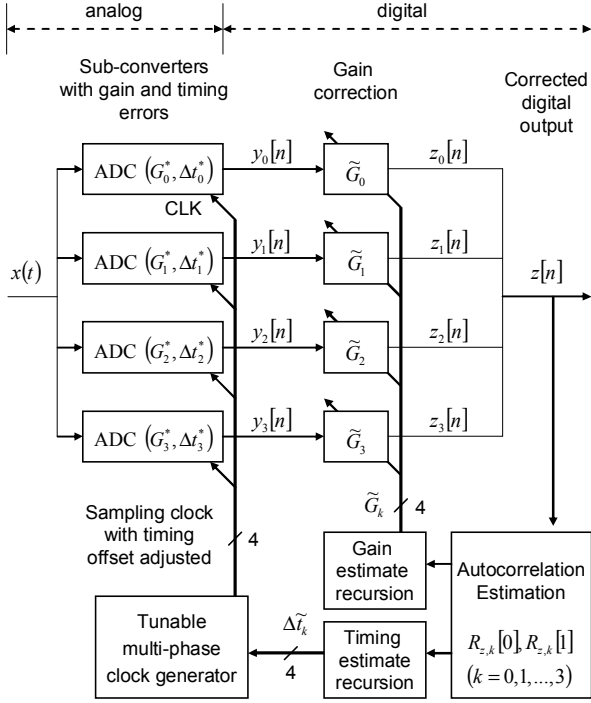[15] S. Haykin, *Adaptive Filter Theory,* Fourth-Edition, Upper Saddle River, NJ: Prentice-Hall, 2002.

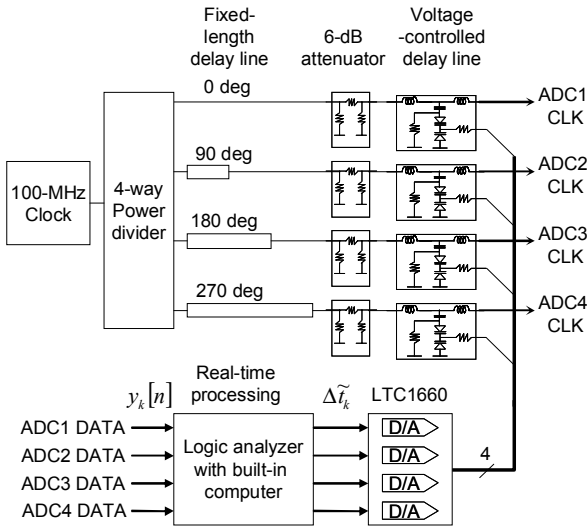Figure 1. A *M*=4 TIADC system with the proposed mismatch correction scheme.

Figure 2. Experimental four-phase clock generator with voltage-controlled delay lines using varactors. 6-dB attenuators prevent cross-line tuning by minimizing the input impedance variation of delay line across tuning ranges.
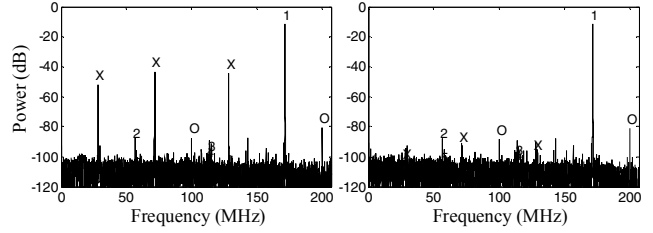
Figure 3. Measured TIADC output ($z[n]$) spectrum before (left) and after 300 iterations (right). Input is a sinusoid at 171.567MHz which is marked with '1'. Gain and sampling time mismatch spurs are labelled with 'X'. 'O' represents offset spurs. Signal harmonics have labels '2','3',…, '5'.
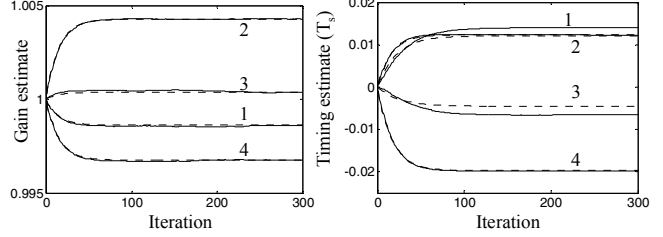

Figure 4. Convergence plot of gain (left) and timing (right) estimate with channel numbers shown. Solid lines represent measurement. Dotted lines denote predicted curves by (19) and (20) using intrinsic gain errors [0.9986 1.0043 1.0004 0.9968] and timing errors [0.0120T_s 0.0123T_s -0.0046T_s -0.0198T_s] at 171.567MHz characterized by a training method [13].
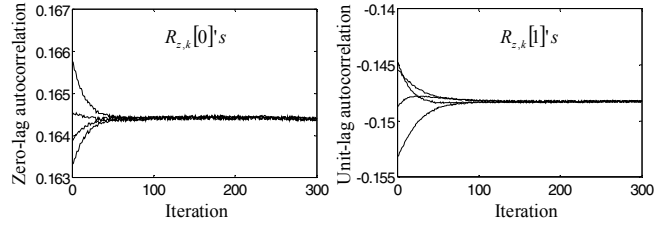

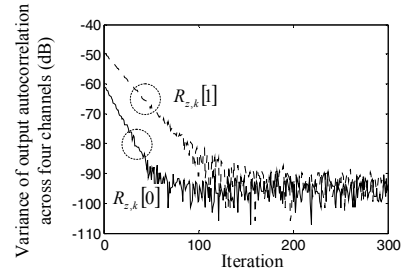Figure 5. Equalization plot of measured $R_{z,k}[0]$'s (left) and $R_{z,k}[1]$'s (right).

Figure 6. Output autocorrelation variance across channels. Equalization is achieved after ~150 iterations.
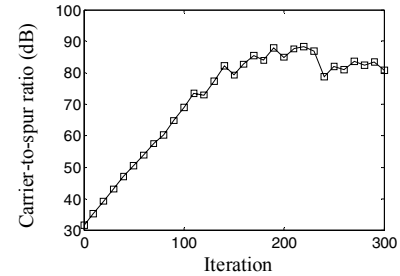

Figure 7. Measured carrier-to-spur ratio. Only gain and timing mismatch spurs (marked as 'X' in Fig. 3) are considered. On achieving convergence, mismatch spurs are suppressed by ~50dB down to ~80dB below carrier.