26.4 40Gb/s CMOS Distributed Amplifier for Fiber-Optic Communication Systems

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A distributed amplifier for 40Gb/s fiber-optic communication systems is designed in 0.18μm CMOS technology. The modified source degeneration technique with an RC combination provides a wide bandwidth and flat gain profile. Micro-strip line (MSL) consisting of metal1 and metal6 is used in layout design to realize accurate characteristic impedance. A 4dB gain and a 39GHz bandwidth in which the gain variation is within 1dB and confirmed a clear 40Gb/s output waveform. These results indicate that this technique is suitable for increasing bandwidth.

The rapid growth of the Internet drives the demands for high-speed and high-capacity transmission systems. Wavelength division multiplexing (WDM) is the most attractive technique for increasing transmission capacity, and ultra-massive-capacity transmission experiments using a WDM system with a data-rate of 40Gb/s per channel are reported. The cost and per-channel power dissipation of this system need to be reduced, making CMOS is the most promising device. Since the maximum oscillation frequency of CMOS is not higher than that of other devices, realizing analog circuits, especially baseband amplifiers up to millimeter-wave frequencies is difficult. Amplifiers with III-V and SiGe technologies are reported [1]; however, the authors believe no CMOS amplifier applicable to 40Gb/s fiber optics has been reported. In this paper, 40Gb/s CMOS distributed amplifier with modified source degeneration to achieve flat gain and wide bandwidth.

To realize a 40Gb/s amplifier, a distributed configuration in which Fig. 26.4.1 shows the conventional distributed amplifier. The bandwidth is determined by the input capacitance of the transistor and the inductance of the transmission line yielding a wider bandwidth than that of lumped element circuits. In addition, Fig. 26.4.1 also shows the equivalent circuits of the input transmission lines. Some CMOS distributed amplifiers are reported [2] [3], but they have a forward gain slope and insufficient bandwidth for 40Gb/s applications. In fiber-optic systems, the input waveforms contain various frequency-components from near DC to millimeter wave; therefore, a flat gain is required to amplify the input signal precisely. Two causes of forward gain slopes are:

1. The large input capacitance of CMOS transistor.
2. Input and output-transmission line losses due to the conductive substrate.

To solve the first problem, a modified source degeneration technique is employed. The gate attenuation α_g is quite important as it shows the upper frequency limit and the gain flatness of the distributed amplifier. α_g is represented as $\omega^2 C_{in}{}^2 R_g Z_0/2$, where Z_0 is the characteristic impedance of the synthetic transmission line. The total line loss is proportional to $e^{-N\alpha g}$, where N is the number of the unit section; Thus, the frequency-deviation of α_g is equivalent the gain profile. Figure 26.4.2 shows the simplified model of the transistor from which the real part of the input admittance of Y_{11} equals $\omega^2 C_{gs}{}^2 R_g$. It is a quadratic function of frequency, and the slope of the quadratic curve increases in proportion to $C_{gs}{}^2$. Since C_{gs} of a 0.18μm CMOS is much larger than those of other III-V FETs, it causes the forward gain slope and drastically reduces bandwidth. To reduce C_{gs}, a source resistance R_s and a source capacitance C_s is inserted rather than the conventional resistance. This is shown in Fig. 26.4.3. This R_s reduces the input capacitance, but it also acts as a series input resistance and increases the charging time of the input capacitance. When the capacitance C_s is inserted in parallel with R_s, it mitigates increasing the charging time. As shown in Fig. 26.4.3, the RC combination changes the input capacitance to $C_{gs}/(1+g_m R_s)$, reducing the effective value of C_{gs}. Figure 26.4.4 shows the real part of Y_{11} for the unit cell. The slope of Y_{11} has been improved markedly with this technique: the frequency where the slope increases sharply is higher than that of conventional unit cells. The proposed configuration consequently improves gain flatness and broadens bandwidth. Insertion of R_s lowers the extrinsic g_m of the transistor, so the gain of the amplifier is lower than that of a conventional one.

To solve the second problem, MSL comprised of metal1 and metal6 is used. This structure provides accurate characteristic impedance and avoids unwanted differences between simulation and measurements due to the conductive substrate. The MSL characteristics with EM simulation agree well with measured results even though metal1 has slots to relax the stress.

To obtain the wider bandwidth, less than 50Ω is used so as not to degrade significantly the return loss at the gate and drain terminations. Z_0 is defined by equation (1) and the cutoff frequency is determined by equation (2) in Fig. 26.4.1, indicating a lower L improves the bandwidth. Furthermore, use of a common gate transistor having a wider gate-width than that of a common source transistor in a cascode configuration makes the maximum available gain at 40GHz higher and increases the bandwidth than that of a conventional configuration.

The chip size of the amplifier is 1.1 mm x 3.0 mm and its power dissipation is 140mW. The transistor's cutoff frequency, f_T and the maximum oscillation frequency, f_{max} are 51 and 100 GHz respectively. Figure 26.4.5 shows the simulated and measured frequency characteristics of the distributed amplifier. The measured S-parameters are in good agreement with the simulated ones. The gain ripple is within ±1 dB, and up to 40GHz the group delay deviations are within ±15 ps and the input and output return losses are below –10 dB. A clear 40Gb/s output waveform is measured on wafer (Fig. 26.4.6). These results indicate that CMOS technology is promising for 40Gb/s fiber-optic communication systems.

Acknowledgements:
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References:
[1] H. Shigematsu et al., "A 54-GHz Distributed Amplifier with 6-Vpp Output for a 40-Gb/s LiNbO3 Modulator Driver," *IEEE J. Solid-State Circuits*, vol. 37, pp. 1100-1105, Sep. 2002.
[2] B. M. Ballweber et al., "A Fully Integrated 0.5-5.5 GHz CMOS Distributed Amplifier," *IEEE J. Solid-State Circuits*, vol. 35, pp. 231-239, Feb. 2000.
[3] H. T. Ahn et al., "A 0.5-8.5-GHz Fully Differential CMOS Distributed Amplifier," *IEEE J. Solid-State Circuits*, vol. 37, pp. 985-993, Aug. 2002.

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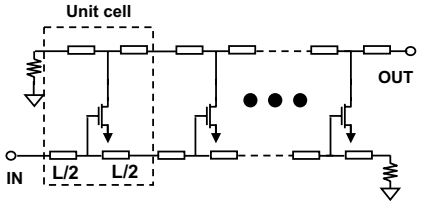
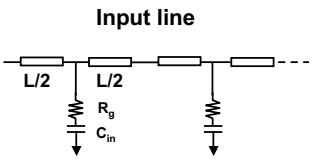


Z_0 of synthetic line:

$$Z_0 = \sqrt{LC_{in}} \quad (1)$$

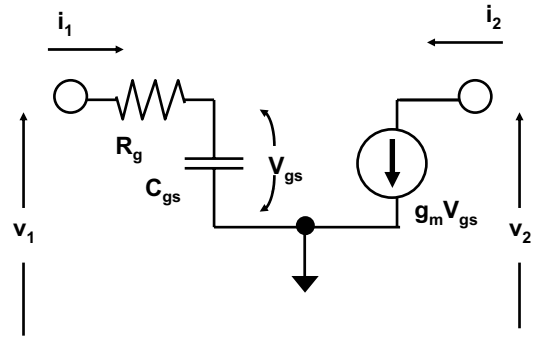
Cut-off frequency:

$$f_c = 1/\pi\sqrt{LC_{in}} \quad (2)$$



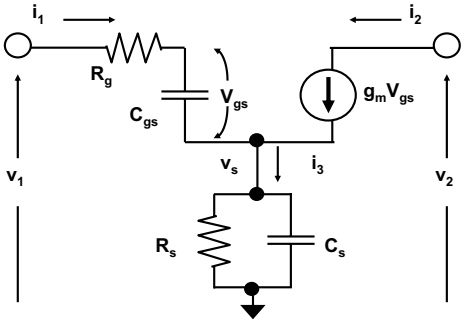
$$\alpha_g = \omega^2 C_{in}^2 R_g Z_0 / 2$$

Figure 26.4.1: Distributed amplifier.



$$Y_{11} = \omega^2 C_{gs}^2 R_g + j\omega C_{gs}$$

Figure 26.4.2: Simplified equivalent circuit of transistor.



$$v_s = V_{gs} * \{g_m R_s - j\omega(C_s R_s g_m - C_{gs})R_s\}$$

$$Y_{11} = \omega^2 C_{gs}^2 R_g / (1 + g_m R_s)^2 + j\omega C_{gs} / (1 + g_m R_s)$$

Figure 26.4.3: Modified source degeneration.

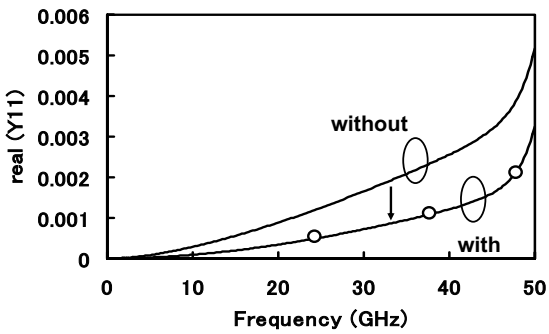


Figure 26.4.4: Real part of Y_{11} with and without RC.

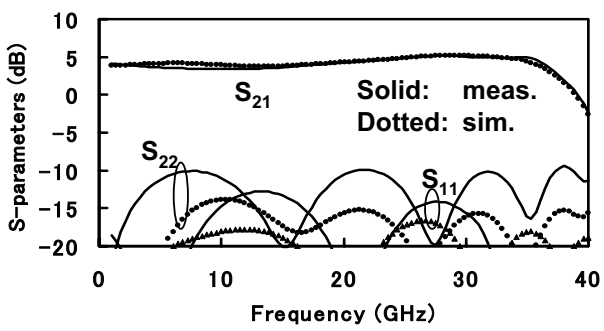


Figure 26.4.5: Frequency characteristics of the amplifier.

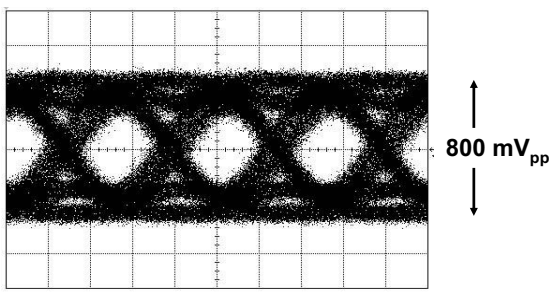


Figure 26.4.6: 40-Gb/s output waveform.

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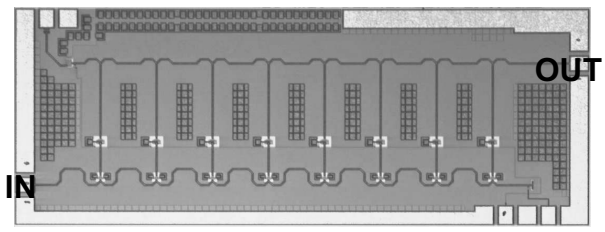

Chip size: 1.1 mm x 3.0 mm

Figure 26.4.7: Chip micrograph.

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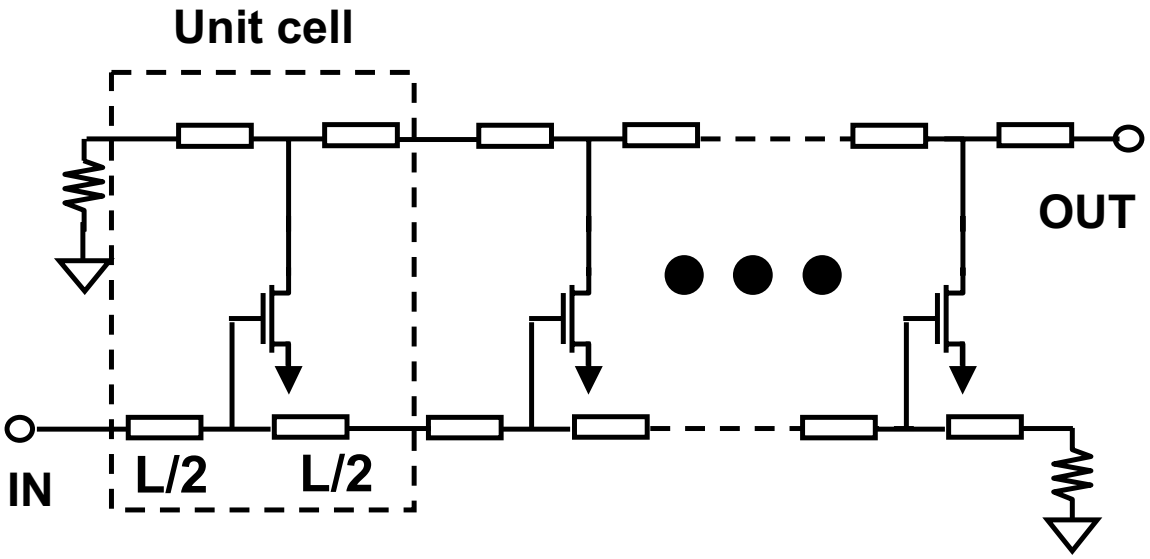

Z_0 of synthetic line:

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Cut-off frequency:

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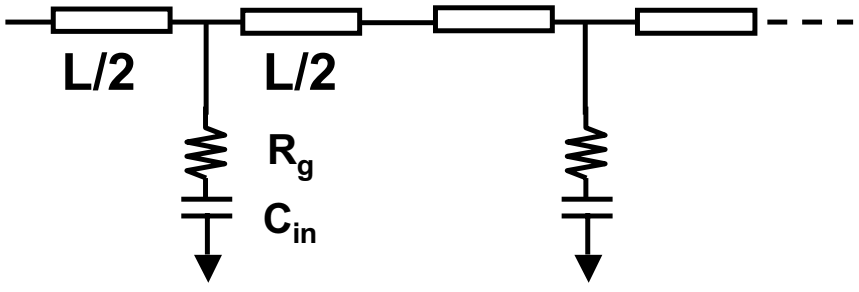
Input line



$$\alpha_g = \omega^2 C_{in}{}^2 R_g Z_0 / 2$$

Figure 26.4.1: Distributed amplifier.

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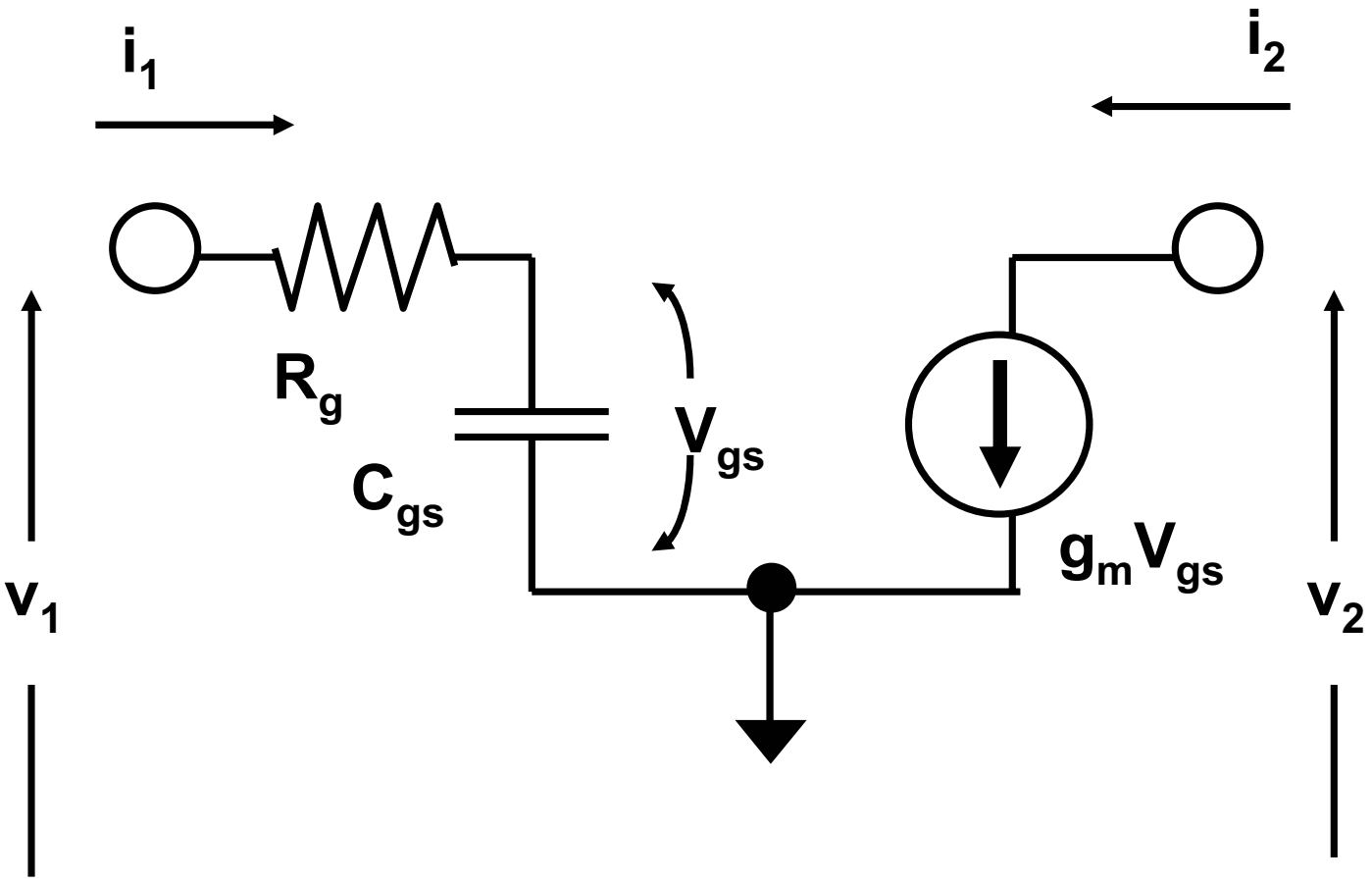

$$Y_{11} = \omega^2 C_{gs}{}^2 R_g + j\omega C_{gs}$$

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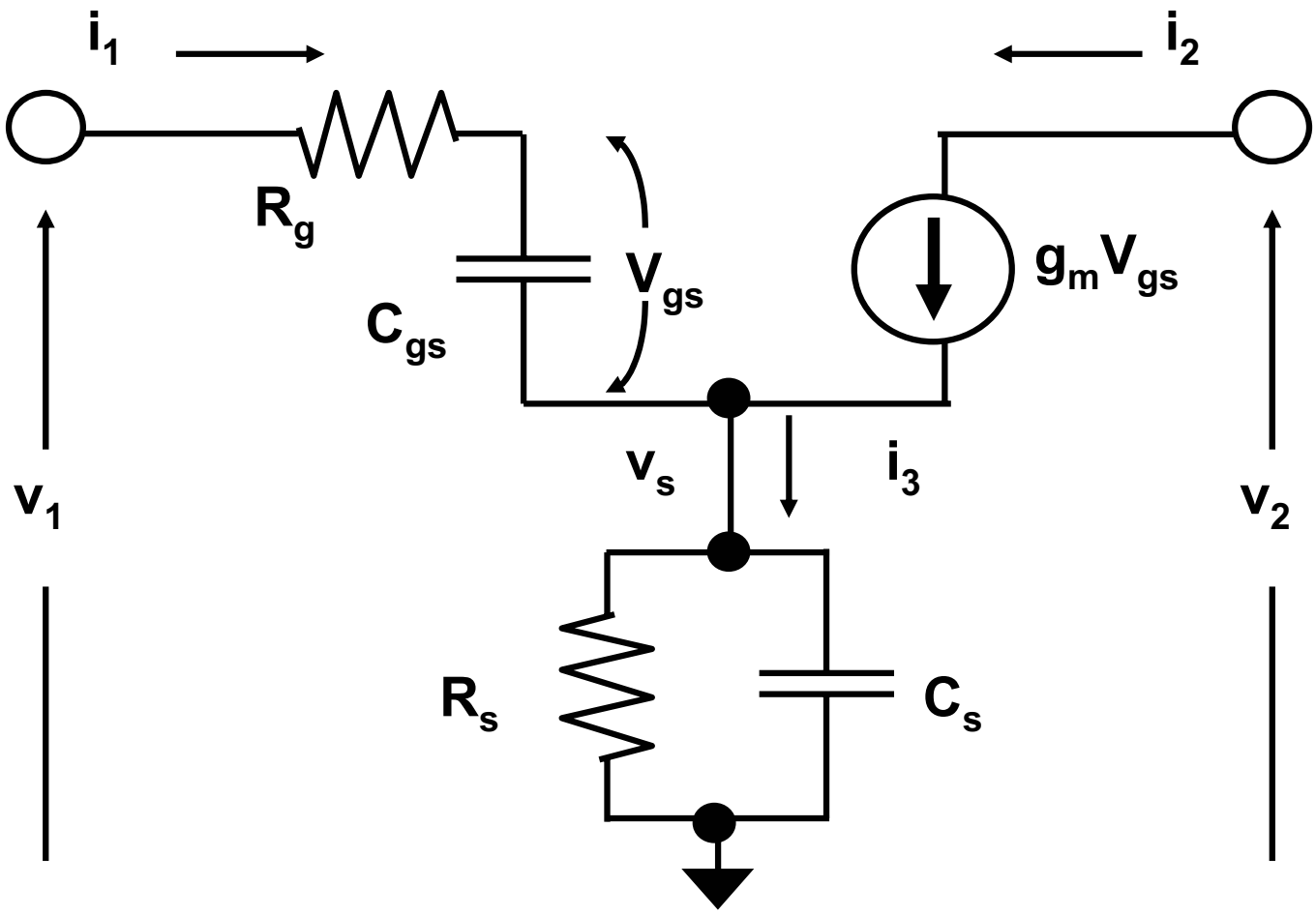

$$v_s = V_{gs} * \{g_m R_s - j\omega(C_s R_s g_m - C_{gs})R_s\}$$

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Figure 26.4.3: Modified source degeneration.

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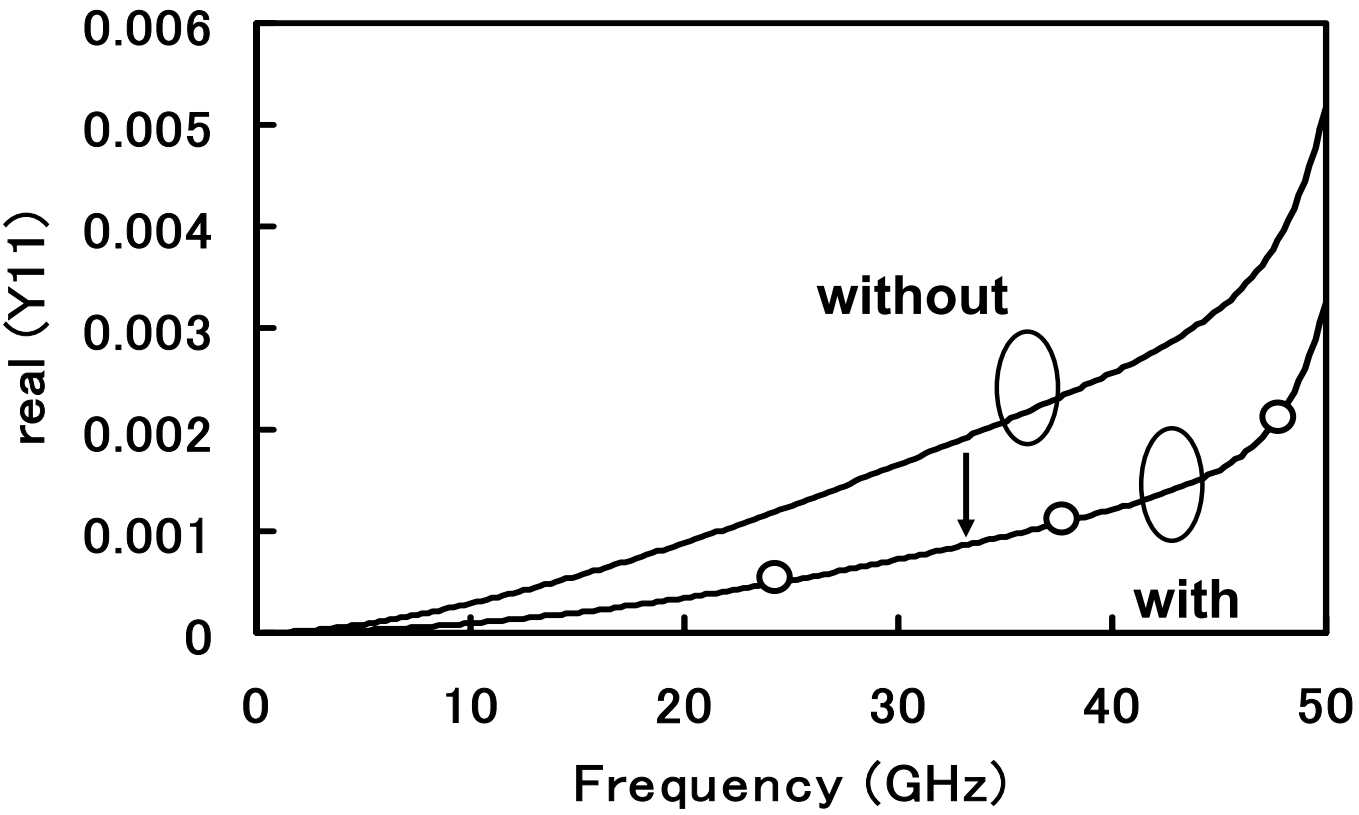

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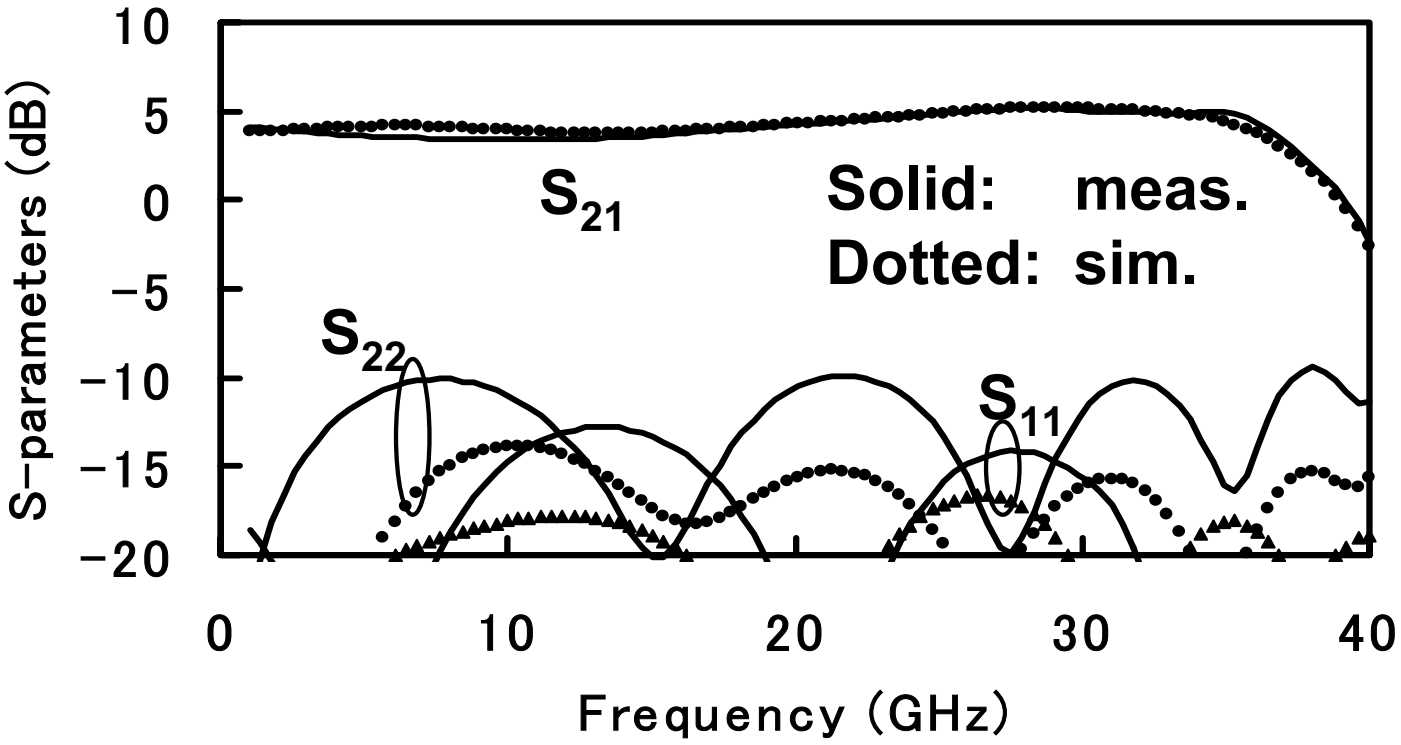

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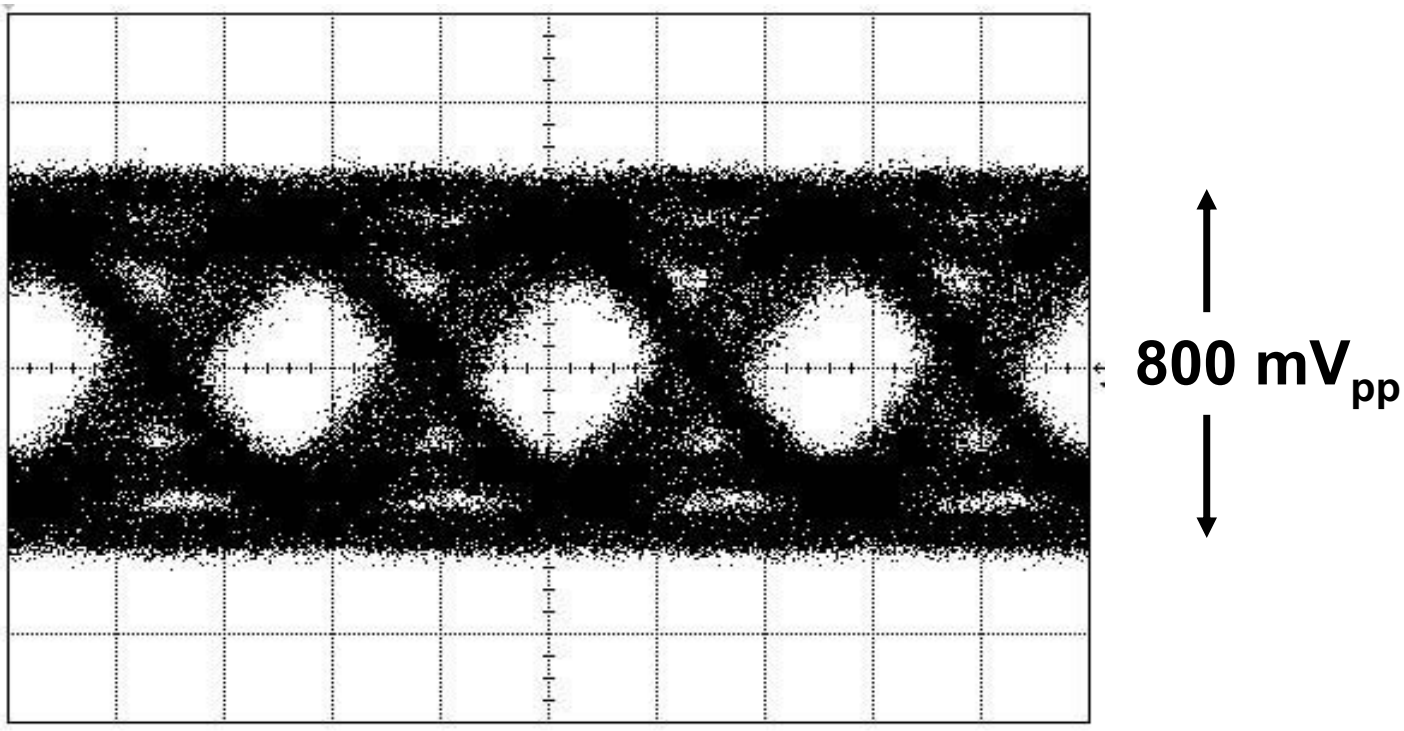

Figure 26.4.6: 40-Gb/s output waveform.

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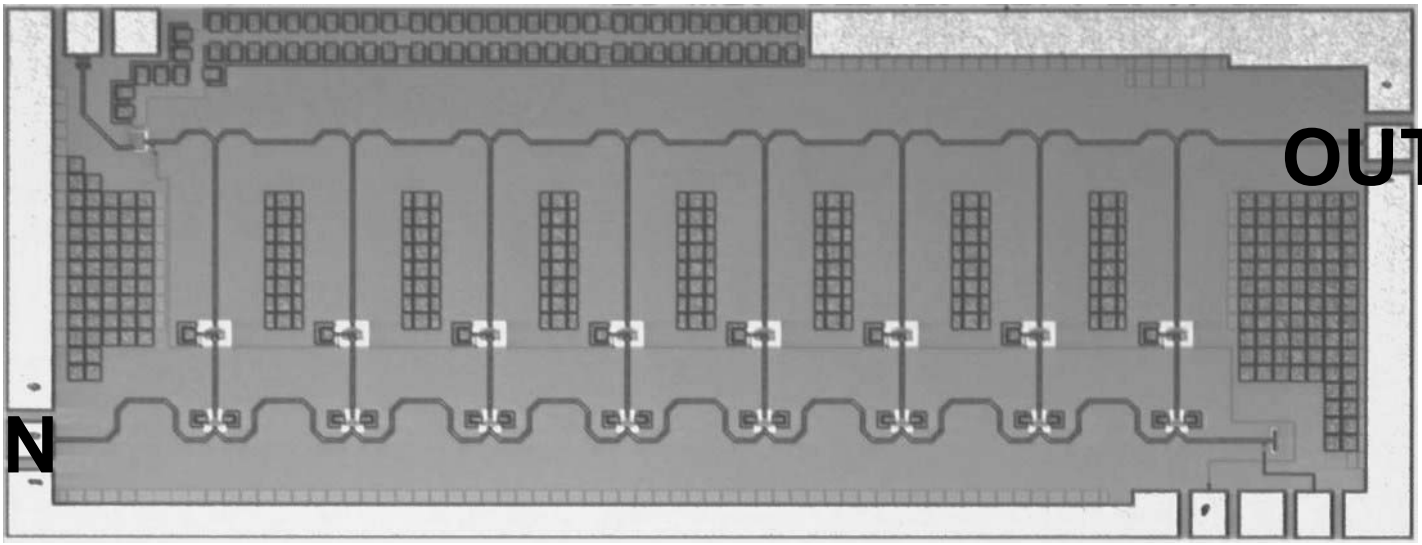

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