Power Gain Singularities in Transferred-Substrate InAlAs–InGaAs-HBTs

Miguel Urteaga and Mark J. W. Rodwell, *Fellow, IEEE*

***Abstract*—Deep submicron transferred-substrate heterojunction bipolar transistors exhibit peaking and singularities in the unilateral power gain (U) at high frequencies. Unbounded U has been observed in some devices over a 20–110 GHz bandwidth. Associated with the effect are a strong decrease in collector-base capacitance with increased bias current, and negative conductance in the common-emitter output conductance G_{22} and positive conductance in the reverse conductance G_{12}. Unbounded U is observed in devices operating at current densities as low as 0.56 mA/μm^2. A potential explanation of the observed characteristics is dynamic electron velocity modulation in the collector-base junction. A theoretical model for the dynamics of capacitance cancellation by electron velocity modulation is developed, and its correlation with experimental data examined.**

***Index Terms*—Capacitance cancellation, heterojunction bipolar transistors (HBT), InGaAs, InP, unilateral power gain, velocity modulation.**

I. Introduction

By scaling heterojunction bipolar transistor (HBT) dimensions to the submicron scale, the magnitudes of the base resistance and the collector-base capacitance can be reduced, thereby increasing the power gain cutoff frequency $f_{\max}$ [1]. In a series of publications [2]–[4], transferred-substrate HBTs have been reported with progressively decreasing lateral dimensions of the collector-base and emitter-base junctions, as a result of which progressively increasing high frequency power gains have been observed.

The observed trend of increasing device gain with scaling is more rapid than simple geometric scaling theory predicts [1]. In [1], a submicron transferred-substrate HBT was reported with measured 20 dB unilateral power gain at 100 GHz. A -20 dB/decade extrapolation of the measured transistor power gain predicts a power gain cutoff frequency $f_{\max}$ of $\sim$1 THz. Utilizing a modified hybrid-pi circuit model that accounts for the distributed nature of the base-collector junction parasitics [1], and given the device geometry, the measured f_τ and the measured base sheet and contact resistivity of the device, the predicted power gain cutoff frequency of the transistor is only 420 GHz.

The predicted power gain of the device was calculated under the assumption that the parasitic collector-base capacitance was equal to a parallel plate capacitance determined from the collector contact dimensions. However, as noted in [1], [3], the observed high-frequency power gain of these devices is in part due to a substantial (and experimentally observed) decrease in the collector-base capacitance with increasing collector bias current. A reduction in collector-base capacitance with increased current due to electron velocity modulation in the collector depletion region was predicted by Moll and Camnitz [5], and further investigated by Betser and Ritter [6]. Given these data, it was noted in [1] that a determination of $f_{\max}$ by a -20 dB/decade extrapolation of the measured unilateral power gain should be treated with considerable caution.

Further investigation of the high frequency power gains of submicron transferred-substrate HBTs has been pursued to frequencies up to 220 GHz. Methods have been developed for precision on-wafer characterization [7] across measured frequency bands, and transferred-substrate HBTs have been fabricated with emitter junction widths as small as 0.3 μm. For these recently fabricated devices, peaking, and in some cases singularities, are observed in the high-frequency unilateral power gain. In some devices, U is unbounded over a full 20–110 GHz bandwidth. Associated with these observations are a rapid decrease in collector-base capacitance with bias current, and negative resistance trends in the device common-emitter output admittance (Y_{22}) and the reverse transmission (Y_{12}).

In this paper, an extended version of the Moll/Camnitz collector velocity modulation theory [5] is developed in which the high-frequency dynamics of collector-base capacitance cancellation are considered. It is shown that modulation of the electron velocity in the collector by an applied collector-base voltage may produce both a frequency-dependent reduction in the effective collector-base capacitance and a negative conductance between collector and base.

In Section II, experimental data is presented showing a singularity in the unilateral power gain of a submicron transferred-substrate HBT. Evidence of bias dependent capacitance cancellation and negative resistance effects in the device are also shown. A series of recent publications have presented a hypothesis describing a resonance behavior in the unilateral power gain due to the dynamics of hole movement in the collector for HBTs operating under the condition of base pushout. [8]–[10]. Given the similarities to the measured data, parameters of highlighted importance from the proposed theory are discussed. Section III presents a model for the dynamics of capacitance cancellation due to electron velocity modulation, and in Section IV, the model is added to a conventional HBT circuit model, and simulations are compared to device measurements.

Manuscript received January 30, 2003; revised April 16, 2003. This work was supported in part by the Office of Naval Research under Contracts N0014-99-1-0041 and N0014-01-0024. The review of this paper was arranged by Editor C.-P. Lee.

The authors are with the Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA 93106 USA (urteaga@ece.ucsb.edu).

Digital Object Identifier 10.1109/TED.2003.813908

II. Experimental Data

A. Measurement Methods

On-wafer device measurements have been performed in 6–45, 75–110, and 140–220 GHz frequency bands, using an HP8510 Vector Network Analyzer with Oleson test set extensions for the higher frequency bands. The measurements were calibrated using a through-reflect-line (TRL) calibration [11], [12], with calibration standards realized on the device substrate.

The transferred-substrate process provides a well-controlled microstrip wiring environment with a thin (5 μm) spin-on-polymer dielectric substrate (Benzocyclobutene, ($\varepsilon_r = 2.7$) [1]. The thin substrate thickness ensures a single-mode transmission line propagation environment across the measurement frequency ranges. Electromagnetic simulations of the microstrip lines have been performed, and corrections have been applied to measurements to account for the complex characteristic impedance of the Line standard due to resistive losses.

The reverse transmission characteristics (S_{12}) of submicron HBTs are difficult to measure due to the extremely small collector-base junction capacitance of the devices (<10 fF). A standard 12-term network analyzer error correction does not account for coupling between on-wafer probes, and the magnitude of this coupling can be on the order of S_{12} for a submicron device. To reduce probe-to-probe coupling, devices were embedded in lengths of on-wafer transmission line with a probe-to-probe separation of $\sim 500\ \mu$m. The TRL calibration was used to place the measurement reference planes at the device terminals.

Quantifying the accuracy of network analyzer calibrations is difficult. The reflection coefficient of the open and short reflect standards are not specified in the TRL calibration, and thus measurement of these provides a partial verification of the calibration. Measurement of these standards showed little amplitude and phase variation in the 6–45 GHz and 75–110 GHz bands. For example, in the 75–110 GHz band, measurements of open-circuit and short-circuit calibration standards showed <0.1 dB amplitude variation and <1.5 degrees phase variation.

In the 140–220 GHz, measurements showed a larger degree of variation. Measurements of an open circuit standard after calibration consistently showed ~0.2 dB of gain and a phase variation of ~5 degrees over the band. Small gain variations can be tolerated in the measurements of tuned-amplifier circuits, and the 140–220 GHz VNA has shown consistent measurements of such circuits [13]. For device measurements and parameter extraction, a higher level of measurement accuracy is required. We are particularly concerned with our measurements of the reverse transmission characteristics (S_{12}) of transistors in the 140–220 GHz band, which as discussed previously, are difficult to measure for submicron devices. For this reason, data from the 140–220 GHz band is not used to draw conclusions about power gain singularities and negative resistance effects observed in the reported submicron HBTs. We are also hesitant to report power gains measured in this band, but do include the data for completeness.

B. Device Measurements

We consider measurements of a transferred-substrate device with emitter junction dimensions $0.3 \times 18\ \mu$m^2, and collector stripe dimensions of $0.7 \times 18.4\ \mu$m^2. The layer structure was grown by solid-source molecular beam epitaxy at UCSB. Important features of the layer structure include: an InAlAs–InGaAs emitter-base heterojunction with chirped super lattice grading to remove the conduction band discontinuity, a 400 Å base layer beryllium doped at 4×10^{19} cm^{-3} with 50 meV compositional band-gap grading, and a 3000 Å InGaAs collector doped at 1×10^{16} cm^{-3} with a 50 Å delta doping of 1×10^{17} cm^{-3} located 250 AA from the base-collector junction. Details of the transferred-substrate process flow are described in [1].

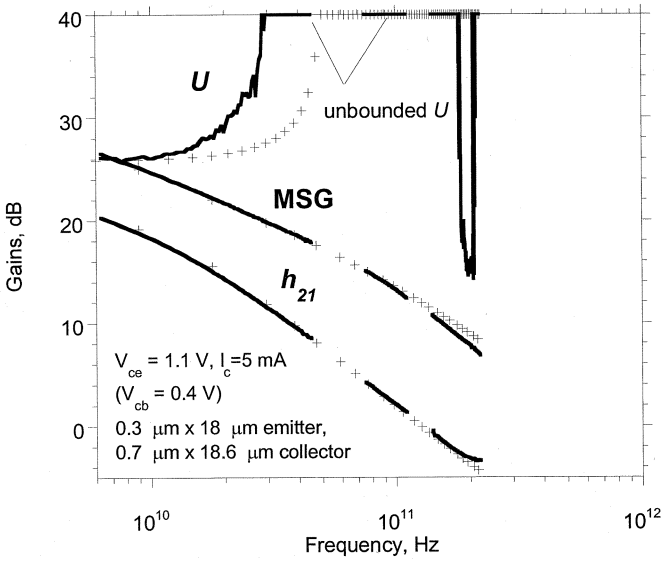


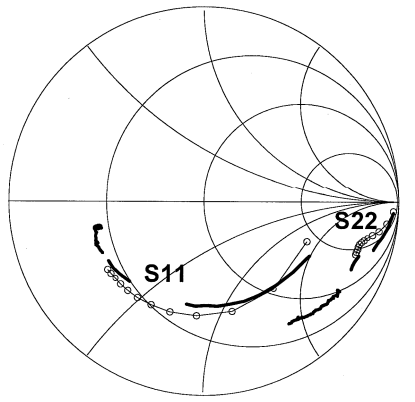
Fig. 1. Measured unilateral power gain (U), maximum stable gain (MSG), and short circuit current gain (h_{21}) of submicron HBT (solid lines). Also included in the plot are simulated gains using transistor model developed in Section IV (crosses). The simulated results assume a low-frequency capacitance cancellation of 3 fF, which corresponds to the measured decrease in C_{cb} at these bias conditions.

Fig. 1 shows the unilateral power gain (U), the short circuit current gain (h_{21}), and the maximum stable gain (the device is potentially unstable over the full measured frequency range) of the device measured at a bias condition of $\mathrm{V_{CE}} = 1.1$ V and $\mathrm{I_C} = 5$ mA. The unilateral power gain is observed to increase and become negative at ~30 GHz, remaining negative across the entire 75–110 GHz band. To better understand the consequences of a negative unilateral power gain, consider the expression for U in terms of a two-port network's Y-parameters [14]

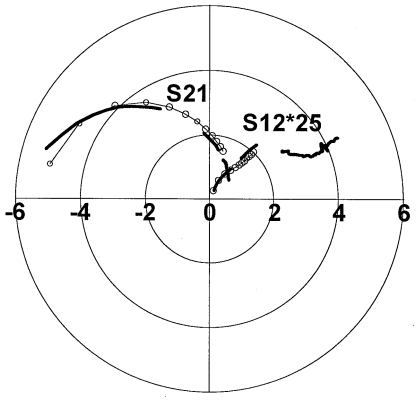
$$U = \frac{|Y_{21} - Y_{12}|^2}{4(G_{11}G_{22} - G_{21}G_{12})} \tag{1}$$

where G_{11}, G_{12}, G_{21}, and G_{22} are the real parts of the network's Y-parameters.

Note that under the condition of negative unilateral power gain, an addition of the appropriate shunt resistive loading will result in unbounded U, and therefore, negative U is equivalent to unbounded (infinite) unilateral power gain. From (1), it is also observed that a negative unilateral power gain may be obtained in the presence of a negative output conductance (G_{22}) or a positive feedback component (G_{12}). An HBT in common-emitter configuration will normally exhibit positive G_{22} and negative G_{12}. Later in this section, bias dependent measurement data of G_{12} and G_{22} will be presented.



(a)



(b)

Fig. 2. Transistor S-parameters measured in 6–45, 75–110, and 140–220 GHz frequency bands (solid lines). Device bias conditions $\mathrm{V_{CE}} = 1.1$ V and $\mathrm{I_C} = 5$ mA. Also included in the plots are simulated S-parameters (6–110 GHz) using the transistor model developed in Section IV (circles).

For completeness, the measured device S-parameters across all three of the measured frequency bands are presented in Fig. 2. Note that while S_{11}, S_{22}, and S_{21} show a relatively smooth variation across the three measurement bands, S_{12} in the 140–220 GHz range appears to deviate significantly from the trajectory of the measurements in the lower frequency bands. The deviation of S_{12} supports the suspicion that the measurement may be corrupted from excessive on wafer probe-to-probe coupling.

For an HBT well described by a hybrid-pi model, the unilateral power gain will show a -20 dB/decade roll-off independent of the reactances of the on-wafer embedding network and the transistor configuration (i.e. common-emitter versus common-base). This behavior motivates the use of U to extrapolate the $f_{\max}$ of a transistor. The presented measurement of the unilateral power gain clearly does not show a well-behaved -20 dB/decade roll-off, and the negative resistance effects observed in measurements of G_{22} and G_{12} are not predicted by a standard hybrid-pi circuit model.

A recent series of publications [8]–[10] has proposed a resonance behavior in the unilateral power gain for InGaAs collector HBTs operating under the condition of base-pushout [15]. The theory proposes a sub-f_τ resonance in the unilateral power gain followed by a much steeper than -20 dB/decade roll-off in the unilateral power gain. Given the similarity of the theory to the presented results and the fact that the publications make specific reference to results from our research group, we feel it is necessary to present data of highlighted importance in [8]–[10].

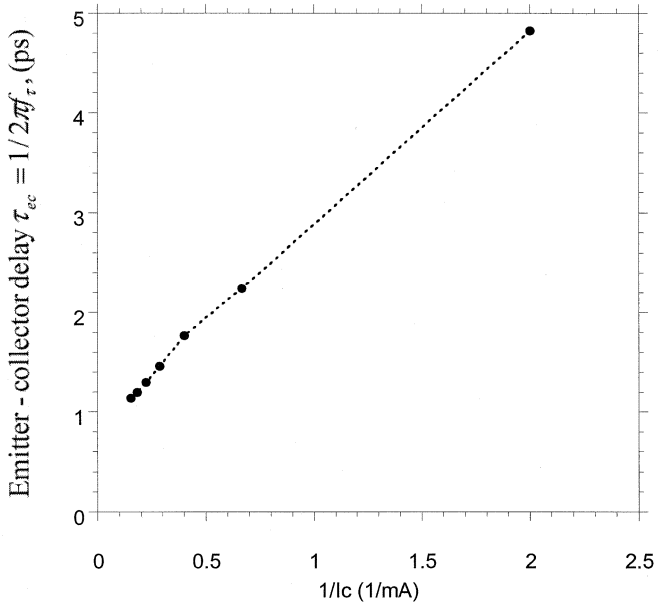


Fig. 3. Transistor forward delay ($\tau_{ec} = 1/2\pi f_\tau$) plotted versus inverse of collector current at constant collector base voltage $\mathrm{V_{CB}} = 0.35$ V.

As the theory in [8]–[10] depends on the device operating in the base pushout regime, we note for the data presented in Fig. 1, the operating current density of the device referenced to the emitter junction area is 0.93 mA/μm^2. The collector current density, which determines the Kirk threshold, will be even smaller due to collector current spreading [16]. Unbounded unilateral power gain over the 75–110 GHz band was observed for currents as low as 3 mA corresponding to an emitter current density of 0.56 mA/μm^2.

Fig. 3 shows the transistor forward delay time, $\tau_{ec} = 1/2\pi f_\tau$, plotted versus the inverse of the collector current at a constant base-collector voltage, $\mathrm{V_{CB}} = 0.35$ V. The data does not show an increase in the delay time at increasing current densities, a phenomenon normally associated with base-pushout in silicon bipolar transistors [15]. In III–V HBTs, analysis of base-pushout operation is more complicated as ballistic electron transport may be enhanced at high current densities [17]. We note that Fig. 3 shows a slight variation from a linear dependence that would be expected if the collector transit time did not vary with collector current. However, the voltage dependence of the base-emitter junction capacitance may also contribute to this observation.

The sub-f_τ resonance theory of [8]–[10] makes definite predictions of measurable transistor quantities and these predictions may be compared to experimental data. Among these predictions are: an increase in the slope of the roll-off in the maximum available and maximum stable gain at frequencies above the resonance [8], an experimentally measured increase in the roll-off of the short-circuit current gain for a device said to be operating in base pushout [10], a peaking in the magnitude of the common-base current gain $\alpha(\omega)$ followed by a steep decrease [9], [10], and a strong peaking in the effective collector-base ca-

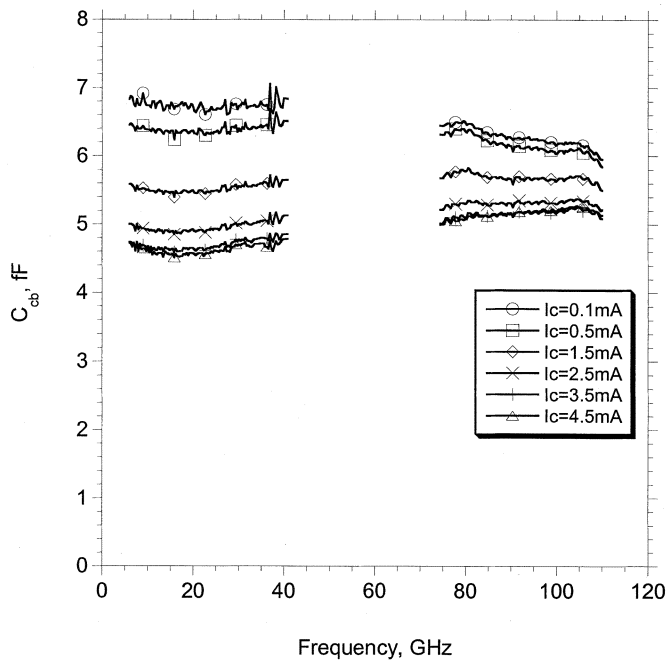


Fig. 4. Effective base-collector capacitance C_{cb} at varying $\mathrm{I_C}$ and $\mathrm{V_{CB}} = 0.35$ V.

pacitance with increasing frequency [9]. None of these experimentally observable trends were seen in the measured transistor characteristics. Given the aforementioned observations, it is our assertion that under the device bias conditions presented in this paper, the HBT is not operating in the base pushout regime.

For an intrinsic HBT described by a Tee-model with zero collector series resistance and zero extrinsic collector-base capacitance, the collector-base admittance Y_{CB} is described in terms of the network Z-parameters as

$$Y_{CB} = \frac{1}{Z_{22} - Z_{21}}. \tag{2}$$

The transferred-substrate technology has a zero series resistance Schottky collector contact, and an extremely low extrinsic collector-base capacitance, justifying the assumptions of (2). However, the technology suffers from relatively large input and output parasitic capacitances to ground (1–15 fF), arising from interconnect metal overlap with the thermal via underneath each device [1].

The input and output layout capacitances were extracted from S-parameter measurements using a technique similar to [18]. The output capacitance was de-embedded from the measured S-parameters of the device. Through circuit simulations, it was found that the addition of a parasitic input capacitance to a transistor model does not have a significant impact on the imaginary part Y_{CB} extracted using (2), and for the data presented here, this capacitance was not de-embedded from measurements.

An effective collector-base capacitance can be defined as $C_{cb} = \mathrm{Im}(Y_{CB})/\omega$. Fig. 4 shows bias dependent measurements of C_{cb} plotted versus frequency in the 6–45 GHz and 75–110 GHz bands. The data is plotted for various values of collector current $\mathrm{I_C}$ and a constant collector-base voltage $\mathrm{V_{CB}} = 0.35$ V. The effective collector-base capacitance is found to have a large dependence on the device bias conditions. A reduction in the low-frequency collector-base capacitance of $\sim$2 fF is observed over the range of applied $\mathrm{I_C}$.

Associated with the observed singularity in the unilateral power gain are negative resistance trends in the HBT reverse conductance G_{12} and in the output conductance G_{22}. Trends not predicted by standard HBT circuit models. To illustrate this, consider Y_{12} of an HBT described by a hybrid-pi equivalent circuit model. To simplify the analysis, we consider the device to have zero series emitter resistance, an assumption that reduces the terms in the expression for Y_{12} but does not change the overall behavior of the parameter. Y_{12} expanded to second order in frequency is then given by

$$Y_{12} = -\left(\frac{1}{R_{cb}} + \omega^2 C_{cb,i} C_{be} R_{bb}\right) - \mathrm{j}\omega(C_{cb,i} + C_{cb,x}) \tag{3}$$

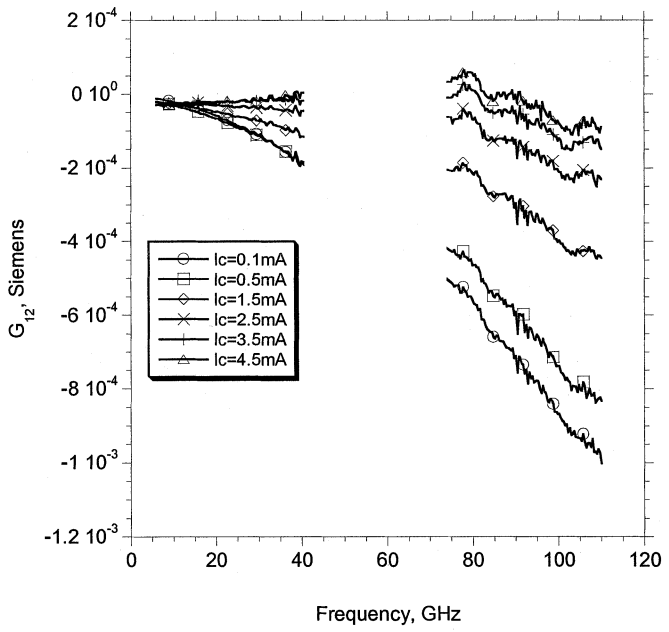
where C_{be} is the base-emitter capacitance (junction and diffusion), R_{bb} is the base resistance, $C_{cb,\mathrm{i}}$ is the portion of collector-base capacitance internal to R_{bb} in the circuit model, $C_{cb,x}$ is the remaining collector-base capacitance external to R_{bb}, and R_{cb} is a finite collector-base resistance that arises in InGaAs collector HBTs from impact ionization in the collector region.

For an HBT described by a hybrid-pi circuit model the real part of $Y_{12}(G_{12})$, will show a parabolic variation with frequency, and will always be negative. Fig. 5 shows G_{12} for the transistor of Fig. 1 plotted versus frequency at varying collector currents and a constant collector-base voltage $\mathrm{V_{CB}} = 0.35$ V. The data shows that at low bias currents G_{12} demonstrates the frequency dependence of (3). However, as the current increases, the slope of G_{12} changes, and eventually, positive G_{12} is observed over portions of the frequency band. Similarly, G_{22}, also plotted in Fig. 5, shows a trend toward negative output conductance with increasing bias current.

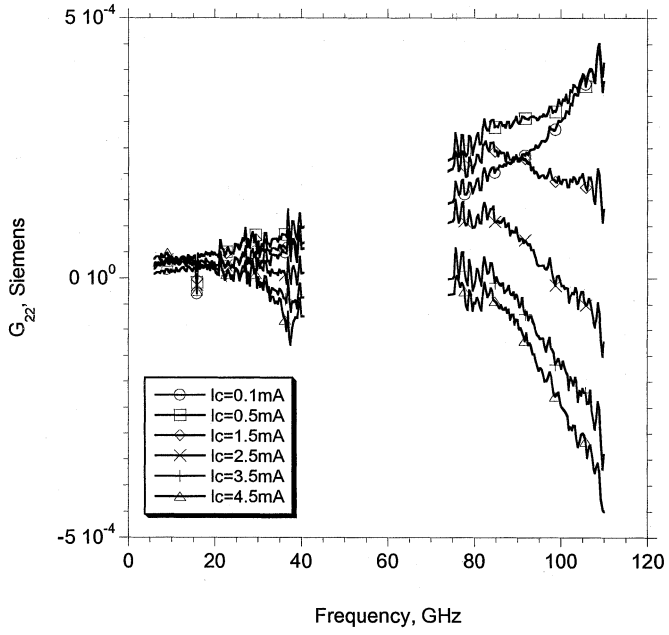
III. Capacitance Cancellation Through Electron Velocity Modulation

Fig. 4, as described in the previous section, shows evidence of a decrease in the effective collector-base capacitance of the transistor with increasing collector current. In this section, we develop a dynamic model for capacitance cancellation through electron velocity modulation in the collector space charge region. In analyzing the effect beyond first order in frequency, negative conductance terms are observed.

In advanced III–V HBTs, electrons entering the collector space charge region experience ballistic transport, and may travel a significant fraction of the collector at a higher velocity than the saturation velocity of the bulk semiconductor [17]. The electric field profile in the collector influences the velocity profile, as the kinetic energy of the electrons determines the scattering probability to lower velocity satellite conduction bands. At higher applied collector-base voltages, InGaAs-collector HBTs will typically exhibit larger collector transit times due to a lower effective velocity. Modulation of the collector velocity changes the collector space charge profile due to the redistribution of the density profile of mobile electrons. Capacitance cancellation arises because modulation of mobile charge in the collector screens the base and collector terminals from changes in the electric field.



(a)



(b)

Fig. 5. G_{12} (a) and G_{22} (b) plotted versus frequency at varying $\mathrm{I_C}$ and $\mathrm{V_{CB}} = 0.35$ V.

A static derivation of capacitance cancellation through this phenomenon was proposed by Moll and Camnitz [5], and more fully developed by Betser and Ritter [6]. In the static derivation the intrinsic collector-base capacitance of the HBT is given by

$$C_{cb} = \frac{\varepsilon A_E}{W_C} - I_C \frac{\partial \tau_C}{\partial V_{CB}}\bigg|_{W_C} \tag{4}$$

where A_E is the emitter area, ε is the dielectric constant, and W_C is the thickness of the collector depletion region. The term $\varepsilon A_E/W_C$ is the standard dielectric capacitance, and the term $-I_C \partial \tau_C/\partial V_{CB}|_{W_C}$ represents the capacitance cancellation. In this expression we have ignored a term related to the collector-base output conductance, which is shown by Betser and Ritter to be insignificant for practical HBTs [6].

The static derivation of capacitance cancellation is limited by the charge control assumption that changes in the collector space charge occur instantaneously. Clearly, this assumption must fail at frequencies approaching the inverse of the collector transit time. It will be shown in the derivation that follows that the degree of capacitance cancellation decreases with increasing frequency, and more importantly, that negative resistance effects due to electron velocity modulation may be significant at relatively low frequencies.

We consider the dynamics of capacitance cancellation under the assumption of a collector electron velocity which is a function of $\mathrm{V_{CB}}$, but explicitly ignore the variation of velocity as a function of position within the collector. Having in the preceding discussions considered the importance of ballistic transport effects in the collector, we recognize that the resulting analysis is therefore only approximate. However, our goal is to present a theory as to the origin of negative resistance effects in InGaAs-collector HBTs through velocity modulation, and not to develop an exact model.

The dynamics of capacitance cancellation will be analyzed in the time domain. We consider an HBT operating with a dc collector-base voltage $\mathrm{V_{CB,0}}$ and a dc collector current $\mathrm{I_{C,0}}$. For the given bias conditions, electrons in the space-charge region travel with a velocity v_o, and we further define an inverse velocity $s_o = 1/v_o$.

The collector region has a thickness W_C and is uniformly doped at a concentration of N_D. We assume that the collector region is fully depleted at the applied DC bias conditions, such that W_C is not modulated by small changes in the applied collector base voltage. To further simplify the analysis, we assume that the base and subcollector regions are heavily doped and undepleted. Under these assumptions, the entire collector-base voltage is dropped across the collector space charge region. The total charge density in the region is given by $n(x) = qN_D - J_E s_o$, where $J_E = I_{C,0}/A_E$ is the current density entering the collector region from the base.

We consider the time evolution of the current at the collector terminal in response to a small step in the collector base voltage ΔV_{CB} applied at $t = 0$. At $t = 0^+$, there will be an instantaneous change of the sheet charge at the base and collector terminals determined by the dielectric capacitance of the depleted collector region. The change in electron velocity caused by the applied ΔV_{CB} is assumed to occur instantaneously and uniformly across the collector space charge region. The inverse velocity after application of the voltage step is given by $s(x) = s_0 + \Delta s$, where $\Delta s = \Delta V_{CB}(\partial s/\partial V_{CB})$. As discussed previously, Δs would normally be positive for an InGaAs-collector HBT, however, the derivation that follows is valid for arbitrary Δs.

The mobile electron charge in the collector region can be viewed as a collection of traveling sheets of charge. The displacement current generated at the collector terminal from a sheet of charge with density ρ_s traveling at velocity v through the depleted collector is given by $J_d = -\rho_s v/W_C$, where we have defined J_d to be a positive current if flowing into the collector terminal.

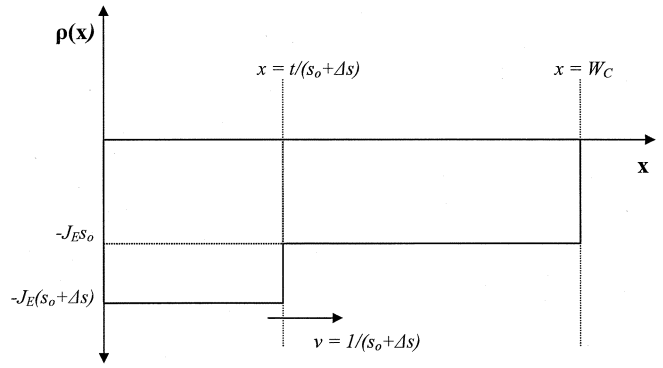


Fig. 6. Electron space charge density in collector region at time t after application of collector-base voltage step.

At $t = 0^+$, the electron charge in the collector is uniformly distributed, and we divide the region into sheets of charge of thickness Δx and charge density $\rho_s = -J_E s_o \Delta x$. The total collector current at $t = 0^+$ can be determined by summing the displacement current contributions from all of the sheets of charge in the collector region while taking $\Delta x \to 0$. The change in collector current is then given by

$$\Delta J_C|_{t=0^+} = \int_0^{W_C} \frac{J_E s_o}{W_C(s_o + \Delta s)} dx - J_E = \frac{J_E s_o}{(s_o + \Delta s)} - J_E \approx \frac{-J_E \Delta s}{s_o}. \quad (5)$$

Note that although the charge density is determined by the initial unperturbed electron velocity, the perturbed velocity is used to describe the moving charge sheet. Equation (5) shows that immediately after the application of the collector-base voltage step the collector current has been reduced from its initial value J_E, indicating a trend toward negative conductance. It is important to note that J_E, the electron current entering the collector region, will not vary with the applied ΔV_{CB}. The base region in III–V HBTs is highly doped and modulation of the collector-base voltage will not cause a significant change in the base width, and hence, the electron current entering the collector will stay constant. This conclusion is supported by lack of Early effects in standard III–V HBTs.

To evaluate the time evolution of the collector current, we must consider the redistribution of electron charge in the collector region. We assume that the redistribution of the electron space charge takes place as a moving charge front as illustrated in Fig. 6. The charge front enters at the collector-base junction and travels through the collector at the perturbed electron velocity, such that the charge distribution at time t is given by

$$n(x) = \begin{cases} qN_D - J_E(s_o + \Delta s), & \text{for } 0 \le x < \frac{t}{(s_o+\Delta s)} \\ qN_D - J_E s_o, & \text{for } \frac{t}{(s_o+\Delta s)} \le x \le W_C. \end{cases} \quad (6)$$

At $t = W_C(s_0 + \Delta s)$, the collector charge density has reached its uniform steady-state distribution determined by the perturbed electron velocity.

Modeling the electron charge redistribution as a uniform moving charge front assumes that the density of electrons does not in itself perturb the electron velocity. This assumption may not hold at high current densities, where the density of electrons is comparable to the collector donor charge. Extending calculations to include the effects of current modulation on the electron velocity may be necessary to more accurately model the collector-base admittance at high current densities.

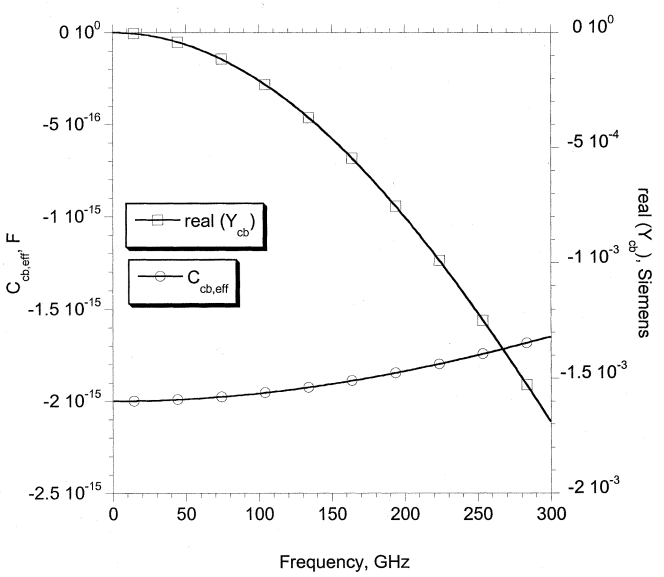


Fig. 7. Effective collector-base capacitance ($C_{cb,\text{eff}}$) and real part of Y_{cb} from (8).

Using the same formalism used to derive (5), we can calculate as a function of time the change in current at the collector terminal with the charge density described by (6).

$$\Delta J_C(t) = \begin{cases} \frac{-J_E \Delta s}{s_o} + \frac{J_E \Delta s}{W_C s_o^2} t, & \text{for } 0 < t \le W_C(s_o + \Delta s) \\ 0, & \text{for } W_C(s_o + \Delta s) < t. \end{cases} \quad (7)$$

Equation (7) shows that the collector current initially decreases and then linearly increases back to its dc value J_E, which it reaches at time $t = W_C(s_0 + \Delta s)$ when the electron charge front has filled the collector region.

The time dependence of the collector current has been calculated for a step change in the applied collector-base voltage. Using Fourier techniques, the step response can be used to calculate the frequency response of the collector current to an applied collector-base voltage, and an effective collector-base admittance $Y_{cb} = \partial I_c / \partial V_{CB}|_{I_E}$ can be determined.

The calculation of Y_{cb} is described in the Appendix. It is shown that the effective collector-base admittance is given by

$$Y_{cb} = \left.\frac{\partial I_c}{\partial V_{CB}}\right|_{I_E} = -\frac{I_{C,0}}{\tau_c}\frac{\partial \tau_c}{\partial V_{CB}}\left(1 - e^{-j\omega\tau_c}\frac{\sin \omega\tau_c}{\omega\tau_c}\right) = -\frac{C_{cb,\text{canc}}}{\tau_c}\left(1 - e^{-j\omega\tau_c}\frac{\sin \omega\tau_c}{\omega\tau_c}\right) \quad (8)$$

where τ_c is the collector transit time, and $C_{cb,\text{canc}} = I_{C,0}\partial\tau_c/\partial V_{CB}$ is the low frequency capacitance cancellation. Expanding (8) to second order in frequency gives

$$Y_{cb} = \frac{-j\omega C_{cb,\text{canc}}}{1 + j\omega\frac{2\tau_c}{3}} + \mathrm{O}(\omega^3) + \ldots. \quad (9)$$

Equation (9) shows that at low frequencies the base-collector admittance due to velocity modulation can be described by a series network with a negative capacitance of magnitude

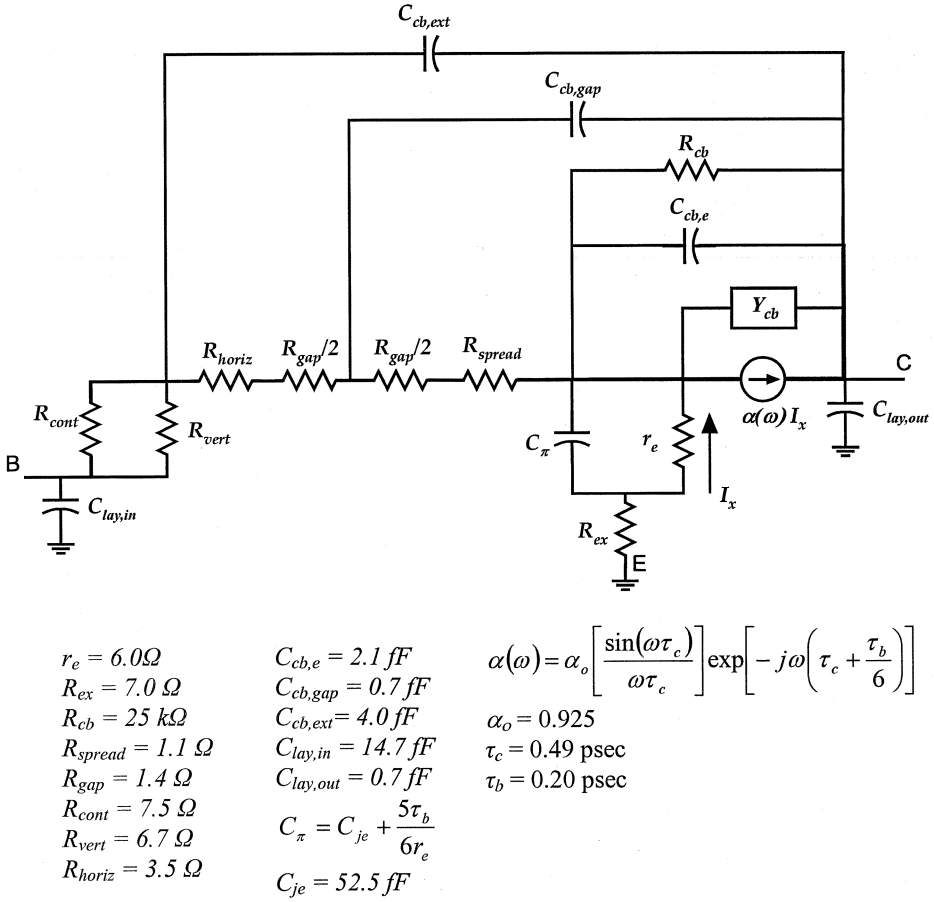


Fig. 8. Equivalent circuit model and parameter values used to simulate HBT. Admittance block Y_{cb} implements capacitance cancellation model of (8).

$C_{cb,\mathrm{canc}}$ in series with a negative resistance of magnitude $2\tau_c/(3C_{cb,\mathrm{canc}})$. This network appears in parallel with the dielectric capacitance of the intrinsic collector-base junction. Equation (9) is useful for modeling the effects of velocity modulation at low frequencies, and provides physical insight in describing these effects. However, for the simulations presented in the remainder of this paper, the full frequency dependent expression for Y_{cb} (8) is used.

Fig. 7 shows the equivalent collector-base capacitance ($C_{cb,\mathrm{eff}} = \mathrm{Im}(Y_{cb})/\omega$) and real part of Y_{cb} calculated from (8). The data is plotted to 300 GHz and assumes a low frequency capacitance cancellation of 2 fF and a collector transit time of 0.5 psec. It is seen that with increasing frequency the effective negative collector-base capacitance decreases, while the real part Y_{cb} becomes more negative.

IV. Equivalent Circuit Model

In this section, the collector-base admittance model developed in the previous section will be added to a small-signal HBT model, and observations of negative resistance effects in device simulations will be presented. Prior to developing the circuit model, we consider whether electron velocity modulation can explain the degree of capacitance cancellation observed experimentally in transferred-substrate HBTs.

The static capacitance cancellation model of (4) relates the low- frequency reduction in the effective collector-base capacitance to the derivative of the collector transit time with respect to the collector-base voltage. This derivative is taken under the condition of a constant collector depletion region thickness (W_C), and as pointed out in [6] this parameter is not generally available from measured transistor data. However, in the transferred-substrate technology the lightly doped collector region is followed by a Schottky collector contact, and if fully depleted, we expect to observe little variation in the collector depletion thickness. If the depleted collector thickness does not vary with applied $\mathrm{V_{CB}}$, then an approximate measure of the term $I_C \partial\tau_c/\partial V_{CB}|_{W_C}$ can be determined from the change in the transistor f_τ in response to a small change in the collector-base voltage.

For the transistor described in Section II, the HBT f_τ was measured at a constant collector current and the collector-base voltage was varied between 0.35 V and 0.45 V. At a collector current of 4.5 mA, an $f_\tau = 123$ GHz and $f_\tau = 117$ GHz were measured at $\mathrm{V_{CB}} = 0.35$ V and $\mathrm{V_{CB}} = 0.45$ V, respectively. If the decrease in f_τ is solely attributed to an increase in the collector transit time, then the low frequency capacitance cancellation is approximated by $C_{cb,\mathrm{canc}} = I_C \Delta\tau_c/\Delta V_{CB} = 3.0$ fF. This value indicates that electron velocity modulation can account for the large relative decrease in the measured low frequency C_{cb}. Unfortunately, due to their poor breakdown and thermal characteristics, the validity of (4) can only be tested over a limited bias range for InGaAs-collector transferred-substrate HBTs. A more detailed experimental consideration of (4) was performed in [6].

The transistor is modeled using a modified Tee-topology shown in Fig. 8. The intrinsic elements of the model are

common to a standard bipolar Tee-model [19]. Additional elements are included to account for the distributed nature of the collector-base junction parasitics [1], [7], and we will describe those terms in detail.

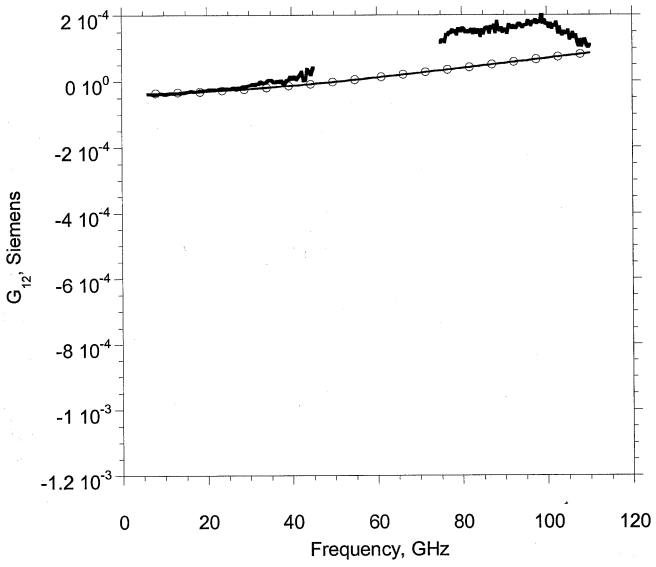
The terms $C_{cb,e}$ and $C_{cb,gap}$ represent the portion of the collector-base capacitance directly under the emitter and the gap between the emitter and base contact, respectively. The values of these parameters are calculated using the estimated transistor geometry. The additional capacitance $C_{cb,ext}$ accounts for the remaining collector-base capacitance that is extracted from measurements at zero collector current and the applied base collector voltage such that $C_{cb,ext} = C_{cb0,meas} - C_{cb,e} - C_{cb,gap}$.

The resistances R_{spread}, R_{cont} and R_{gap} represent the spreading resistance under the emitter, the base contact resistance, and the gap resistance between the emitter and base contact, respectively. The additional resistance R_{vert} accounts for the vertical access resistance over the portion of the base contact that overlaps the collector contact, and R_{horiz} represents the lateral sheet resistance over the same path. The physical values of the resistances were determined from the estimated transistor geometry, and sheet and contact resistances that were measured on the transistor epitaxy by the TLM method.

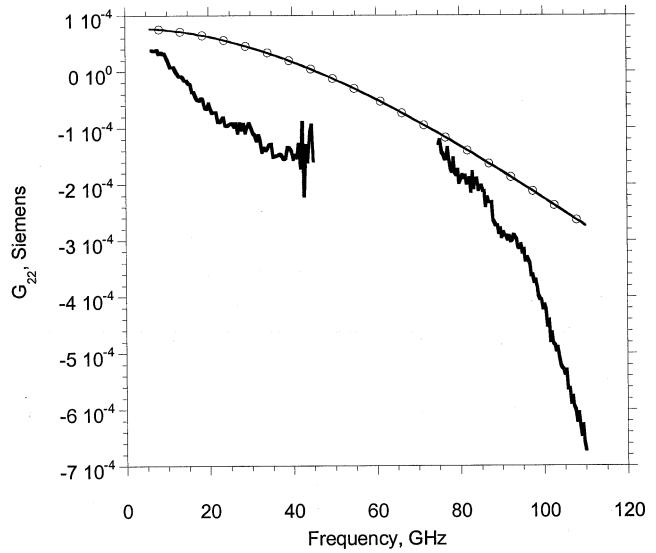
The collector-base admittance due to electron velocity modulation (8) is included in the model as the admittance Y_{cb} appearing in parallel with $C_{cb,e}$. For simulations, a low frequency collector-base capacitance cancellation $(I_C \partial \tau_c / \partial V_{CB})$ of 3 fF has been assumed. This value corresponds to the measured decrease in C_{cb} for the device at the bias conditions of Fig. 1. The remaining terms in the small-signal model were determined using a bias dependent extraction technique similar to that presented in [20]. A complete description of all of the parameter values is included in Fig. 8.

Included in Fig. 1 are the simulated unilateral power gain, maximum stable gain and short circuit current gain of the transistor model of Fig. 8 plotted to 220 GHz. In Fig. 2 the simulated S-parameters from 6–110 GHz are included with the measured S-parameter of the device. Besides the extraction methods described above, no further optimization of the model parameters was performed. Still, relatively good agreement is seen between measured and modeled transistor S-parameters. Additionally, a singularity is observed in the simulated unilateral power gain occurring at a frequency of $\sim$50 GHz, and U remains unbounded over the remaining simulated frequency range. Because of the high frequency limitations of the Tee-model and the approximations used to derive the collector-base admittance model, we will not use our model to make any predictions of the transistor's $f_{\max}$. We do note that the transistor power gain benefits from the negative resistance effects observed in the collector-base admittance, as the simulated maximum stable gain of the device is observed to increase with the addition of the dynamic capacitance cancellation model versus a purely static capacitance cancellation model.

Negative resistance trends observed in the measurements are also seen in the simulated results. Fig. 9 shows the measured and simulated G_{12} and G_{22} of the transistor. Larger negative resistance effects appear to be seen in the measured transistor parameters. The transformation from S-parameters to Y-parameters is not linear, and larger variations in the Y-parameters may be observed for smaller relative variations in the S-parameters. This is particularly true when the S-parameters lie near the edges of the Smith chart, as is the case with transferred-substrate HBTs.



(a)



(b)

Fig. 9. Real part of transistor Y-parameters (a) G_{12} and (b) G_{22}. Measured data (solid lines) and simulated data (circles) at same bias conditions as Fig. 1.

V. Conclusion

Power gain singularities have been observed in the measurements of submicron InGaAs-collector HBTs. Associated with these singularities are trends toward negative conductance in the common-emitter output conductance, and positive conductance in the common-emitter reverse transmission characteristics. These trends cannot be predicted by standard HBT circuit models.

The HBTs also exhibit a decrease in the effective collector-base capacitance with increasing current density. A dynamic

model for collector-base capacitance cancellation due to electron velocity modulation in the collector has been developed. This model was incorporated with a small-signal equivalent HBT circuit model and singularities in the simulated unilateral power gain were observed.

A consequence of the observation of singularities in the unilateral power gain is that the transistor $f_{\max}$ cannot be extrapolated from measurements of U. However, a sharp increase in the roll-off of the transistor's maximum stable/maximum available gain was not observed at higher frequencies, and transferred-substrate HBTs exhibit high levels of power gain to the frequency limits of commercially available network analyzers. Indeed, single-transistor amplifiers using transferred-substrate HBTs have exhibited 6.3 dB gain at 175 GHz [13]. Ultimately, it is through direct measurement and the use of devices in circuit applications that the maximum usable frequency of highly scaled transistors will be determined.

APPENDIX

The step response of the change in collector current to an applied collector-base voltage in the presence of velocity modulation is given in (7). The frequency dependence of the collector-base admittance will be determined from the impulse response of the collector-base current. Given the same DC bias conditions and collector velocity assumptions described in Section III, we consider a voltage impulse applied at time $t = 0$ described by $\Delta V_{CB}(t) = (v_{CB}\Delta t)\delta(t)$, where v_{CB} is the magnitude of the applied impulse and Δt is the duration of the impulse.

The impulse response of the change in collector current can be determined from the derivative of the step response given by (7). The impulse response of the collector current is given by

$$\Delta J_C(t) = \frac{-J_E v_{CB}\Delta t}{s_0}\frac{\partial s}{\partial V_{CB}}\delta(t) + \frac{J_E v_{CB}\Delta t}{s_0^2 W_C}\frac{\partial s}{\partial V_{CB}} rect\left(\frac{t}{W s_o} - \frac{1}{2}\right). \quad \text{(A1)}$$

This expression can be rewritten to include the collector transit time. Under the assumption of an electron velocity that does not vary with position in the collector, the collector transit time is given by $\tau_c = W_C s/2$ and $\partial\tau_c/\partial V_{CB} = (\partial/\partial V_{CB})(W_C s/2) = (W_C/2)(\partial s/\partial V_{CB})$. Substituting these expressions into (A1) gives

$$\Delta J_C(t) = \frac{-J_E v_{CB}\Delta t}{\tau_c}\frac{\partial \tau_c}{\partial V_{CB}}\delta(t) + \frac{J_E v_{CB}\Delta t}{2\tau_c^2}\frac{\partial \tau_c}{\partial V_{CB}} rect\left(\frac{t}{2\tau_c} - \frac{1}{2}\right). \quad \text{(A2)}$$

The small-signal collector base admittance is found by taking the Fourier transform of the impulse response

$$Y_{CB}(\omega) = \frac{\Delta I_C(\omega)}{\Delta V_{CB}(\omega)} = \frac{\Im\left[A_E \Delta J_c(t)\right]}{\Im\left[\Delta V_{CB}(t)\right]} = \frac{-I_{C,0}}{\tau_c}\frac{\partial \tau_c}{\partial V_{CB}}\left(1 - e^{-j\omega\tau_c}\frac{\sin\omega\tau_c}{\omega\tau_c}\right). \quad \text{(A3)}$$

We note that this derivation has been performed under the condition of a constant current J_E entering the collector depletion regions, as is necessary for deriving the small signal base-collector admittance.

REFERENCES

[1] M. J. W. Rodwell, M. Urteaga, T. Mathew, D. Scott, D. Mensa, Q. Lee, J. Guthrie, Y. Betser, S. C. Martin, R. P. Smith, S. Jaganathan, S. Krishnan, S. Long, R. Pullela, B. Agarwal, U. Bhattacharya, L. Samoska, and M. Dahlstrom, "Submicron scaling of heterojunction bipolar transistors," *IEEE Trans. Electron Devices*, vol. 48, pp. 2606–2624, Nov. 2001.

[2] Q. Lee, B. Agarwal, R. Pullela, D. Mensa, J. Guthrie, L. Samoska, and M. Rodwell, "A >400 GHz $f_{\max}$ transferred substrate heterojunction bipolar transistor IC technology," *IEEE Electron Device Lett.*, vol. 19, pp. 77–79, Mar. 1998.

[3] Q. Lee, S. C. Martin, D. Mensa, R. P. Smith, J. Guthrie, and M. J. W. Rodwell, "Submicron transferred-substrate heterojunction bipolar transistors," *IEEE Electron Device Lett.*, vol. 20, pp. 396–398, Aug. 1999.

[4] Q. Lee, S. C. Martin, D. Mensa, R. P. Smith, J. Guthrie, S. Jaganathan, Y. Betser, T. Mathew, S. Krishnan, L. Samoska, and M. J. W. Rodwell, "Submicron-transferred-substrate heterojunction bipolar transistors with greater than 1 THz $f_{\max}$," in *Proc. 57th Device Res. Conf.*. Santa Barbara, CA, June 28–30, 1999.

[5] L. H. Camnitz and N. Moll, "An analysis of the cutoff-frequency behavior of microwave heterojunction bipolar transistors," in *Compound Semiconductor Transistors*, S. Tiwari, Ed. New York: IEEE, 1992, pp. 21–45.

[6] Y. Betser and D. Ritter, "Reduction of the base collector capacitance in InP/GaInAs heterojunction bipolar transistors due to electron velocity modulation," *IEEE Trans. Electron Devices*, vol. 46, pp. 628–633, Apr. 1999.

[7] M. Urteaga, S. Krishnan, D. Scott, Y. Wei, M. Dahlstrom, S. Lee, and M. J. W. Rodwell, "Submicron InP-based HBT's for ultra-high frequency amplifiers," *Int. J. High-Speed Electron. Syst.*.

[8] B. Willen, M. Rohner, and H. Jäckel, "Unilateral power gain limitations due to dynamic base widening effects," *IEEE Electron Device Lett.*, vol. 22, pp. 370–372, Aug. 2001.

[9] M. Rohner, B. Willen, and H. Jäckel, "Sub-f_t gain resonance in InP/InGaAs-HBTs," *IEEE Trans. Electron Devices*, vol. 49, pp. 213–220, Feb. 2002.

[10] B. Willen, M. Rohner, V. Schwarz, and H. Jäckel, "Experimental evaluation of InP-InGaAs power-gain resonance," *IEEE Electron Device Lett.*, vol. 23, pp. 579–581, Oct. 2002.

[11] G. F. Engen and C. A. Hoer, "Thru-reflect-line: an improved technique for calibrating the dual six-port automatic network analyzer," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-27, pp. 987–993, Dec. 1979.

[12] Network Analysis: Applying the HP 8510B TRL Calibration for Non-Coaxial Measurements, Hewlett Packard Product Note 8510-8.

[13] M. Urteaga, D. Scott, T. Mathew, S. Krishnan, Y. Wei, and M. Rodwell, "Single-stage G band HBT amplifier with 6.3 dB gain at 175 GHz," in *GaAs IC Symp. Dig.*, Baltimore, MD, Oct. 21–24, 2001, pp. 83–87.

[14] S. J. Mason, "Power gain feedback amplifier," *IRE Trans. Circuit Theory*, vol. CT-1, pp. 20–25, 1954.

[15] C. T. Kirk, "A theory of transistor cutoff frequency (f_{tau}) fall-off at high current density," *IEEE Trans. Electron Devices*, vol. ED-9, p. 164, 1962.

[16] P. J. Zampardi and D.-S. Pan, "Delay of Kirk effect doe to collector current spreading in heterojunction bipolar transistors," *IEEE Electron Device Lett.*, vol. 17, pp. 470–472, Oct. 1996.

[17] T. Ishibashi, "Nonequilibrium electron transport in HBTs," *IEEE Trans. Electron Devices*, vol. 48, pp. 2595–2605, Nov. 2001.

[18] D. Costa, W. U. Liu, and J. S. Harris, "Direct extraction of AlGaAs/GaAs heterojunction bipolar transistor small-signal equivalent circuit," *IEEE Trans. Electron Devices*, vol. 38, pp. 2018–2024, Sept. 1991.

[19] A. P. Laser and D. L. Pulfrey, "Reconciliation of methods for estimating f_{max} for microwave heterojunction transistors," *IEEE Trans. Electron Devices*, vol. 38, pp. 1685–1692, Aug. 1991.

[20] S. J. Spiegel, D. Ritter, R. A. Hamm, A. Feygenson, and P. R. Smith, "Extraction of InP/InGaAs heterojunction, bipolar transistor small-signal equivalent circuit," *IEEE Trans. Electron Devices*, vol. 42, pp. 1059–1064, June 1995.

Miguel Urteaga received the B.A.Sc. degree in engineering physics from Simon Fraser University, Vancouver, BC, Canada, in 1998 and the M.S. degree in electrical and computer engineering from University of California, Santa Barbara, in 2001. He is currently pursuing the Ph.D. degree at UCSB, where his research work includes device design and fabrication of high-speed JnP HBTs, as well as the design of ultrahigh frequency integrated circuits.

Mark J. W. Rodwell (F'03) received the B.S. degree from the University of Tennessee, Knoxville, in 1980 and the M.S. and Ph.D. degrees from Stanford University, Stanford, CA, in 1982 and 1988, respectively.

He is a Professor and the Director of the Compound Semiconductor Research Laboratories and the NSF Nanofabrication Users Network (NNTJN) at the University of California, Santa Barbara. He was with AT&T Bell Laboratories, Whippany, NJ, from 1982 to 1984. His research focuses on very high bandwidth bipolar transistors and multigigahertz bipolar circuit design for mixed-signal applications and fiber-optic transmission. Recent research activities also include bipolar and field-effect transistors in the 6.1-Å material system, microwave power amplifier design, and monolithic transistor circuits operating above 100 GHz.

Dr. Rodwell was the recipient of a 1989 National Science Foundation Presidential Young Investigator award. His work on GaAs Schottky-diode ICs for subpicosecond/mm-wave instrumentation was awarded the 1997 IEEE Microwave Prize.