University of California
Santa Barbara

ICs, Modules, and Links for 200–300 GHz Wireless Communications

A dissertation submitted in partial satisfaction
of the requirements for the degree

Doctor of Philosophy
in
Electrical and Computer Engineering

by

Utku Soylu

Committee in charge:

Professor Mark Rodwell, Chair
Professor James Buckwalter
Professor Upamanyu Madhow
Professor Loai Salem

June 2023

The Dissertation of Utku Soylu is approved.

Professor James Buckwalter

Professor Upamanyu Madhow

Professor Loai Salem

Professor Mark Rodwell, Committee Chair

May 2023

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by

Utku Soylu

To my parents, Yasemin and İrfan, and my brother, Ufuk, for their unlimited love and support.

Acknowledgements

First and foremost, I would like to express my sincere gratitude to my advisor, Prof. Mark Rodwell, for granting me this valuable opportunity. I consider it a privilege to be under his guidance as his student, and I feel extremely fortunate to have had the opportunity to work with him throughout my Ph.D. studies. He has been a great teacher and mentor throughout my graduate studies at UCSB.

I would like to express my gratitude to the members of my Ph.D. committee: Prof. James Buckwalter, Prof. Upamanyu Madhow, and Prof. Loai Salem. Their valuable feedback on areas that required improvement and their unwavering support have been truly appreciated. I am immensely grateful for the productive and instructive weekly meetings we had with Prof. Buckwalter's and Prof. Madhow's teams. The collaboration we fostered was highly beneficial to my research.

I would like to express my deepest gratitude to both the past and current members of the Rodwell group, as their tremendous help and support have been invaluable to me. I extend my heartfelt thanks to Amirreza Alizadeh, Ahmed Ahmed, Ali Farid, Arda Simsek, Seungchan Lee, Ceylin Bormali, and Logan Whitaker for their contributions to my research. Each of them played a role in my growth, and I gained valuable insights through my interactions with them. In particular, I would like to extend a special thank you to Amirreza Alizadeh, Ahmed Ahmed, and Ali Farid for their guidance throughout my Ph.D. journey. Their assistance and support in areas such as IC design, module design, and measurements have been instrumental to my progress. Additionally, I feel incredibly fortunate to have had the opportunity to work with visiting professor Munkyo Seo during my second year of the Ph.D. His foundational work laid the groundwork upon which I built my transceivers. I would also like to express my appreciation to the former members of the device group: Brian Markman, Yihao Fang, and Hsin-Ying Tseng, for

their valuable interactions and contributions.

Being a part of the ComSenTer and SRC community has been an absolute blessing. It has afforded us a remarkable opportunity to collaborate and engage with esteemed researchers from leading universities worldwide. I am deeply grateful for the invaluable collaboration and interaction we have had with the distinguished ComSenTer professors, industry liaisons, and SRC industry members. Their contributions and unwavering support have played a vital role in the advancement and achievements of our research endeavors. I would like to extend my heartfelt appreciation to the Semiconductor Research Consortium (SRC) ComSenTer program for their generous funding.

I would like to express my gratitude to Teledyne Scientific and Imaging for their invaluable support in IC fabrication. I am especially thankful to Dr. Miguel Urteaga for providing practical insights and considerations in mm-wave IC and packaging design. I am also grateful to UCSB Cleanroom for their assistance in antenna fabrication. Furthermore, I would like to extend my appreciation to Royal Circuits and Bay Area Circuit for their exceptional PCB fabrication and assembly services. The contributions of Kyocera, Advotech, and MicroQ in module assembly are also greatly appreciated. Lastly, I would like to thank RapidDirect for their assistance in mechanical component fabrication. Their support has been instrumental in the successful execution of my project.

Last but not least, I would like to thank my family, my parents, Yasemin and İrfan, and my brother, Ufuk. Without their unconditional love and support, I could not achieve.

Curriculum Vitæ

Utku Soylu

Education

2023	Ph.D. in Electrical and Computer Engineering, University of California, Santa Barbara.
2019	M.S. in Electrical and Computer Engineering, University of California, Santa Barbara.
2018	B.S. in Electrical and Electronics Engineering, Boğaziçi University, İstanbul, Turkey.

Professional Experience

9/2018 - 6/2023	Research Assistant at the High-Frequency Electronics Group at University of California, Santa Barbara, USA.
6/2021 - 9/2022	Summer Internship at IBM T. J. Watson Research Center, Yorktown Heights, NY, USA.
6/2021 - 8/2021	Summer Internship at Nokia Bells, Murray Hill, NJ, USA.

Publications

1. **U. Soylu**, A. Alizadeh, M. Seo, A. S. H. Ahmed, , M. J. W. Rodwell, "A 202 GHz Link Using Planar Transceiver Modules," submitted, *2023 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, Monterey, CA, USA.

2. **U. Soylu**, A. Alizadeh, M. Seo, M. J. W. Rodwell, "280-GHz Frequency Multiplier Chains in 250-nm InP HBT Technology," *IEEE Journal of Solid-State Circuits (JSSC)*, Sept., 2023.

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Abstract

ICs, Modules, and Links for 200–300 GHz Wireless Communications

by

Utku Soylu

There is an increasing demand for high data-rate wireless communications in endpoint and backhaul links. In this research, we develop next-generation wireless communication systems (200–300 GHz), as millimeter frequencies provide vast amounts of available bandwidth, and shorter wavelengths permit many elements in physically compact arrays. This thesis focuses on building the necessary hardware and infrastructure for such systems.

First, we investigate two important building blocks: low noise amplifiers (LNAs) and frequency multipliers. We present a comprehensive study on multi-stage LNA design based on low total (cascaded) noise figure, i.e., noise measure (NM). 200 GHz LNAs in common-base (CB) and common-emitter (CE) topologies were presented with record noise figure among HBT technologies: 7.4±0.7 dB over 196–216 GHz (CB) and 7.2±0.4 dB over 196–216 GHz (CE). 280 GHz frequency multipliers (8:1 and 16:1) are presented with record spectral purity. The 8:1 frequency multiplier generates −0.6 dBm output power and has a 3-dB bandwidth of 48 GHz. Spurious harmonics are suppressed by more than 28 dBc over the 3-dB bandwidth. The 16:1 frequency multiplier generates −0.6 dBm output power and has a 3-dB bandwidth of 44 GHz. Spurious harmonics are suppressed by more than 26 dBc over the 3-dB bandwidth.

Next, 200 and 280 GHz broadband transceivers in Teledyne 250 nm InP HBT technology are presented. The 280 GHz transmitter IC has a peak conversion gain of 21.6 dB with 36 GHz of 6-dB modulation bandwidth, and dissipates 1535 mW. The measured saturated output power is 14.1 dBm at 272 GHz. The 280 GHz receiver IC has a peak

conversion gain of 22 dB with 34.5 GHz of 6-dB modulation bandwidth, and dissipates 455 mW. The measured double sideband (DSB) noise figure is 10.8 dB at 281.5 GHz. These are the record output power and noise figure reported at and around 280 GHz. The 200 GHz transmitter IC has a record output power (15.3–16.5 dBm) and efficiency (2.71–3.57%) over 195–200 GHz. The 200 GHz receiver IC has a record DSB noise figure (7.7–9.3 dB) over 200–212 GHz.

Finally, we demonstrate packaged 200 GHz 1-channel transmitter and receiver modules with series-fed microstrip patch antennas on glass. The packaged transmitter module has effective isotropic radiated power (EIRP) of 21.6 dBm with 20 GHz 3-dB modulation bandwidth and 62° E-plane and H-plane 3-dB beamwidth. The packaged receiver module has a 14 GHz 3-dB modulation bandwidth and 62° E-plane and H-plane 3-dB beamwidth. Modules can support a wide range of modulation schemes (i.e., QPSK, 16QAM). The link measurements at 7.15 meters showed 13.4% error vector magnitude (EVM) during 32 Gb/s, 16 quadratic-amplitude modulation (QAM) transmission. The integrated transmitter and receiver modules can be used for a broad range of applications, including wireless backhaul, imaging, and radar applications.

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Chapter 1

Introduction

1.1 Milllimeter Wave Wireless Communications

There is an increasing demand for wireless communications between base stations and between base stations and users (Fig. 1.1). This demand will continue to grow due to new innovative applications and the expanding population's need for high-speed internet access. However, the available spectrum is limited. To enhance spectrum efficiency, higher-order modulation schemes can be employed to transmit more bits within the same frequency range. Nevertheless, there comes a point where additional frequency bands need to be utilized. As designers of mm-wave integrated circuits, we can address this challenge by operating at higher frequencies and taking advantage of the broader spectrum available and fit a greater number of channels into compact areas, thereby increasing the overall link capacity [1, 2].

However, several obstacles need to be overcome, including high atmospheric loss, high path loss (proportional to $\frac{\lambda^2}{R^2}$), beam blockage, and the performance limitations of power and noise in devices. Advanced III-V compounds technologies, with high power gain cut-off frequency ($f_{\max}$), made it possible to build complete transceivers above 200 GHz

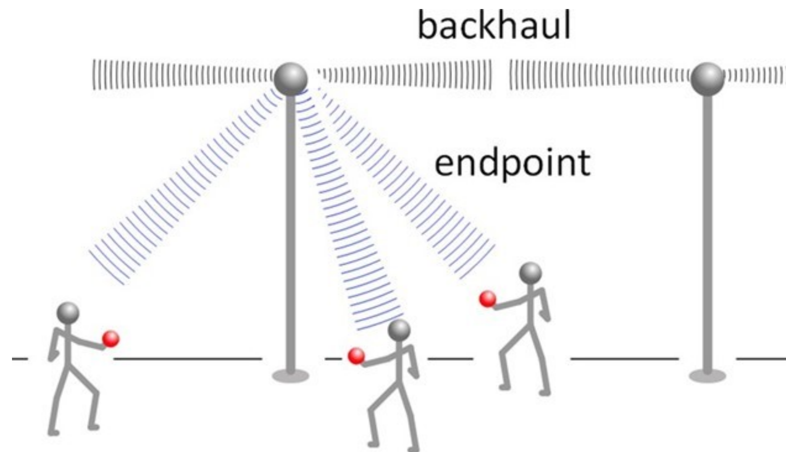


Figure 1.1: Spatially-multiplexed mm-wave base stations for backhaul links and mm-wave wireless communication for the user endpoint (*Courtesy of Prof. Mark J W. Rodwell*).

with high output power and low noise figure. With state-of-the-art power and low-noise amplifiers, the 200–300 GHz frequency range can support wireless backhaul and endpoint links with capacities well above 100 Gb/s in short-range applications (a few hundred meters), serving future communication networks. To realize this, we must first design ICs, and modules, and ultimately demonstrate wireless transmission experiments using these modules (Fig. 1.2).

This thesis proposes solutions for mm-wave wireless communications with the aim of achieving high data rates and enabling long-range communications. The focus is on studying key building blocks such as low noise amplifiers and frequency multipliers. Using these building blocks, broadband high-performance transceivers operating at 280 GHz are developed. Additionally, significant effort is dedicated to IC packaging to ensure the modules can be effectively utilized in real communication systems. Furthermore, transceiver ICs, antennas, and antenna chip transitions are designed and developed at 200 GHz to realize high data rate wireless communications. Experimental tests are conducted indoors, with links at a distance of 7.15 meters, providing practical validation of the proposed approaches.

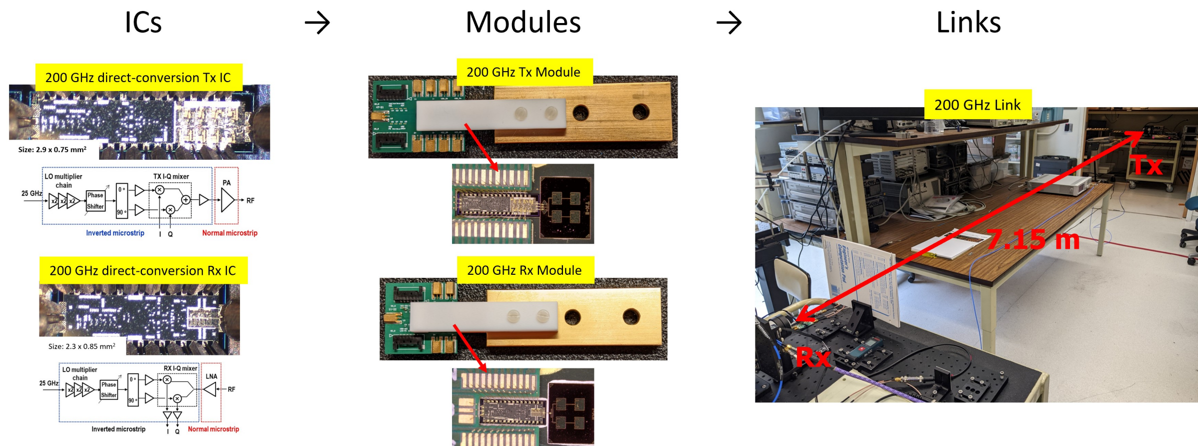


Figure 1.2: Building steps for mm-wave communications: IC design, module design, and link experiments.

1.2 Dissertation Contributions and Organization

Chapter 2 concentrates on the design of multi-stage LNAs using the noise measure technique. We begin with the calculations to determine the minimum noise measure and minimum noise measure impedance. We offer a practical method to illustrate the minimum noise measure impedance on the Smith Chart. We implement 200 GHz LNAs in common-base and common-emitter topologies using the noise measure technique. Lastly, we present the on-wafer measurement results, which include noise figure measurements using a hot-cold noise source.

Chapter 3 focuses on the design of a frequency multiplier chain that utilizes cascaded frequency doublers. We delve into factors associated with the generation of spurious harmonics. Then, we discuss the design of frequency doubler cells and single-ended to differential conversion. We implement broadband 280 GHz 8:1 and 16:1 frequency multiplier chains. Finally, we present on-wafer measurement results, including a precise characterization of spurious harmonics.

Chapter 4 presents a single-channel receiver and transmitter that operates at 280 GHz, providing a comprehensive explanation of the transceiver architecture and its constituent

building blocks. We elucidate the continuous wave (CW) on-wafer measurement results. The receiver's noise figure is measured using a less accurate gain method. Lastly, we conclude by comparing the performance of our Rx and Tx ICs with state-of-the-art transceivers designed for the same *WR*-3 band.

Chapter 5 focuses on the design and characterization of the 200 GHz modules, which utilizes fully integrated InP direct-conversion Tx and Rx ICs, as well as corporate-fed patch antennas on a 50 μm fused silica substrate. We will provide concise information about the design of the 200 GHz ICs and antennas, along with the measured performance results. The leading designer for the transmitter and receiver ICs, including all the building blocks except for the power amplifier, low noise amplifier, and 50 Ω baseband driver, is Prof. Munkyo Seo. The power amplifier is designed by Dr. Ahmed Ahmed, while the antenna and IC-antenna transition are designed by Dr. Amirreza Alizadeh. Lastly, we will showcase the design and assembly process of the modules, as well as the continuous wave over-the-air characterization of these modules.

Chapter 6 focuses on the implementation of short-range (52.5 cm) and long-range (7.15 m) wireless communication links using the transmitter and receiver modules described in Chapter 5. We validate the functionality of the modules through data transmission experiments. The modules are highly integrated and require straightforward physical assembly without waveguide interfaces, and achieve significantly higher transmitter output power. 8 Gbaud 16 QAM data transmission (32 Gb/s) over 7.15 meters, on a link with 10.4 dB added attenuation, showed 13.4% RMS error vector magnitude.

1.3 Permissions and Attributions

The material presented in this dissertation is partially derived from the following publications. The primary contributor to these works is the author of the dissertation,

and the co-authors have granted their approval for the utilization of the material in this dissertation.

1. **U. Soylu**, A. Alizadeh, M. Seo, A. S. H. Ahmed, , M. J. W. Rodwell, “A 202 GHz Link Using Planar Transceiver Modules,” submitted, 2023 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCI-CTS), Monterey, CA, USA.
2. **U. Soylu**, A. Alizadeh, M. Seo, M. J. W. Rodwell, “280-GHz Frequency Multiplier Chains in 250-nm InP HBT Technology,” IEEE Journal of Solid-State Circuits (JSSC), Sept., 2023.
3. **U. Soylu**, A. Alizadeh, A. S. H. Ahmed, M. Seo, M. J. W. Rodwell, “A 272 GHz InP HBT Direct-Conversion Transmitter with 14.1 dBm Output Power,” 2023 18th European Microwave Integrated Circuits Conference (EuMIC), Berlin, Germany.
4. **U. Soylu**, A. Alizadeh, M. Seo, M. J. W. Rodwell, “A 280 GHz InP HBT Direct-Conversion Receiver with 10.8 dB NF,” 2023 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), San Diego, CA, USA.
5. **U. Soylu**, A. Alizadeh, M. Seo, M. J. W. Rodwell, “A 280 GHz (x8) Frequency Multiplier Chain in 250 nm InP HBT,” 2022 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS), Phoenix, AZ, USA.
6. **U. Soylu**, A. S. H. Ahmed, M. Seo, A. Farid, M. J. W. Rodwell, “200 GHz Low Noise Amplifiers in 250 nm InP HBT Technology,” 2021 16th European Microwave Integrated Circuits Conference (EuMIC), London, UK.

Chapter 2

Millimeter-Wave Low Noise Amplifier Fundamentals

2.1 Introduction

Low noise amplifiers (LNAs) are the key components in any receiver. Based on equations 2.1 and 2.2, the receiver's noise figure (NF) sets a boundary for the required minimum detectable signal (MDS) power, thus limiting the transmission range. LNAs are used to suppress the noise contribution of the following stages in the receive chain, such as the down-conversion mixer and baseband amplifier. The LNAs have to minimize their own noise contribution while suppressing this noise. When designing a multi-stage LNA for a low total (cascaded) noise figure, the individual stages should be designed for the lowest noise measure (M), rather than the lowest noise figure (NF). This approach minimizes the total noise contribution of the input and subsequent LNA gain stages. Passive element losses at millimeter-wave frequencies can significantly contribute to the LNA's total noise, so the LNA should be designed to minimize the loss in the input matching network. Therefore, the design procedure is critical.

$$NoiseFloor = 10 \times log_{10}(\frac{kT}{1mW}) + 10 \times log_{10}(\frac{Bandwidth}{1Hz}) + NF \quad (2.1)$$

$$MDS = NoiseFloor + SNR \quad (2.2)$$

The transistor noise measure (M), defined by equation (2.3) where F is the noise figure and G is the gain, establishes a lower limit for the cascaded noise figure ($F_{cascade}$) of a multi-stage LNA, as given by equation (2.4). Moreover, if the embedding circuit is passive, lossless, and reciprocal, the minimum noise measure remains unaffected by the surrounding circuit [3]. In other words, M is an invariant 2-port parameter. Specifically, in common-base and common-emitter configurations, when passive element losses can be neglected, the minimum $F_{cascade}$ and M values are identical. These values remain unchanged even if the stage is unilateralized or capacitively neutralized, or if the gain is maximized using Singhakowinta's technique [4].

$$M = \frac{F-1}{1-G^{-1}} \quad (2.3)$$

$$F_{cascade} = M + 1 = F + \frac{F-1}{G} + \frac{F-1}{G^2} + ... = \frac{F-G^{-1}}{1-G^{-1}} \quad (2.4)$$

This chapter will primarily concentrate on the design of multi-stage LNAs using the noise measure technique. It will delve into the calculations for determining the minimum noise measure and minimum noise measure impedance. Additionally, a practical method for illustrating the minimum noise measure impedance on the Smith Chart will be provided. The chapter will showcase 200 GHz LNAs employing common-base and common-emitter topologies. Finally, the on-wafer measurement results, including NF measurements using a hot-cold noise source, will be presented.

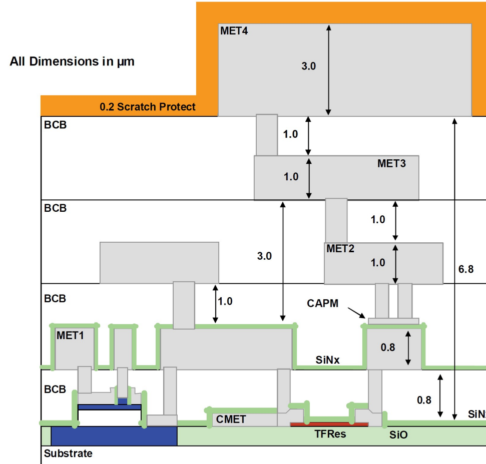


Figure 2.1: Cross-section view of 250 nm InP HBT technology.

2.2 250 nm InP HBT Technology

All the integrated circuits (ICs) presented in this thesis are implemented using Teledyne's 250 nm InP HBT technology. Figure 2.1 provides a cross-sectional view of the 250 nm InP technology [5]. This technology offers a maximum power gain cut-off frequency (f_{max}) of 650 GHz at the top metal layer. It also supports a maximum current density of 3 mA/μm and has a breakdown voltage ($V_{\text{BR,CEO}}$) of 4.5 V. Additionally, the technology includes four Au interconnect layers, 50 Ω/square thin film resistors, and 0.3 fF/μm^2 MIM (Metal-Insulator-Metal) capacitors. The 50 Ω microstrip lines, with the top metal (M4) serving as the signal line and the bottom metal (M1) as the ground, exhibit a loss of 0.88 dB/mm (equivalent to 0.9 dB/λ) at 200 GHz. At 280 GHz, the loss increases to 1.0 dB/mm (equivalent to 0.78 dB/λ). The transmission line losses, which include skin effect loss, dielectric loss, and radiation loss, escalate in dB/mm as the frequency rises. Conversely, the transmission line loss in terms of dB/λ decreases as the frequency increases. This characteristic provides an additional advantage in high-frequency design, as the loss of transmission line-based matching network components diminishes.

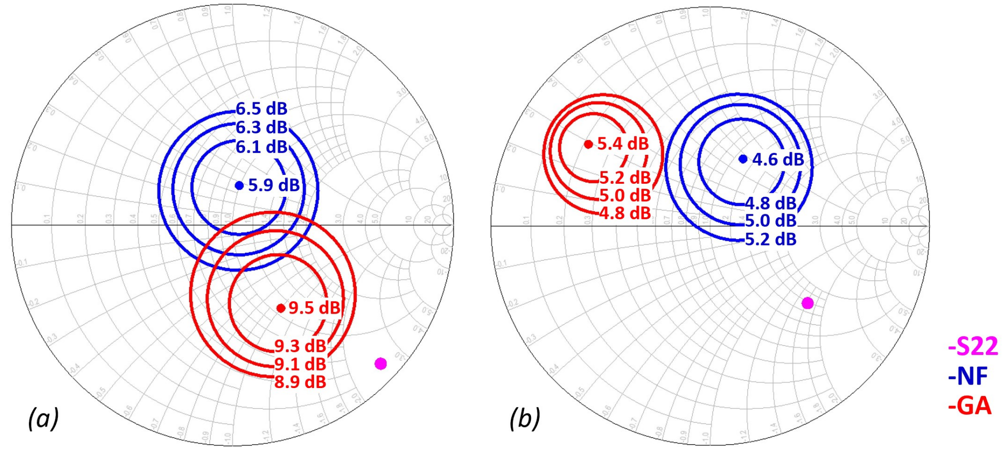


Figure 2.2: S_{22}, NF and GA circles at 200 GHz. Data is for (a) (0.25 × 5 μm^2) HBT in CB configuration with 200 fF base capacitance and (b) (0.25 × 3 μm^2) HBT in CE configuration, biased at V_{CB}=0.4 and J_{E}=0.5 mA/μm.

2.3 Low Noise Amplifier Design

At millimeter-wave frequencies, receivers implemented in SiGe and InP HBT technologies have demonstrated greater integration scales compared to III–V HEMT technologies, however, HEMTs offer better noise performance [5, 6, 7, 8, 9, 10, 11]. Reducing HBT LNA noise figure will make all-HBT 200–300 GHz receivers more competitive, and in hybrid receivers combining a HEMT LNA and an HBT IC for the post-LNA and remaining receiver mm-wave stages, will minimize the required gain, hence number of stages, in the HEMT LNA.

Since the cascaded noise figure ($F_{cascade}$) is independent of the stage configuration, the choice of stage configuration is based on either a high feasible bandwidth or high gain per stage. The common-base (CB) stage provides greater gain per stage (Fig. 2.2a), hence noise contributions associated with loss in the output matching network are reduced. Further, with greater gain per stage, fewer stages are required, reducing DC power. Because the common-emitter (CE) stage has lower output impedance (Fig. 2.2b), its output matching network is more readily designed for wide bandwidth.

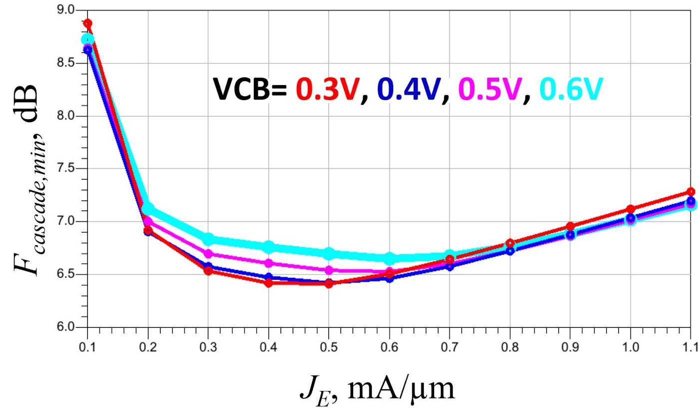


Figure 2.3: Minimum $F_{cascade}$ as a function of emitter current density (J_{E}) and collector-base voltage (V_{CB}) for a $0.25 \times 5\ \mu\mathrm{m}^2$ HBT in CB configuration with 200 fF base capacitance at 200 GHz.

2.3.1 Determining Bias Condition

Most widely-used RF computer-aided design programs compute NF_{min} but not M_{min}, and compute NF but not M as a function of source impedance. To address this limitation, Python scripts were written to compute these quantities from the output of the CAD simulation software. Given this, the first step in the design is to determine, from CAD simulation, the emitter current density and collector-base voltage giving the lowest M, hence the lowest $F_{cascade}$. For the IC technology used, at 200 GHz, the simulated minimum $F_{cascade}$ of a bare $0.25 \times 5\ \mu\mathrm{m}^2$ device is 6.4 dB with J_{E}=0.5 mA/μm and V_{CB}=0.4 V (Fig. 2.3). Figure 2.3 illustrates the best noise performance attainable with this technology. Slightly higher bias settings will be used to achieve lower $F_{cascade}$ when output-matching network losses are considered.

2.3.2 Displaying source impedance for minimum M

In addition to noise figure (NF) and available gain (GA), the noise measure (M) can also be represented as a function of the source reflection coefficient, resulting in circles of constant M [12]. However, widely-used RF computer-aided design programs do not

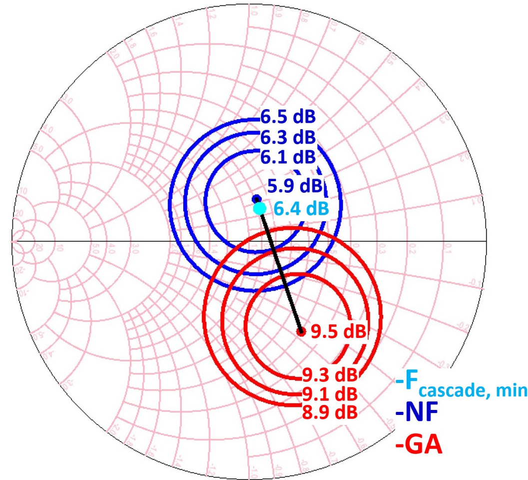


Figure 2.4: CAD display, in Keysight ADS, of the contours of constant noise figure and available gain (GA) in the plane of the source reflection coefficient. A Python script draws a line (black) between the centers of the NF and GA circles, computing the minimum noise measure along this line. Data is for an 0.25 × 5 μm^2 HBT in CB configuration with 200 fF base capacitance biased at V_{CB}=0.4 and J_{E}=0.5 mA/μm, simulated at 200 GHz.

typically offer this capability. To address this, a Python script was written to approximate the M_{min} and the associated source impedance by utilizing the circles of constant NF and GA (Fig. 2.4). The script works by drawing a line between the centers of the NF and GA circles, and then calculating the value of M for each point on this line. The script determines the point on the line that yields the M_{min} (minimum noise measure impedance). This approach allows for the determination of M_{min} using the available data from the CAD simulation, enabling a more comprehensive analysis of the circuit's noise performance.

If the NF and GA circles were perfectly concentric, the impedance for M_{min} would indeed lie along the constructed line, and the graphical algorithm described earlier would accurately determine M_{min} and the associated impedance. However, in practice, the circles may deviate to some extent from this ideal scenario, as shown in Figure 2.4. Although the deviation is not significant, a more precise procedure can be employed by utilizing the relationships of [12].

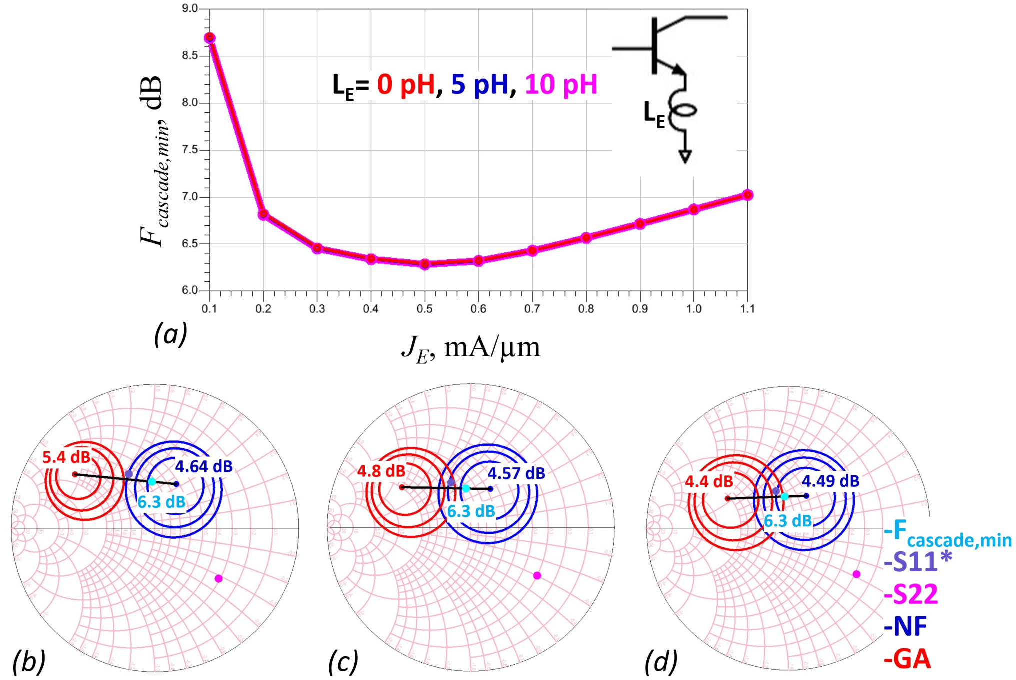


Figure 2.5: (a) Minimum $F_{cascade}$ as a function of emitter current density ($J_{\rm E}$) and emitter degeneration ($L_{\rm E}$) for a 0.25 × 3 μm^2 HBT in CE configuration biased at $V_{\rm CB}$=0.4 V. The minimum M impedance, S_{11} conjugate, S_{22}, NF and GA circles: (b) $L_{\rm E}$= 0 pH, (c) $L_{\rm E}$= 5 pH, (d) $L_{\rm E}$= 10 pH.

Figure 2.5a illustrates the impact of emitter degeneration ($L_{\rm E}$) on the minimum $F_{cascade}$ of a CE device. As $L_{\rm E}$ increases, the maximum GA decreases, and the minimum NF also decreases. However, these changes are balanced in such a way that the minimum $F_{cascade}$ remains constant. The values of minimum $F_{cascade}$ for $L_{\rm E}$=0, 5, 10 pH overlap with each other. Figure 2.5(b–d) show the NF and GA circles, and the minimum M impedance.

2.3.3 Area Scaling and Degeneration

In CE LNAs, introducing an appropriate nonzero value for the emitter inductive reactance ($jwL_{\rm E}$) enables input tuning for a zero input reflection coefficient while simultaneously achieving minimum $F_{cascade}$. This tuning is accomplished without increasing

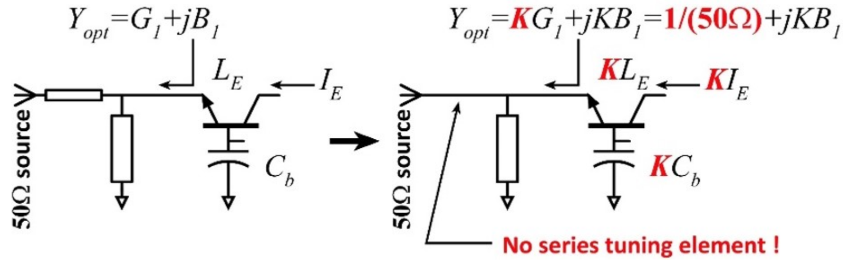


Figure 2.6: (a) Input matching network without proper emitter junction area scaling, (b) input matching network with proper emitter junction area scaling.

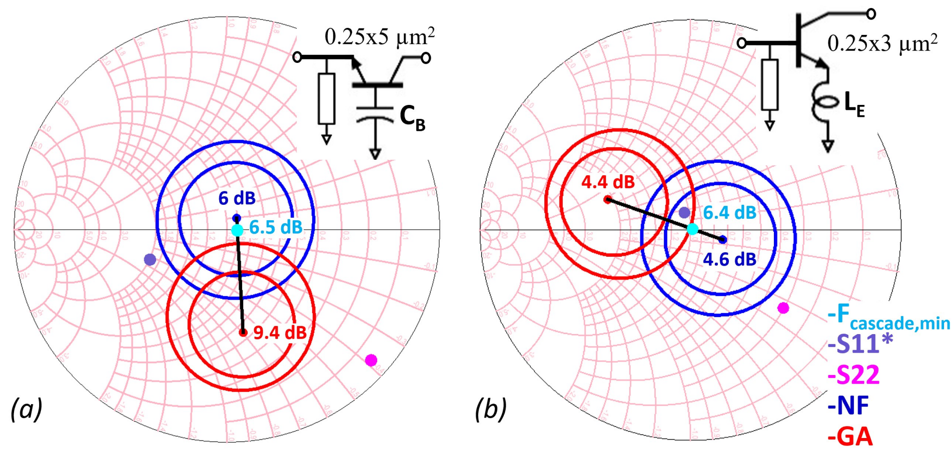


Figure 2.7: (a) Input matched CB stage and (b) input matched CE stage with proper emitter junction area scaling.

the $F_{cascade}$, as shown in Figure 2.5. On the other hand, in CB LNAs, a nonzero value for the base capacitive impedance ($1/jwC_{\mathrm{B}}$) serves the same purpose. Subsequently, the HBT junction area is scaled, together with the DC current and the base capacitor, so that the source conductance for minimum noise measure is 20 mS (Fig. 2.6); this permits the input stage to be noise-matched to 50 Ω with a single inductive shunt element (Fig. 2.4), avoiding the added attenuation, hence the added noise, of a series matching element, equation 2.5.

$$F_{cascade} = F_{input_match} + F_{transistor} + \frac{F_{output_match} - 1}{G} + ... = \frac{F - G^{-1}}{1 - G^{-1}} \qquad (2.5)$$

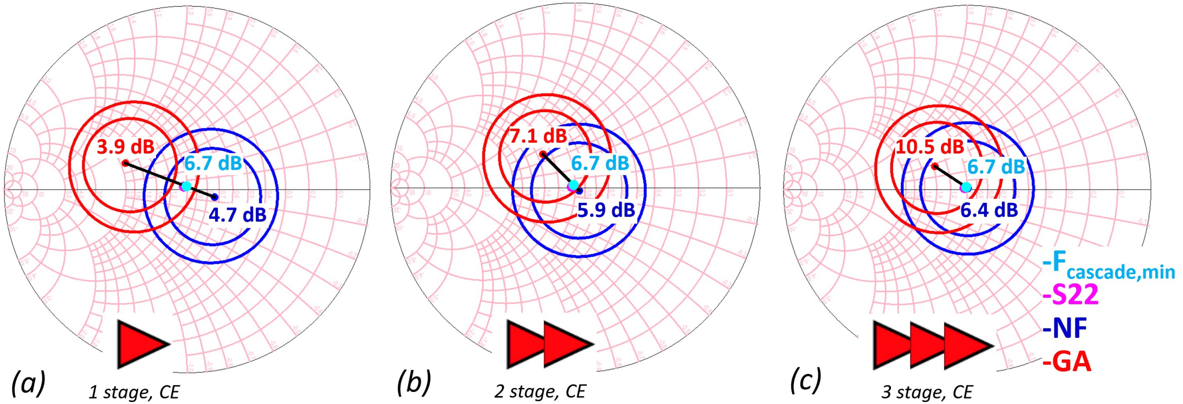


Figure 2.8: Minimum $F_{cascade}$ impedance, S_{22}, NF and GA circles for cascaded stages in CE configuration: (a) 1 stage, (b) 2 stages, (c) 3 stages.

2.3.4 Input/Output Matching Network and Cascading

Figure 2.7 shows CB ($5\,\mu$m) and CE ($3\,\mu$m) stages with proper emitter junction area scaling to minimize the noise contribution of the input matching network. Despite the presence of the input matching network loss, the minimum $F_{cascade}$ is only degraded by 0.1 dB. In the CB stage, the base capacitance is tuned to achieve in-band stabilization, which results in a small-signal mismatch. On the other hand, in the CE stage, the emitter inductance is easily tuned to provide small-signal matching and out-of-band stabilization (Fig. 2.7).

In a multistage LNA design, for the lowest noise, each stage output is matched to the M_{min} impedance of the cascaded stage. This can be accomplished in a stage-by-stage design procedure in which each stage is designed to have a M_{min} for a $50\,\Omega$ external source impedance and maximum associated gain for a $50\,\Omega$ external load impedance. LNA design must however balance noise against bandwidth and dynamic range. Consequently, the output tuning of the CB design was adjusted to increase the stage bandwidth and 1 dB gain compression point.

In Figure 2.8a, the NF and GA circles represent the CE stage that is matched to have

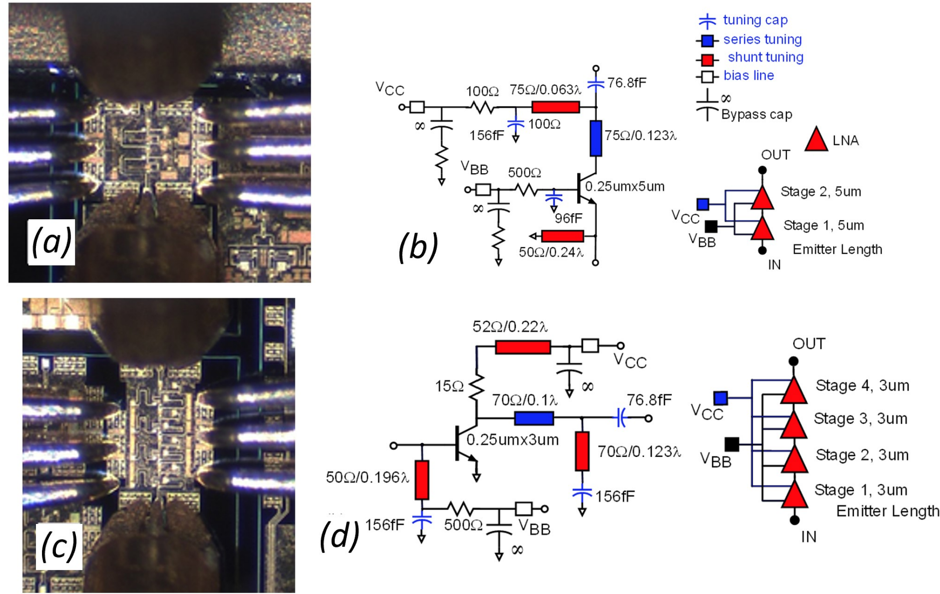


Figure 2.9: CB amplifier: (a) die photo and (b) amplifier circuit diagram. The die area, including DC routing and pads is 0.49 × 0.425 mm^2. CE amplifier: (c) die photo and (d) amplifier circuit diagram. The die area, including DC routing and pads is 0.45 × 0.63 mm^2.

a $50\,\Omega$ M_{min} impedance, with its output also matched to $50\,\Omega$. As the matched stage is cascaded, not only NF_{min} converge to minimum $F_{cascade}$, but also NF_{min} impedance converges to M_{min} impedance (Fig 2.8).

2.4 Measurement Results

2.4.1 S-Parameter Measurements

Figure 2.9 shows the chip micrographs. Measurements are performed on the 3 mil thinned die. S-parameters were measured using a Keysight network analyzer with Oleson *WR*-3 frequency extender modules and GGB *WR*-3 wafer probes. A short-open-load-thru (SOLT) calibration standard on an external substrate moves the reference plane to the probe tips.

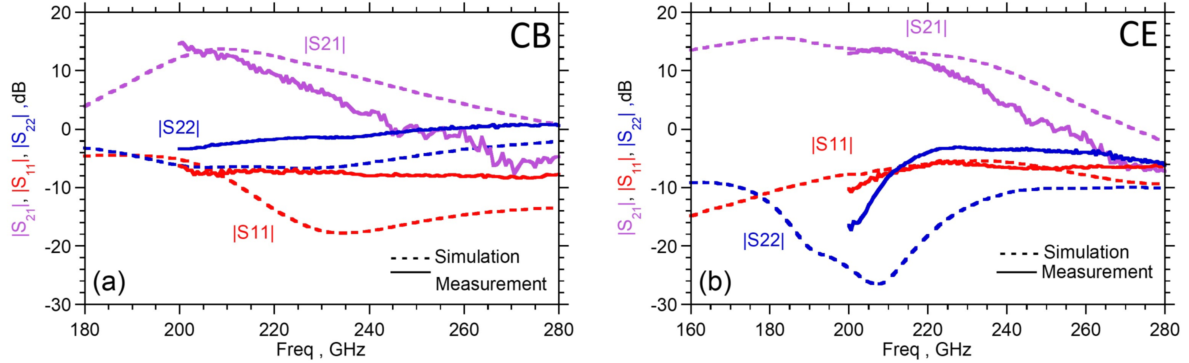


Figure 2.10: Measured (solid) and simulated (dashed) S-parameters: (a) CB and (b) CE amplifier.

Approximately 5% frequency downshift is observed between the amplifier's measured and simulated S-parameters (Fig. 2.10). The device model does not include base inductance, which is the main reason of the frequency shift. By adding extra series inductance to the base, the device model is adjusted.

The CB amplifier (Fig. 2.9a) was biased at $V_{\mathrm{CCLNA}} = 1.5\,\mathrm{V}$, $V_{\mathrm{BBLNA}} = 0.85\,\mathrm{V}$, drawing $I_{\mathrm{CCLNA}} = 6.03\,\mathrm{mA}$, and $I_{\mathrm{BBLNA}} = 0.264\,\mathrm{mA}$. The peak measured small-signal gain ($|\ S21\ |$) is 14.5 dB at 200 GHz, in good agreement with the simulation. The CE amplifier (Fig. 2.9c) was biased at $V_{\mathrm{CCLNA}} = 1.6\,\mathrm{V}$, $V_{\mathrm{BBLNA}} = 0.87\,\mathrm{V}$, drawing $I_{\mathrm{CCLNA}} = 11.68\,\mathrm{mA}$, and $I_{\mathrm{BBLNA}} = 0.436\,\mathrm{mA}$. The peak measured small-signal gain ($|\ S21\ |$) is 13.69 dB at 206 GHz. The CB amplifier has a narrower bandwidth due to the higher CB output impedance.

2.4.2 Power Measurements

Figure 2.11 shows the procedure for gain compression measurements [13], and the setup in the calibration and measuring phases are shown. The 200 GHz signal is generated by a synthesizer (N5183B) and an 8:1 VDI frequency multiplier. The signal is passed through a directional coupler to monitor the input power, and is passed through a *WR*-5

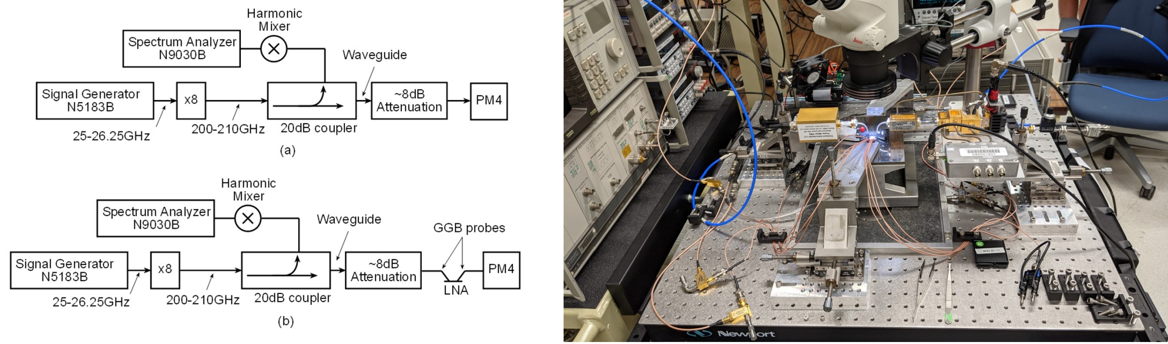


Figure 2.11: Power measurement setup: (a) Calibration phase and (b) measurement phase.

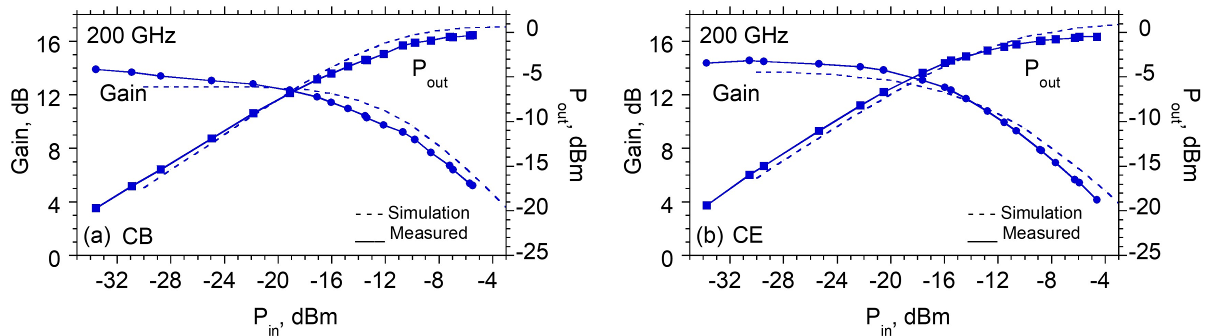


Figure 2.12: Gain compression characteristics: (a) CB and (b) CE amplifier.

fixed attenuator to obtain power levels within the desired range to drive the LNA. By placing an Erickson power meter (PM4) at the attenuator output, and comparing its power measurement to that of the spectrum analyzer, the measurement of input power is thereby calibrated (Fig. 2.11a). The signal source is then connected, via GGB probes, to the amplifier input, and the amplifier output monitored by the PM4 power meter.

The CB and CE amplifiers are biased at $V_{\text{CCLNA}} = 1.5\,\text{V}$, $V_{\text{BBLNA}} = 0.864\,\text{V}$, drawing $I_{\text{CCLNA}} = 5.98\,\text{mA}$, $I_{\text{BBLNA}} = 0.268\,\text{mA}$ and $V_{\text{CCLNA}} = 1.6\,\text{V}$, $V_{\text{BBLNA}} = 0.87\,\text{V}$, drawing $I_{\text{CCLNA}} = 11.73\,\text{mA}$, and $I_{\text{BBLNA}} = 0.522\,\text{mA}$ respectively. The CB and CE amplifiers have $-21.1\,\text{dBm}$, and $-18.2\,\text{dBm}$ input referred P_{1dB} with 12.69 dB and 13.3 dB associated gain, respectively, at 200 GHz (Fig. 2.12). The CB amplifier consumes 9.2 mW while the CE amplifier consumes 19.22 mW.

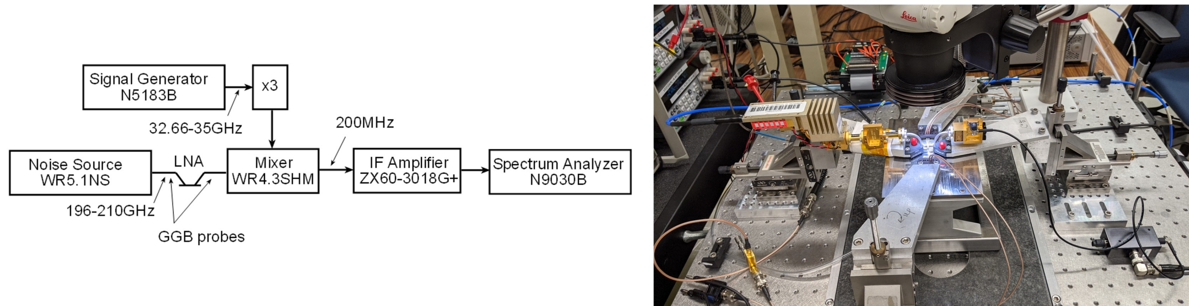


Figure 2.13: Noise measurement setup.

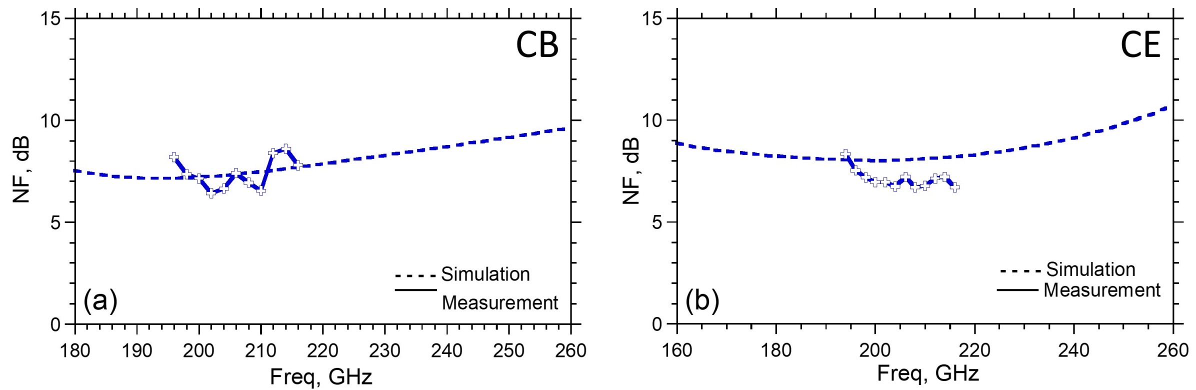


Figure 2.14: Measured (solid) and simulated (dashed) NF: (a) CB and (b) CE amplifier.

2.4.3 Noise Measurements

The LNA noise figure is measured using the hot/cold Y parameter method (Fig. 2.13). A VDI-WR5.1NS hot/cold noise source connected to the LNA input using a GGB *WR*-5 wafer probe. The *WR*-5 probe loss is measured by landing probes on the through structure on the impedance standard substrate. The probe loss is found to be 2.0 dB at 200 GHz, and is deembedded from the measured noise figure. A ∼20 dB low noise post-amplifier (Mini Circuits, ZX60-3018G+) used to reduce the noise contribution from the spectrum analyzer. The subharmonic mixer's (VDI-WR4.3SHM) LO signal was supplied by a QuinStar x3 *WR*-8 multiplier chain (QMM-933510030) and a signal generator (N5183B). The output noise power spectral density was measured at 200 MHz

Table 2.1: Comparison of the recently reported >150 GHz low noise amplifiers.

Reference†	**Technology**	**Topology**	**Freq. (GHz)**	**Gain (dB)**	$P_{\mathbf{DC}}$ **(mW)**	**NF (dB)**
[6]	CMOS 32 nm	CS	200-220	10-18	44.5	11
[7]	SiGe HBT 250 nm	Cascode diff.	156	26	NA	8.5
[8]	SiGe HBT 130 nm	Cascode diff.	220	18	151.2	16
[9]	GaAs mHEMT 50 nm	CS	178-185	24.5	24	3.5
[10]	GaAs mHEMT 50 nm	CS	206	16	NA	4.8
[11]	InP HBT 250 nm	CE	265	24	81.7	10
[5]	InP HBT 250 nm	Cascode	288	8.4	NA	11.2
This work[14]	**InP HBT 250 nm**	**CE**	**200**	**13**	**19.22**	**7.2**
This work[14]	**InP HBT 250 nm**	**CB**	**200**	**14.5**	**9.2**	**7.4**

† Spec values for other works were extracted from their text or otherwise estimated from the plots.

using a spectrum analyzer (N9030B). The CB amplifier (Fig. 2.14a) shows 7.4±0.7 dB NF over 196–216 GHz, while the CE amplifier (Fig. 2.14b) shows 7.2±0.4 dB NF over 196–216 GHz.

2.5 Summary and Conclusion

Table 2.1 compares the performance of the LNAs designed above 150 GHz. To the authors' knowledge, this work demonstrates record noise performance for bipolar transistor amplifiers operating near 200 GHz.

Chapter 3

Millimeter-Wave Frequency Generation Fundamentals

3.1 Introduction

One key challenge in transceiver design is the generation of a local oscillator (LO) (Fig. 3.1a). The LO can be directly generated by a phase-locked loop (PLL), producing an output at the LO frequency (Fig. 3.1b). In this case, the main challenge lies in designing a voltage-controlled oscillator (VCO) with sufficiently low phase noise, as the resulting phase noise outside the PLL loop bandwidth is determined by the VCO.

Alternatively, the LO can be generated by a lower-frequency PLL followed by an N:1 frequency multiplier (Fig. 3.1c). Although this approach increases the PLL phase noise by $20\log(N)$ dB, it can still result in lower phase noise compared to a PLL operating directly at 200–300 GHz. Choosing a larger multiplication factor N allows for a lower input frequency, which facilitates the packaging of the transceiver IC. On the other hand, selecting a smaller N increases the frequency separation of spurious harmonics generated by the multiplier chain, making it easier to suppress them through filtering.

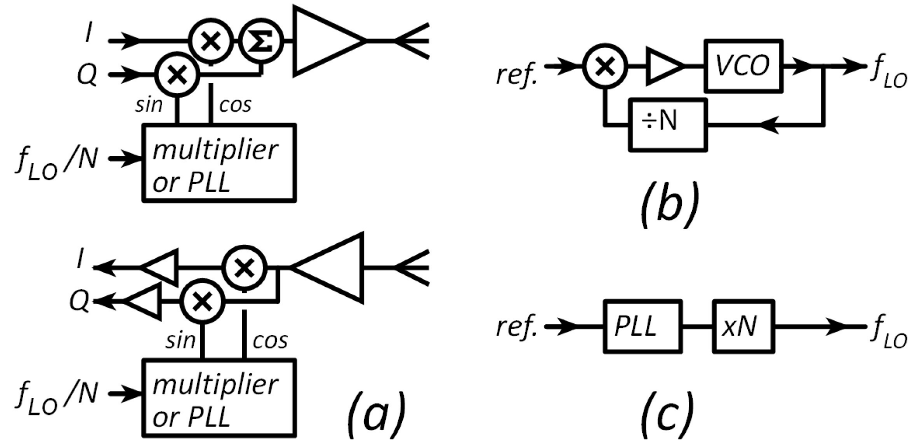


Figure 3.1: (a) Millimeter-wave transceiver architectures with (b) PLLs and (c) multiplier chains for on-chip LO generation.

These spurious LO multiplier harmonics can lead to receivers receiving and transmitters radiating signals at unintended frequencies, causing interference. Key design objectives for such multipliers include the strong rejection of spurious harmonics to improve the signal-to-interference ratio and low DC power consumption to enhance the efficiency of transceivers.

This chapter will primarily focus on the design of a frequency multiplier chain utilizing cascaded frequency doublers. It will explore factors related to the generation of spurious harmonics. Moreover, it will cover the design of frequency doubler cells and single-ended to differential conversion. The chapter will showcase broadband 280 GHz 8:1 and 16:1 frequency multiplier chains. Lastly, it will present on-wafer measurement results, including precise characterization of spurious harmonics. The 280 GHz 8:1 frequency multiplier chain has been integrated into transceivers, which will be explained in Chapter 4.

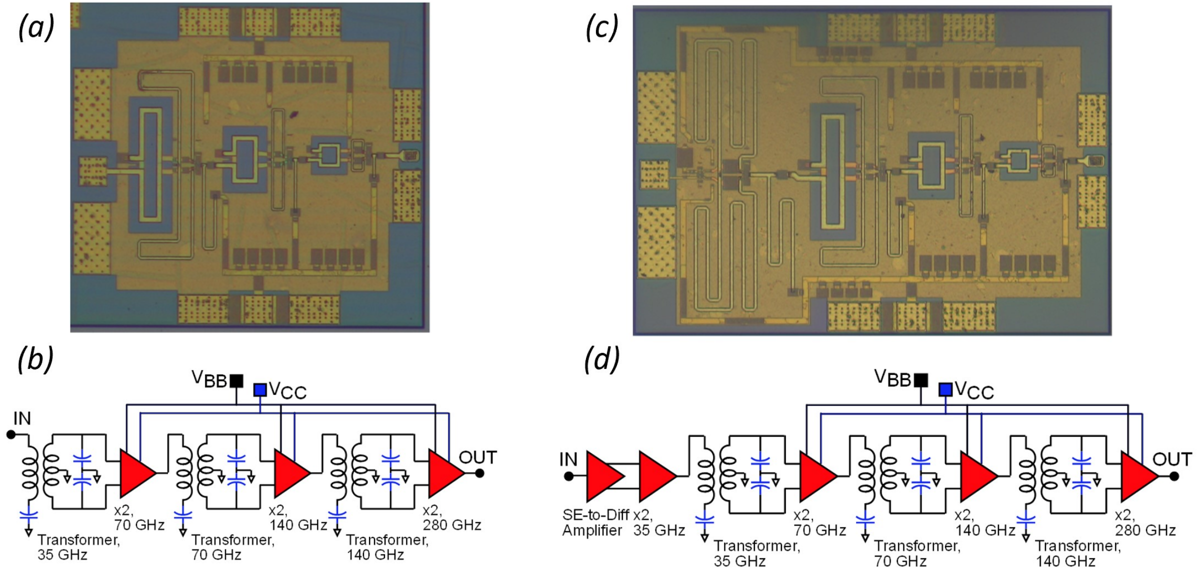


Figure 3.2: (a) Die photograph and (b) block diagram of the 8:1 frequency multiplier; the die area is 0.92 mm×0.8 mm, while the core area, without DC routing and pads, is 0.7 mm×0.56 mm. (c) Die photograph and (d) block diagram of the 16:1 frequency multiplier; the die area is 1.2 mm×0.8 mm, while the core area, without DC routing and pads, is 1 mm×0.75 mm.

3.2 Frequency Multiplier Chain Design

Integrated frequency multiplier chains operating near 280 GHz have been demonstrated in several technologies [15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29]. In this chapter, we will present *WR*-3 band 8:1 and 16:1 frequency multipliers that achieve record spectral purity for designs operating near 280 GHz. The 8:1 multiplier utilizes three cascaded push-push emitter-coupled pairs, serving as balanced frequency doublers. Single-ended to differential conversion is provided by 1:1 transformers at 35, 70, and 140 GHz. On the other hand, the 16:1 multiplier includes an additional input emitter-coupled push-push doubler, with its drive signal generated by a transistor differential input stage. The key design features encompass the selection of the transistor load-line for high efficiency, as well as single-ended to differential conversion with low phase and amplitude imbalance to ensure strong suppression of spurious harmonics.

As depicted in Figures 3.2(a–b), the 8:1 frequency multiplier employs three cascaded doublers to generate a frequency of 280 GHz from a 35 GHz input. Each active doubler cell features a differential input but a single-ended output. Inter-stage transformers are utilized for the necessary single-ended to differential conversion instead of transistor differential amplifiers. Transformers offer superior amplitude and phase balance at high frequencies while consuming no DC power. Illustrated in Figures 3.2(c–d), the 16:1 frequency multiplier incorporates an additional input frequency doubler, producing 280 GHz from a 17.5 GHz input. To optimize die area, this doubler utilizes a transistor differential amplifier instead of an input transformer. Despite consuming greater DC power and occupying a larger die area, the lower input frequency (17.5 GHz compared to 35 GHz) eases IC packaging challenges.

3.2.1 Multiplier Chain Spurious Harmonics

If each frequency doubler in the 16:1 frequency multiplier generated only the 2$^{\text{nd}}$ harmonic of its input frequency, the successive stage output frequencies would be $2f_{\text{in}}$, $4f_{\text{in}}$, $8f_{\text{in}}$, and $16f_{\text{in}}$, where f_{in} represents the input frequency. However, it is important to note that each doubler will also generate unwanted spurious output signals at other harmonics. As we will explore further, the spurious harmonics produced by the initial doubler stages will result in multiplier chain spurious output harmonics that are closest to the desired output harmonic. Therefore, these spurious harmonics pose the greatest design concern.

In the 16:1 frequency multiplier (Fig. 3.3b) driven at f_{in} =17.5 GHz, the spurious harmonic outputs from the first frequency doubler at frequencies f_{in} and $3f_{\text{in}}$ will, upon passing through the second, third, and fourth doublers, generate unwanted outputs of the 16:1 frequency multiplier chain at frequencies (f_{in}, $2f_{\text{in}}$, ..., $24f_{\text{in}}$). These spurious

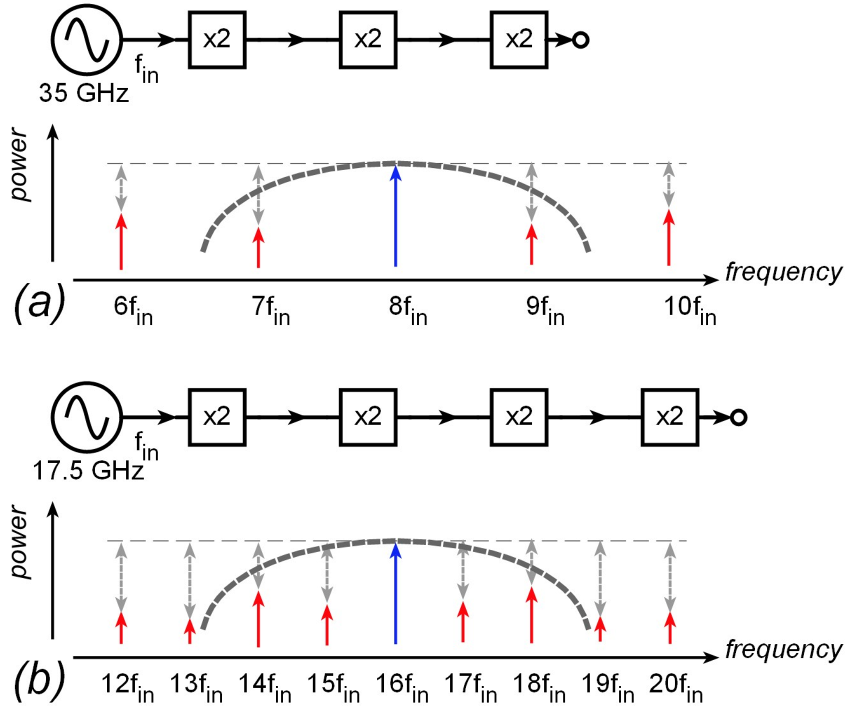


Figure 3.3: The output spectrum of (a) 8:1 FMC and (b) 16:1 FMC.

harmonics, such as $15f_{\text{in}}$ and $17f_{\text{in}}$, are separated in frequency from the desired output harmonic $16f_{\text{in}}$ by $\pm f_{\text{in}}$. Conversely, the spurious harmonic outputs from the second frequency doubler at frequencies $2f_{\text{in}}$ and $6f_{\text{in}}$, after passing through the third and fourth doublers, produce undesired outputs of the 16:1 multiplier chain at frequencies ($2f_{\text{in}}$, $4f_{\text{in}}$, ..., $24f_{\text{in}}$), with spurious harmonics like $14f_{\text{in}}$ and $18f_{\text{in}}$ separated in frequency from the desired output harmonic $16f_{\text{in}}$ by $\pm 2f_{\text{in}}$. This pattern continues, where the spurious harmonics generated by the third doubler stage produce undesired outputs of the 16:1 multiplier chain separated from the desired output harmonic by at least $\pm 4f_{\text{in}}$, and those generated by the fourth stage produce spurious signals at the 16:1 multiplier chain output separated from the desired harmonic by at least $\pm 8f_{\text{in}}$. Since spurious harmonics with frequencies far from the desired harmonic can be effectively suppressed by band-pass filters in the transmitter or receiver, the spurious harmonics generated by the first several multiplier stages are of the greatest concern.

Within each frequency doubler stage, the differential circuit would suppress the adjacent fundamental and 3rd spurious harmonics if it were perfectly symmetrical. However, the presence of transistor or bias circuit mismatch, as well as unbalanced drive signals, disrupts this symmetry and leads to the generation of spurious harmonics. The inter-stage networks serve multiple functions, including single-ended to differential conversion, impedance transformation, and band-pass filtering. These inter-stage networks not only enhance the conversion process but also contribute to improved suppression of spurious harmonics.

3.2.2 Balanced Frequency Doubler Cell

The push-push emitter-coupled pair [30], when fabricated with identical transistors and provided with symmetric DC bias and RF drive signals, exhibits symmetry and does not generate spurious odd harmonics. Figure 3.4 illustrates the circuit, including its voltage and current waveforms, as well as the transistor loadline. The output tuning network of amplifiers can be designed to optimize either the largest small-signal gain or, in the case of power amplifiers, the highest saturated output power. The latter scenario involves a loadline between the points ($I_c = I_{c,max}, V_{ce} = V_{ce,sat}$) and ($I_c = 0\,\mathrm{A}$, $V_{ce} = V_{BR,CEO}$). Similarly, the tuning of the multiplier output can prioritize either the greatest conversion gain or the highest saturated output power. When tuned for maximum saturated output power, the loadline, as shown in Figure 3.4, follows the equation:

$$V_{ce} = (V_{max} - V_{ce,sat})\left(1 - (I_c/I_{max})^2\right) + V_{ce,sat} \tag{3.1}$$

Here, $V_{max} = V_{BR,CEO}$. The designs presented here utilize the above loadline but with a reduced $V_{max} = 2.0\,\mathrm{V}$, which is smaller than $V_{BR,CEO}$. This reduction in output voltage

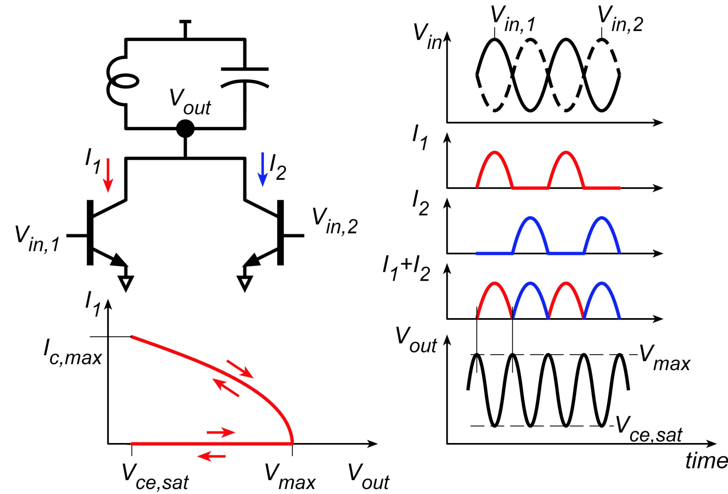


Figure 3.4: Balanced frequency doubler voltage waveforms, current waveforms, and transistor loadline.

lowers the doubler's saturated output power but increases its gain. By balancing output power and gain, the designs aim to maximize the power-added efficiency of the doubler.

To achieve high transistor bandwidth, the emitter stripe lengths in the output doubler stage are adjusted to set the output power at the desired level, while ensuring that the maximum current densities are set near the technology's maximum safe value. Similarly, preceding stages are sized in a similar manner, ensuring that each stage has enough output power to drive the subsequent stage. This design approach eliminates the need for inter-stage amplifiers, thereby avoiding the additional power consumption associated with their use.

When driven at f_{in}, the doubler not only produces outputs at $2f_{\text{in}}$ but also at DC. The RF to DC conversion in the doubler can impact the DC bias of the transistors, leading to a change in the output power at $2f_{\text{in}}$. Figure 3.5a illustrates that if the emitter-coupled pair is biased with a fixed DC voltage V_{BE} (using, for example, a current mirror), increasing the RF input power will result in an increased total charge delivered by each transistor to the output resonant circuit during the $1/2f_{\text{in}}$ conduction period of each transistor. As a result, the amplitude of the RF output voltage at $2f_{\text{in}}$ will also increase. Alternatively, in

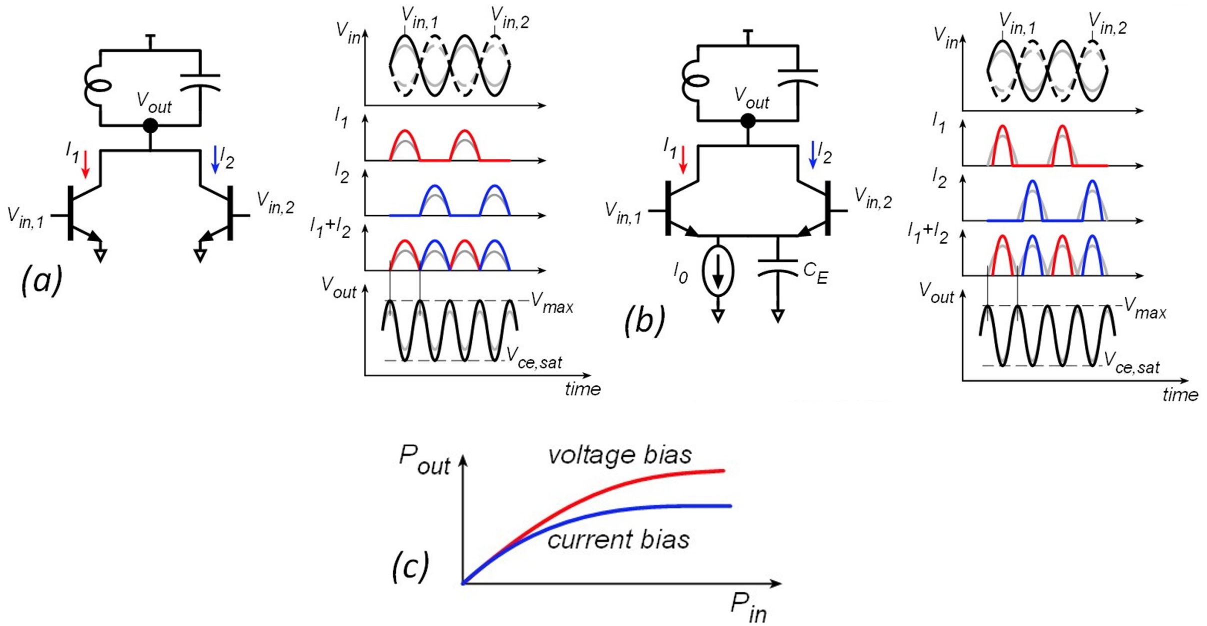


Figure 3.5: Balanced frequency doubler with voltage and current waveforms with varying drive power for designs with (a) fixed voltage bias, and (b) fixed emitter current bias. The fixed emitter current bias design shows a smaller variation (c) of output power with variations of input power.

Figure 3.5b, if the emitter-coupled pair is DC biased with a constant DC current source I_0, and this current is bypassed to ground with a low impedance at f_{in} by C_{E}, then each transistor will deliver a charge of $I_0/2f_{\mathrm{in}}$ to the output circuit during the $1/2f_{\mathrm{in}}$ conduction period. This charge delivery is independent of the amplitude of the RF input signal. This configuration regulates the pulse charge delivered to the output resonator, reducing the variation of the doubler output power in response to input power variations, as depicted in Figure 3.5c.

To avoid the need for an increased supply voltage that would be required to implement the current source I_0 with a transistor, the emitter-coupled pair is biased using a base resistor $R_{\mathrm{B}} = 500\,\Omega$ and an emitter resistor $R_{\mathrm{EE}} = 100\,\Omega$, as shown in Figure 3.6. This configuration establishes a DC bias current $I_0 = (V_{\mathrm{BB}} - V_{\mathrm{BE,DC}})/(R_{\mathrm{EE}} + R_{\mathrm{B}}/\beta)$. The chosen bias current provides a nearly constant value, as variations in the input RF drive

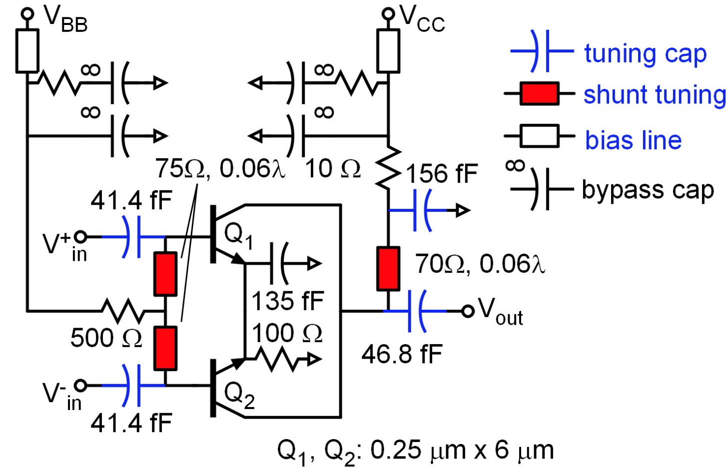


Figure 3.6: Schematic diagram of the 140 GHz to 280 GHz frequency doubler with input and output matching networks.

power result in only small changes in $V_{\mathrm{BE,DC}}$. At low frequencies, the presence of R_{EE} ensures common-mode stability.

Figure 3.6 displays the schematic diagram of the 140 to 280 GHz frequency doubler. Each transistor has an emitter-base junction size of $0.25\,\mu\mathrm{m}\times 6\,\mu\mathrm{m}$ and is biased at $J_{\mathrm{E}} = 0.8\,\mathrm{mA}/\mu\mathrm{m}$ and V_{CB}=0.8 V. For maximum output power (P_{out}), the load line can be adjusted to swing between V_{CEsat} and $V_{\mathrm{BR,CEO}}$. However, in this case, the load line is tuned with a smaller V_{max} to optimize power-added efficiency (PAE). The output network is also tuned accordingly to achieve this transistor loadline when the external load is 50 Ω at 280 GHz. The large signal input impedances at V_{in}^{+} and V_{in}^{-} are tuned to 50 Ω at 140 GHz. In Figure 3.7a, the simulated load line is shown, while Figure 3.7b illustrates the simulated output power as a function of input power, including the input transformer in the simulation. The simulated P_{out} is 1 dBm with an input power of −1 dBm. Therefore, considering similar characteristics for all doublers in the chain, the use of inter-stage amplifiers is not necessary.

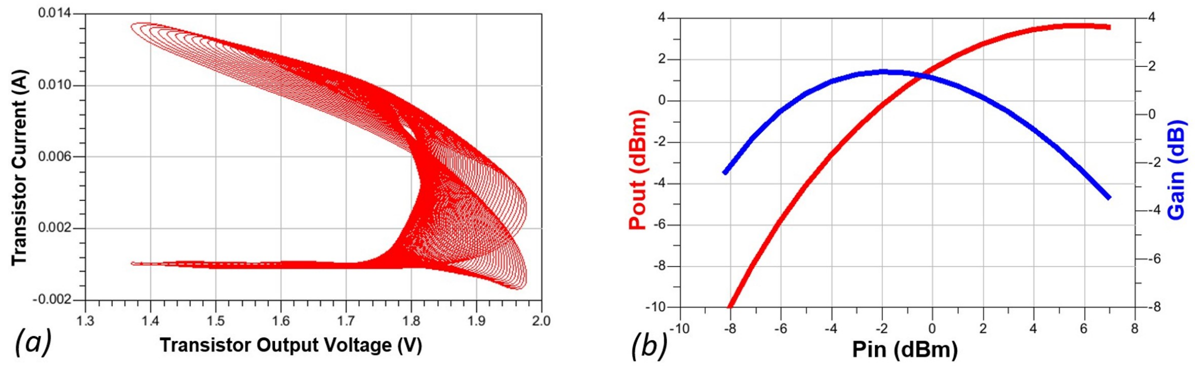


Figure 3.7: (a) Simulated loadline (I_c vs. V_{CE}) where P_{in} is swept from −12 dBm to 2 dBm. (b) Simulated P_{out} vs. P_{in} characteristics of the 140 to 280 GHz frequency doubler. The transistor current displayed in the loadline includes only the collector electron transport current and not the $C_{cb}dV_{cb}/dt$ displacement current associated with the collector-base capacitance.

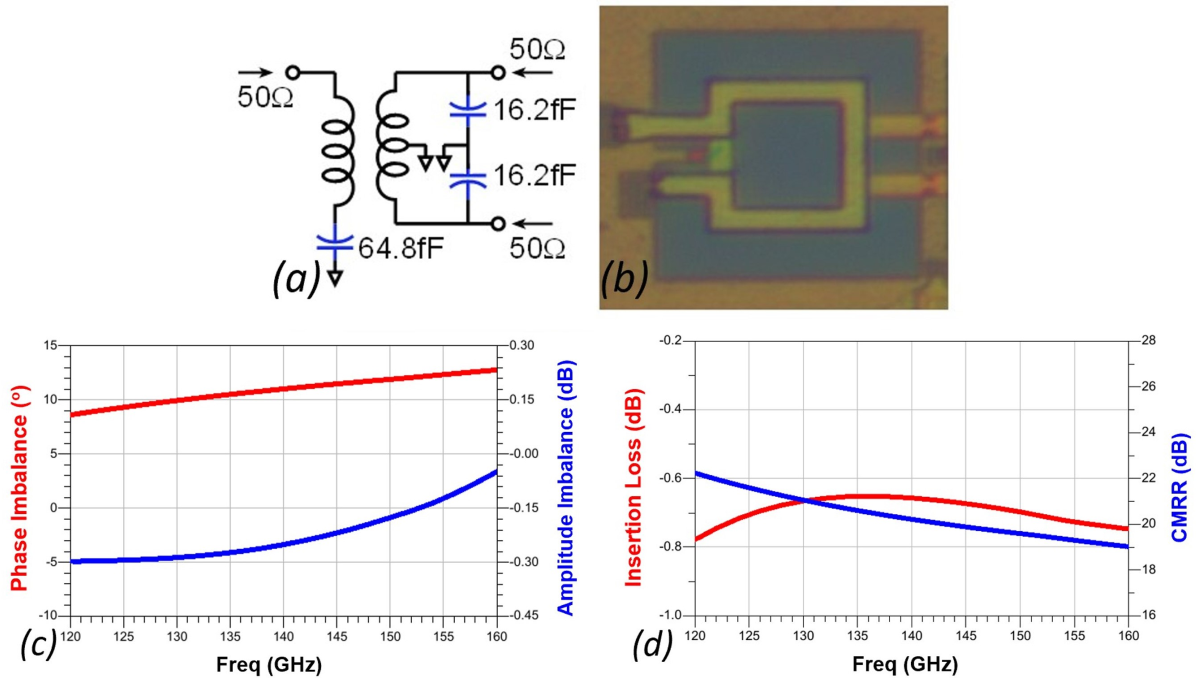


Figure 3.8: 140 GHz transformer balun (a) schematic, (b) die photograph, (c) simulated phase and amplitude imbalance, and (d) simulated insertion loss and CMRR.

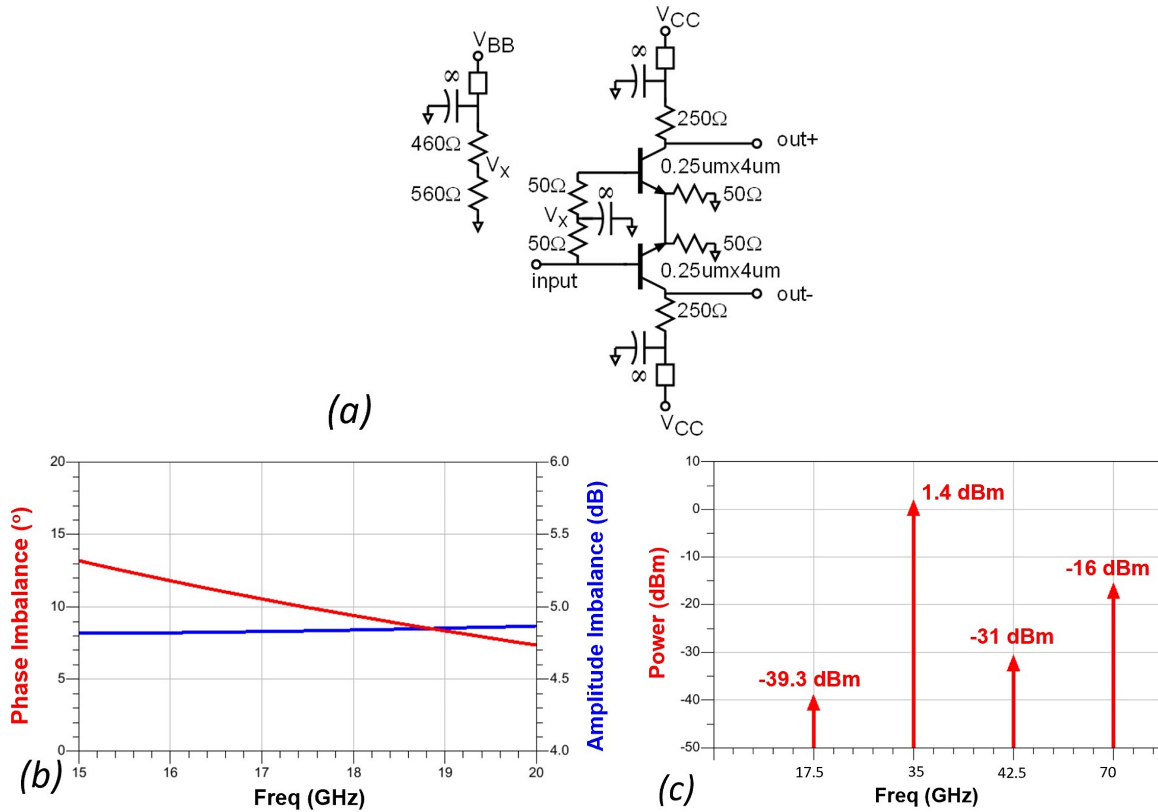


Figure 3.9: Active balun (a) schematic and (b) simulated phase and amplitude imbalance. (c) The simulated output spectrum of the 1st doubler stage integrated with the active balun, with $P_{\text{in}} = -13\,\text{dBm}$.

3.2.3 Single-ended to Differential Conversion

Except for the first doubler in the 16:1 multiplier chain, all frequency doublers generate differential input signals using 1:1 passive transformers, as depicted in Figure 3.8. These transformers are implemented with the top two metal layers to minimize loss (Fig. 3.8b). The dimensions of the transformer lines and the three capacitors are adjusted so that the transformer input impedance is 50 Ω when both output ports are loaded with 50 Ω. The 140 GHz transformer exhibits a simulated phase imbalance of 8.5-12.8° and an amplitude imbalance of 0.1-0.3 dB from 120 to 160 GHz, as shown in Figure 3.8c. At 140 GHz, the simulated insertion loss is 0.6 dB, and the CMRR is 20.2 dB (Fig. 3.8d).

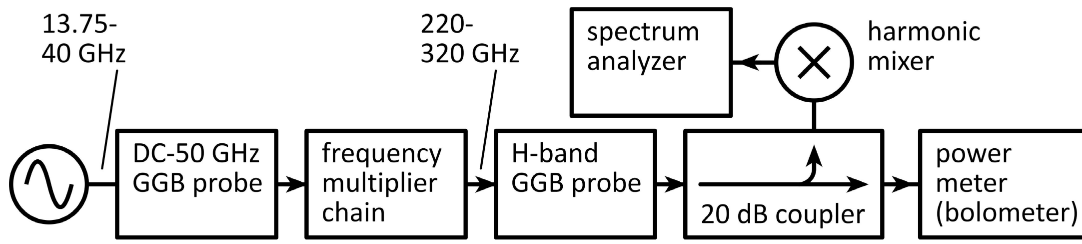


Figure 3.10: Experimental setup for characterizing the frequency doubler.

The first doubler in the 16:1 multiplier chain utilizes a transistor differential pair to convert single-ended input into a differential signal (Fig. 3.9a). The simulated phase imbalance ranges from 7.3-13.1°, while due to the small emitter resistive loading, the amplitude imbalance is subpar at 4.7-4.8 dB from 15 to 20 GHz (Fig. 3.9b). Despite the poor amplitude imbalance, simulations (Fig. 3.9c) demonstrate suppression of adjacent odd-order spurious harmonics by over 32 dBc. The 4th harmonic is suppressed by 17.4 dBc.

3.3 Measurement Results

Figure 3.10 illustrates the measurement setup. The output power spectrum is monitored using a 20 dB *WR*-3 band directional coupler, followed by a *WR*-3 band harmonic mixer (Oleson M03HWD), and a spectrum analyzer (Keysight N9030B). The power at the through port of the 20-dB coupler is monitored using an Erickson PM4 power meter. Before characterizing the frequency multiplier chains using this setup, calibration is performed on the harmonic mixer and spectrum analyzer. This is done by driving the input to the directional coupler with a swept-frequency tone ranging from 220 to 330 GHz from the 8:1 frequency multiplier chain. The power meter measurements and the spectrum analyzer's measurement of the 8th harmonic are then compared. As the spurious harmonics from the multiplier chain are suppressed by more than 25 dBc, over 99% of the power

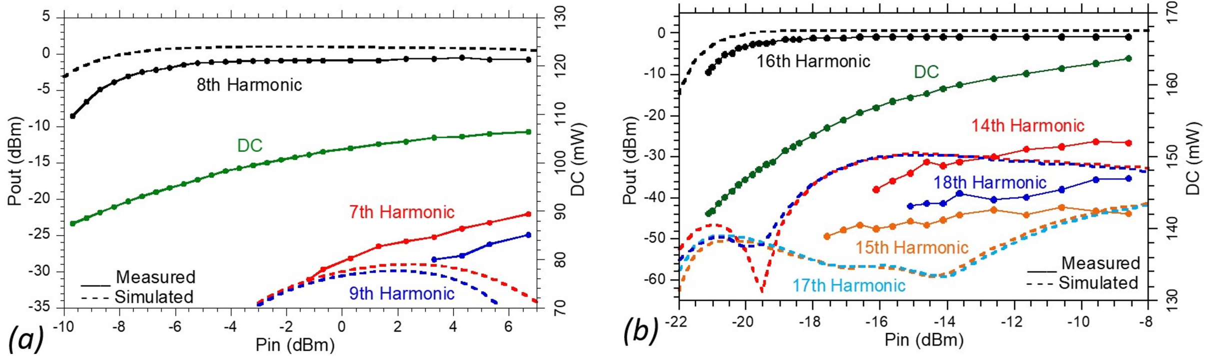


Figure 3.11: Measured P_{out} vs. P_{in} for the desired and spurious harmonics for the (a) 8:1 multiplier with a 35 GHz input and the (b) 16:1 multiplier with a 17.5 GHz input.

measured by the power meter is in the 8$^{\text{th}}$ harmonic. Therefore, the spurious harmonics have a negligible effect on the calibration accuracy. During subsequent characterization of the 8:1 and 16:1 multiplier chains, the spurious harmonic power is measured using the harmonic mixer and spectrum analyzer. However, the mixer's high noise figure, resulting from high-order harmonic mixing, limits the minimum detectable signal power of the spurious harmonics.

The 8:1 frequency multiplier was biased using DC probes with the following values: $V_{\text{CCx8}} = 2.9\,\text{V}$, $V_{\text{BBx8}} = 1.9\,\text{V}$, $I_{\text{CCx8}} = 29.8\,\text{mA}$, and $I_{\text{BBx8}} = 1.2\,\text{mA}$. At 280 GHz, when an input power of $-2\,\text{dBm}$ is applied, the 8:1 multiplier produces an output power of $-0.6\,\text{dBm}$. At this input power level, both the 7$^{\text{th}}$ and 9$^{\text{th}}$ harmonics are below the instrumentation noise floor (Fig. 3.11a). By increasing the input power to $-1.2\,\text{dBm}$, the power of the 7$^{\text{th}}$ rises above the instrument noise level to $-31\,\text{dBm}$. However, it requires further increase in input power to 3.3 dBm for the 9$^{\text{th}}$ harmonic power to be observable above the instrument noise, measuring at $-28.3\,\text{dBm}$. The total DC power consumption is 102 mW when applying an input power of $-2\,\text{dBm}$ (Fig. 3.11a). The core die area is $0.4\,\text{mm}^2$, as depicted in Figure 3.2a.

The 16:1 frequency multiplier was biased using DC probes with the following values: $V_{\text{CCx16}} = 2.9\,\text{V}$, $V_{\text{BBx16}} = 1.9\,\text{V}$, $I_{\text{CCx16}} = 45.1\,\text{mA}$, and $I_{\text{BBx16}} = 3.6\,\text{mA}$. At 280 GHz,

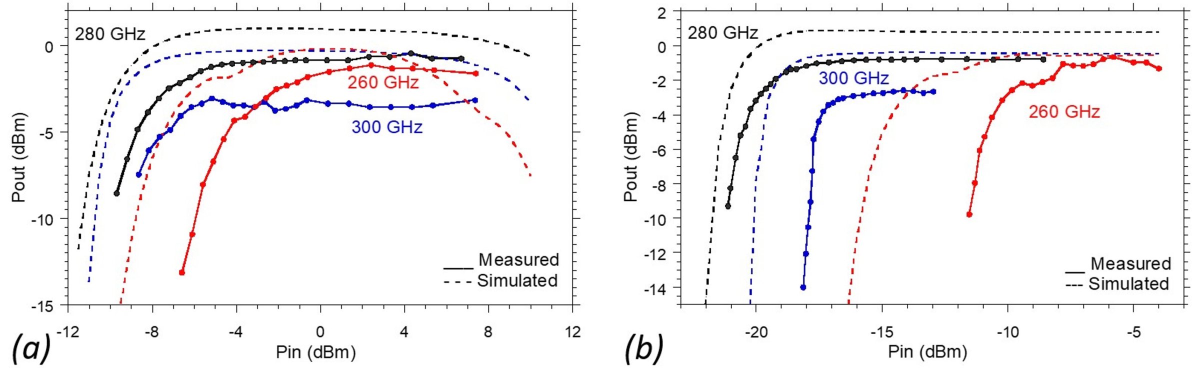


Figure 3.12: Measured P_{out} vs P_{in} at 260 GHz, 280 GHz, and 300 GHz for (a) the 8:1 multiplier and (b) the 16:1 multiplier.

when an input power of −18 dBm is applied, the 16:1 multiplier generates an output power of −1.1 dBm. At this input power level, the spurious harmonics are below the noise floor of the instrumentation (Fig. 3.11b). By increasing the input power to −16.1 dBm, the 15$^{\text{th}}$ harmonic becomes observable above the instrumentation noise, measuring at −47.4 dBm. Further increasing the input power to −14.6 dBm allows the 14$^{\text{th}}$ harmonic to be observed above the instrument noise, measuring at −31.2 dBm. Finally, increasing the input power to −13.6 dBm enables the 18$^{\text{th}}$ harmonic to be observed above the instrument noise, measuring at −38.7 dBm. The total DC power consumption is 162 mW when applying an input power of −13 dBm (Fig. 3.11b). The core die area is 0.75 mm^2, as depicted in Figure 3.2c.

Figure 3.12 displays the output power, specifically at the desired harmonic, as a function of input power, with the input frequency tuned to generate outputs at 260 GHz, 280 GHz, and 300 GHz. In the case of the 8:1 multiplier operating at a 280 GHz output (Fig. 3.12a), the measured 8$^{\text{th}}$ harmonic power is −0.8 dBm with an input power of 0 dBm, which is 1.7 dB lower than the simulated value. Similarly, for the 8:1 multiplier operating at a 300 GHz output, the measured 8$^{\text{th}}$ harmonic power is −3.3 dBm with 0 dBm input power, showing a discrepancy of 3 dB compared to the simulated value.

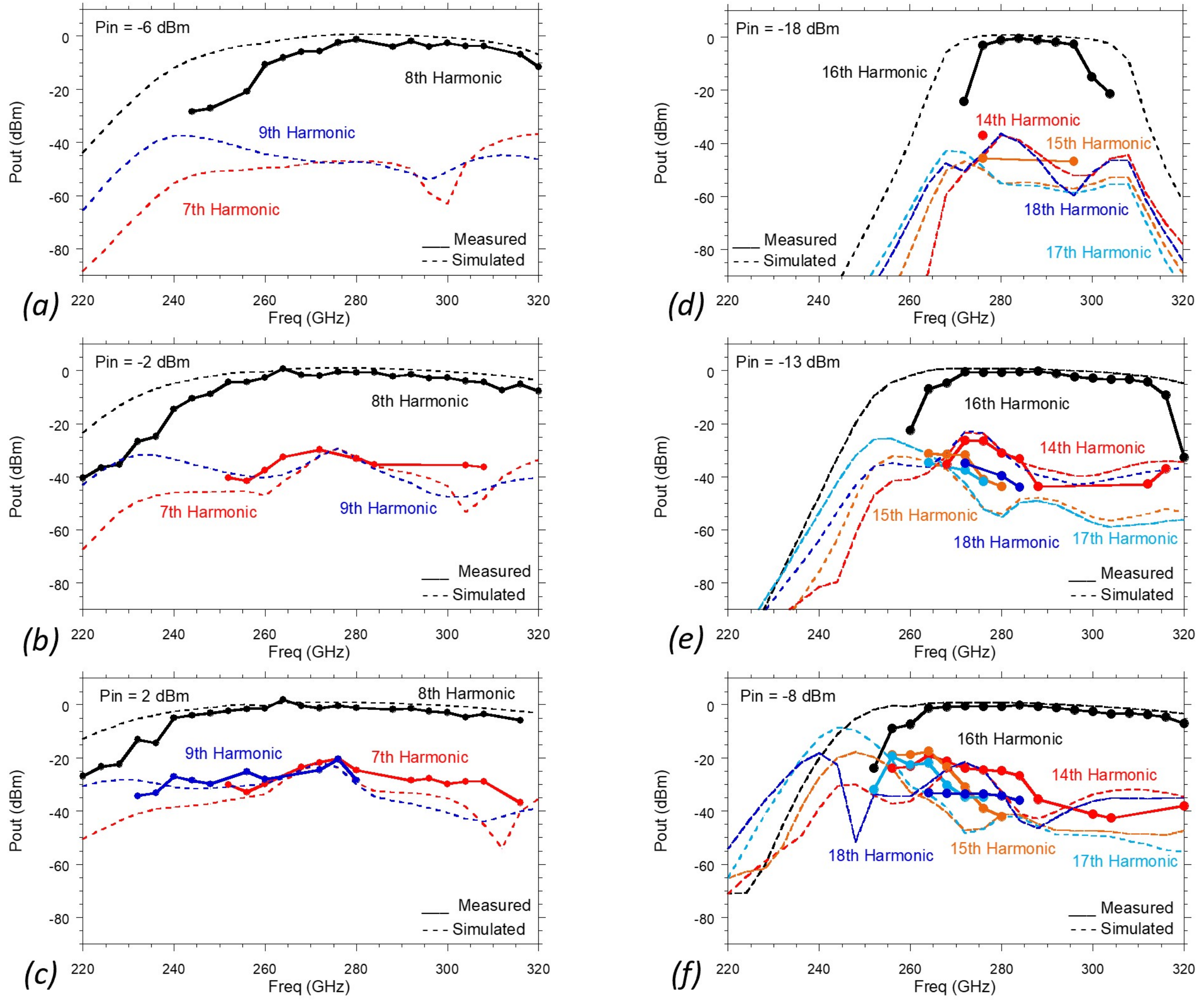


Figure 3.13: Measured and simulated output power at the 7th, 8th, and 9th harmonics of the input frequency, for the 8:1 frequency multiplier chain, at (a) −6 dBm, (b) −2 dBm, and (c) 2 dBm input power. Measured and simulated output power at the 14th through 18th harmonics of the input frequency, for the 16:1 frequency multiplier chain, at (d) −18 dBm, (e) −13 dBm, and (f) −8 dBm input power.

This inconsistency could be attributed to inaccurate large-signal transistor models at high frequencies [5]. Regarding the 16:1 multiplier operating at a 280 GHz output (Fig. 3.12b), the measured 16th harmonic power is −0.8 dBm with an input power of −13 dBm, which is 1.5 dB lower than the simulated value. Similarly, for the 16:1 multiplier operating at a 300 GHz output, the measured 16th harmonic power is −2.6 dBm with an input power of −13 dBm, indicating a deviation of 2.2 dB from the simulated value.

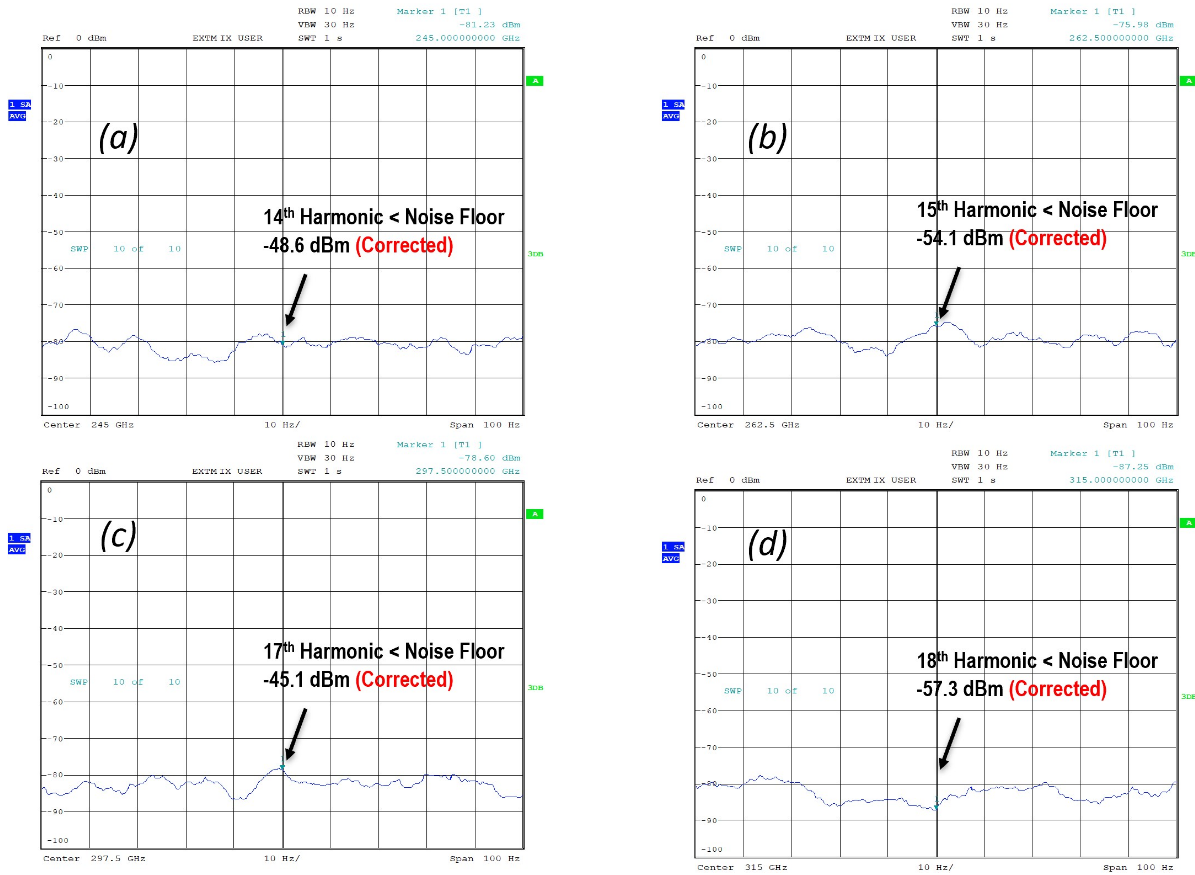


Figure 3.14: Output spectrum of the 16:1 frequency multiplier chain, as measured by the harmonic mixer and spectrum analyzer, given −18 dBm input power at 17.5 GHz. All spurious harmonics within the 220–330 GHz band are below the instrument noise.

Figures 3.13(a–c) depict the measured output power of the 8:1 frequency multiplier chain at the 7th, 8th, and 9th harmonics for input powers of −6 dBm, −2 dBm, and 2 dBm. With an input power of −2 dBm at 35 GHz, the measured 8th harmonic power is −0.6 dBm at 280 GHz. The 3-dB bandwidth is 48 GHz, and the spurious harmonics are suppressed by over 28 dBc within this bandwidth. When the input power is increased to 2 dBm, the 3-dB bandwidth expands to 60 GHz. However, the rejection of spurious harmonics decreases by 8 dB. The input power can be adjusted to achieve either high spectral purity or a wider operating bandwidth, depending on the specific requirements.

Figures 3.13(d–f) present the measured output power of the 16:1 frequency multiplier

Table 3.1: State-of-the-art *WR*-3 band frequency multipliers.

Reference†	**Technology**	**Mult.**	**Freq. (GHz)**	**3-dB BW (GHz)**	$P_{\mathbf{out}}$ **(dBm)**	$P_{\mathbf{DC}}$ **(mW)**	**HRR (dBc)**
[15]	CMOS 40 nm	x3	300	22	2.3	410	NA
[16]	CMOS 40 nm	x9	223	20	4.1	185	35
[17]	SiGe HBT 130 nm	x18	325	11	-3	162	NA
[18]	SiGe HBT 130 nm	x16	245	30	2.5	700	NA
[19]	SiGe HBT 55 nm	x2	245	40	5.5	238	NA
[20]	SiGe HBT 130 nm	x6	240	15	-4	900	14
[21]	SiGe HBT 130 nm	x4	284	39	2.5	384	NA
[22]	SiGe HBT 130 nm	x8	244.5	81	-7.7	240	28
[23]	SiGe HBT 130 nm	x8	300	127	2.3	537	16
[24]	SiGe HBT 130 nm	x4	252	48	5.5	270	20
[25]	SiGe HBT 130 nm	x8	270	50	-5	125	25
[26]	SiGe HBT 130 nm	x18	240	41	6.2	429	25
[27]	SiGe HBT 130 nm	x6	240	68	9	480	15
[28]	GaAs mHEMT 35 nm	x8	260	100	2.5	NA	10
[29]	InP HEMT 80 nm	x6	250	45	5	125	NA
This work[31]	**InP HBT 250 nm**	**x8**	**280**	**48**	**-0.6**	**102**	**28**
This work	**InP HBT 250 nm**	**x16**	**280**	**44**	**-0.6**	**162**	**26**

† Spec values for other works were extracted from their text or otherwise estimated from the plots.

chain at the 14th through 18th harmonics for input powers of −18 dBm, −13 dBm, and −8 dBm. With an input power of −18 dBm at 17.5 GHz, the 14th, 15th, 17th, and 18th harmonics are below the noise level of the instrumentation (Fig. 3.14). At an input power of −13 dBm and a frequency of 17.5 GHz, the measured power of the 16th harmonic is −0.6 dBm at 280 GHz. The 3-dB bandwidth is 44 GHz, and the spurious harmonics are suppressed by over 26 dBc within this bandwidth. Increasing the input power to −8 dBm, while maintaining the frequency at 17.5 GHz, results in an expanded 3-dB bandwidth of 52 GHz. However, the rejection of spurious harmonics decreases by approximately 10 dB. Thus, by adjusting the input power, a trade-off can be made between achieving a wider

operating bandwidth and maintaining a high rejection of spurious harmonics.

3.4 Summary and Conclusion

Table 3.1 compares the performance of the state-of-the-art *WR*-3 band frequency multipliers. To the authors' knowledge, this work demonstrates record spectral purity for frequency multipliers operating near 280 GHz. The 8:1 and 16:1 frequency multipliers can be integrated with a power amplifier [32] to be used as a high power source.

Chapter 4

280 GHz Tranceiver Design

4.1 Introduction

The frequency range of 200–300 GHz has the capability to support wireless backhaul links with capacities significantly surpassing 100 Gb/s, which would serve future communications networks. Various technologies have successfully demonstrated integrated receivers [33, 34, 35, 36, 37, 38, 39, 40, 41, 42] and transmitters [6, 35, 39, 40, 43, 44, 45, 46, 47, 48, 49, 50] operating around 280 GHz. When designing such transceivers, important objectives include achieving a low noise figure and high output power to extend the range of the link, as well as a high bandwidth to accommodate high symbol rates and, consequently, high data rates. This chapter will present a broadband single-channel receiver and transmitter that operates at 280 GHz, providing a detailed explanation of the transceiver architecture and its building blocks. Finally, continuous wave (CW) on-wafer measurement results will be shown.

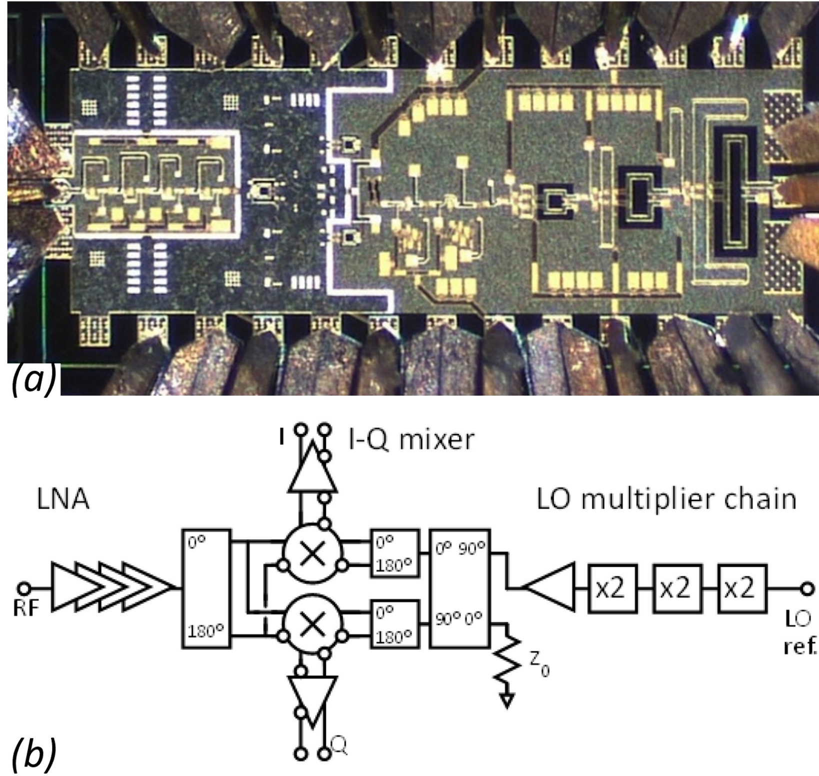


Figure 4.1: 280 GHz direct-conversion receiver: integrated circuit photograph (a), and block diagram (b). The IC is 2.0 mm × 0.8 mm.

4.2 Receiver Architecture and Buildings Blocks

The receiver consists of a broadband millimeter-wave low noise amplifier, followed by down-conversion mixers and broadband 50 Ω baseband output amplifiers for the in-phase (I) and quadrature-phase (Q) signals (Fig. 4.1). The mixers generate local oscillators using an 8:1 LO frequency multiplier, an LO buffer amplifier, and a passive LO quadrature phase generation circuit. In the LNA and frequency multiplier, IC interconnects utilize microstrip lines (MSLs) with the lowest metal plane (M1) serving as the ground. This configuration minimizes loss, resulting in the best LNA noise figure. For the mixer and baseband amplifiers, inverted microstrip lines (IMSLs) are used as interconnects, utilizing the upper metal plane (M4) as the ground. IMSLs eliminate the need for ground plane

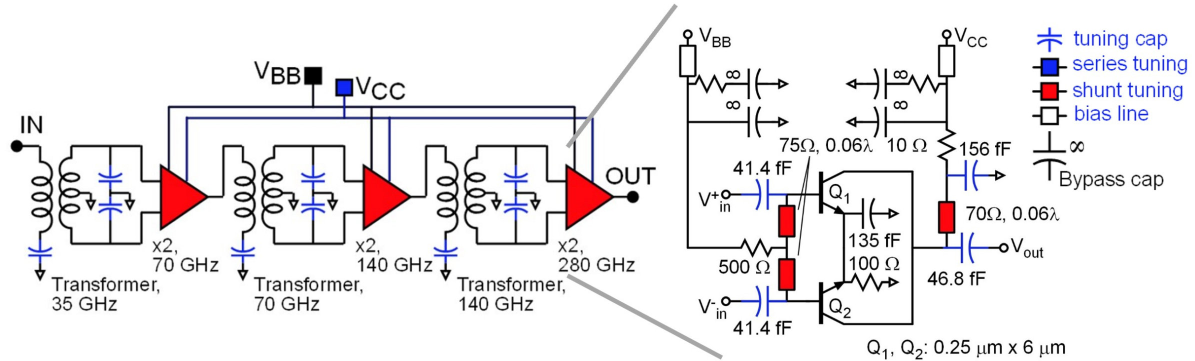


Figure 4.2: Circuit schematics of the LO multiplier (8:1).

holes for each transistor, reducing ground-return parasitics in dense circuits with multiple transistors, such as (I, Q) Gilbert-cell mixers. At 280 GHz, the loss for 50 Ω MSLs is 1 dB/mm, while IMSLs have a loss of 1.9 dB/mm. The simulated transition loss from MSL to IMSL is less than 0.15 dB.

4.2.1 LO Multiplier (8:1)

The 280 GHz LO is generated by employing three cascaded frequency doublers, as depicted in Figure 4.2. A detailed description of this multiplier chain can be found in Chapter 3, and [31]. Each balanced frequency doubler cell utilizes a push-push emitter-coupled pair. Additionally, the chain includes an input transformer balun. At 280 GHz, the measured power of the 8$^{\text{th}}$ harmonic is −0.6 dBm. The multiplier exhibits a 3-dB bandwidth of 48 GHz when the input power is −2 dBm. The adjacent harmonics are suppressed by more than 28 dBc. Considering the finite RF bandwidth of the LNA, other LO harmonics are not expected to cause significant spurious responses in the receiver.

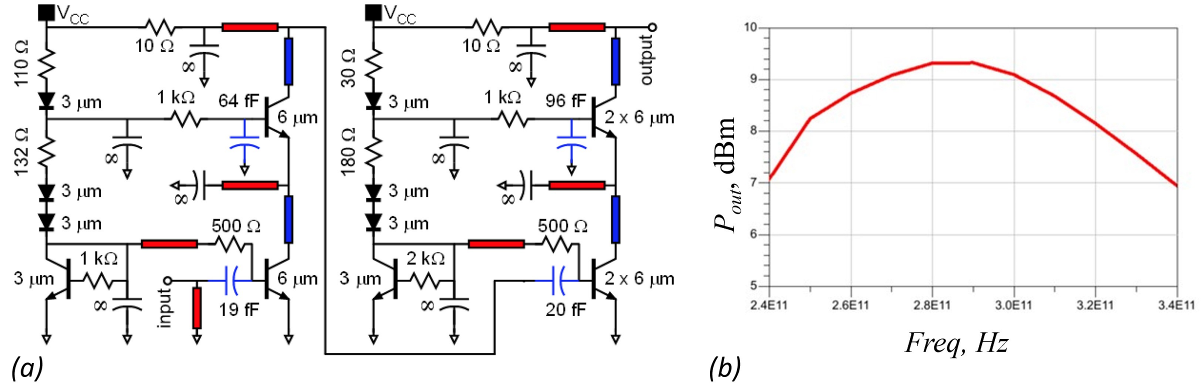


Figure 4.3: LO Driver: (a) circuit schematic, (b) simulated P_{out} vs frequency.

4.2.2 LO Driver

The driver amplifier is responsible for amplifying the LO power to the level required to drive the mixers. The DC bias circuit, illustrated in Figure 4.3a, consists of a pair of cascode stages. To achieve the highest output power and power-added efficiency (PAE), impedance tuning is implemented between the outputs of the common emitter (CE) transistors and the inputs of the common base (CB) transistors. Therefore, the LO buffer amplifier can be seen as a four-stage cascade (CE, CB, CE, CB). The inter-stage impedance tuning is optimized for maximum saturated output power, assuming an input power of 0 dBm, rather than maximum small-signal gain. The CE and CB transistors are individually stabilized using 500 Ω shunt resistors for the CE transistors and the finite base capacitance for the CB transistors. The finite base capacitance also facilitates significant cascade power-combining between the CB and CE stages [51, 52]. In simulation, with an input power of 0 dBm, the output power exceeds 7 dBm across the 240–340 GHz (Fig. 4.3b). The simulated DC power consumption is 160 mW.

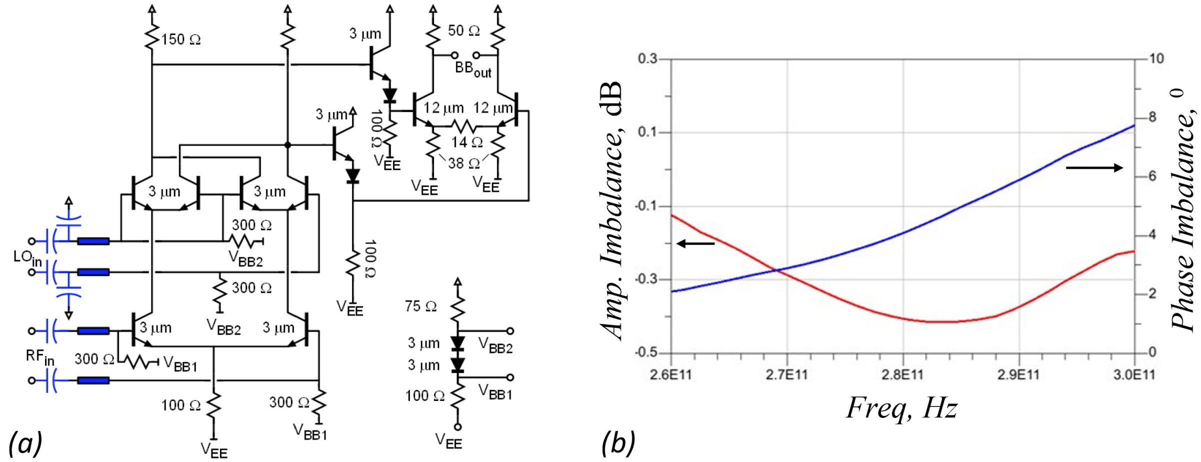


Figure 4.4: Down-conversion I-Q Mixer: (a) circuit schematic, (b) simulated amplitude and phase imbalance vs frequency.

4.2.3 Down-conversion I-Q Mixer and 50 Ω Baseband Driver

The output of the LO driver amplifier is connected to a Lange coupler, followed by a pair of transformer baluns. This configuration generates the four LO phases (0°, 90°, 180°, 270°) required for the I and Q mixers. Each mixer utilizes a double-balanced Gilbert configuration (Fig. 4.4a) and incorporates impedance matching on the LO and RF ports. However, there is no impedance matching between the input RF and LO switching transistors. By increasing the baseband load resistance from 50 Ω to 150 Ω, the noise contributions from the resistor itself and the output buffer are reduced. The differential output amplifiers employ emitter followers as level shifters and incorporate emitter degeneration to enhance linearity. They directly drive an external 50 Ω load. In simulation, the I-Q imbalance is less than 0.4 dB in amplitude and less than 7.8° in phase for output frequencies ranging from DC to 20 GHz (Fig. 4.4b). These results take into account the layout parasitics of the Lange coupler, LO/RF transformers, and baseband output amplifier drivers.

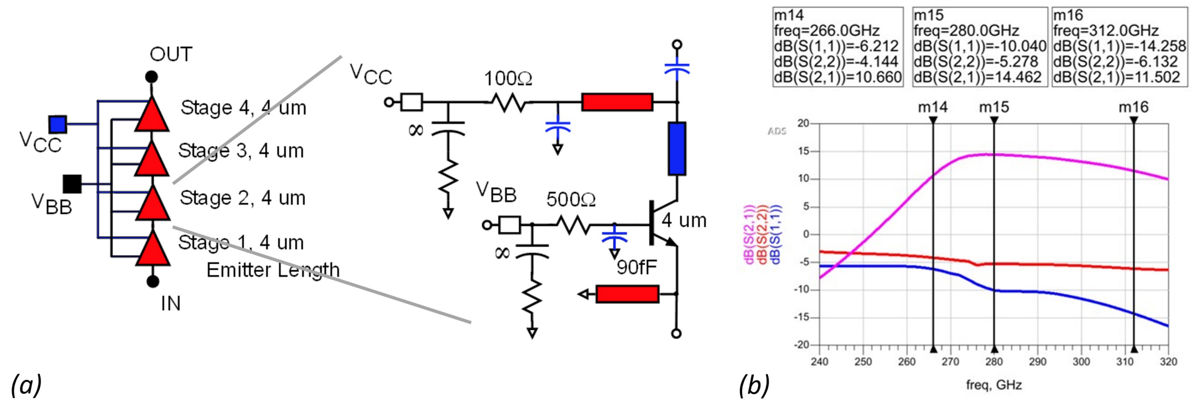


Figure 4.5: LNA: (a) circuit schematic, (b) simulated S-parameters.

4.2.4 LNA

The LNA (Fig. 4.5a) is a four-stage CB amplifier with base capacitive degeneration [14, 51, 52]. A detailed explanation of the LNA design procedure can be found in Chapter 2, and [14]. The base capacitance plays a crucial role in the LNA's performance. It ensures unconditional stability from DC to $f_{\max}$ and adjusts the source impedance to match the complex conjugate of the input impedance, allowing for simultaneous input matching for reflection coefficient and minimum cascaded noise figure. The scaling of the HBT junction area, along with the DC current and base capacitance, is carefully coordinated so that the source conductance for minimum noise measure is set to 20 mS. This enables the input stage to achieve noise matching to 50 Ω using a single inductive shunt element, eliminating the need for an additional series matching element that would introduce attenuation and additional noise [14]. The center frequencies of the four stages are stagger-tuned to provide a wider bandwidth.

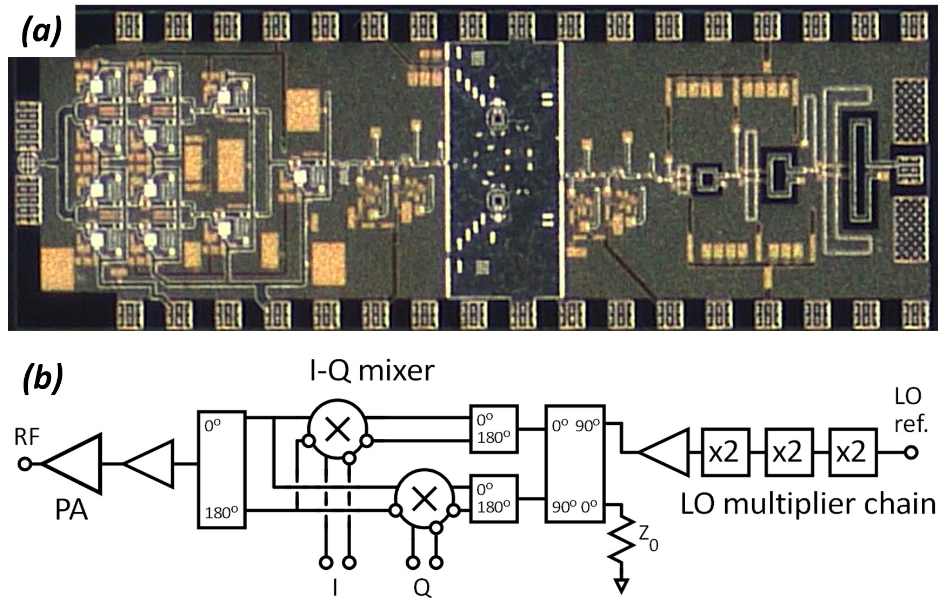


Figure 4.6: 280 GHz direct-conversion transmitter: integrated circuit photograph (a), and block diagram (b). The IC is 2.8 mm x 0.92 mm.

4.3 Transmitter Architecture and Buildings Blocks

The transmitter consists of a broadband millimeter-wave power amplifier (PA), which is preceded by a PA buffer amplifier and up-conversion mixers for the in-phase (I) and quadrature-phase (Q) signals (Fig. 4.6). The local oscillators for the mixers are generated using an 8:1 LO frequency multiplier, an LO buffer amplifier, and a passive LO quadrature phase generation circuit, similar to the LO generation network in the receiver. In the PA, buffer amplifiers, and frequency multiplier, the IC interconnects utilize microstrip lines (MSLs) with the lowest metal plane (M1) serving as the ground. This configuration minimizes loss, resulting in the best power-added efficiency (PAE) for the PA. For the mixers, the interconnects are inverted microstrip lines (IMSLs) using the upper metal plane (M4) as the ground. The same LO buffer amplifier is employed as a PA buffer amplifier, responsible for amplifying the output power of the up-conversion mixers to the level required to drive the PA.

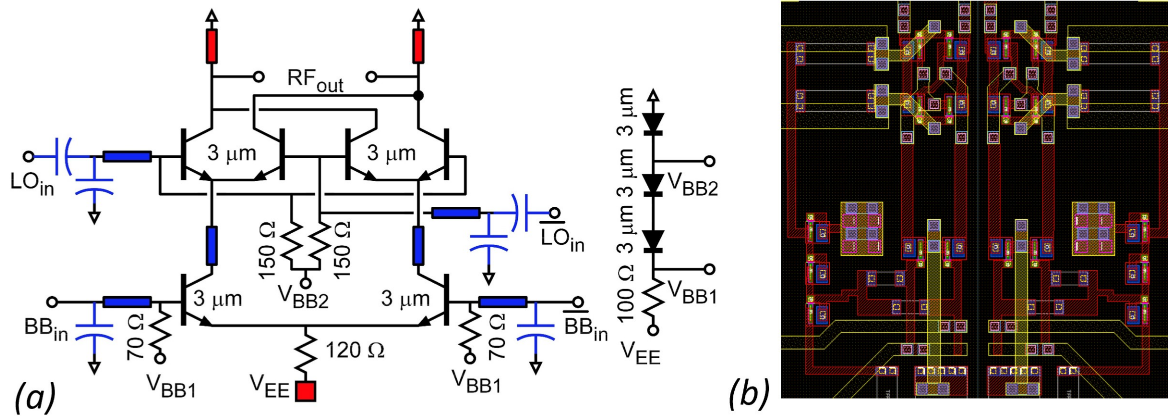


Figure 4.7: Up-conversion I-Q Mixer: (a) circuit schematic, (b) layout.

4.3.1 Up-conversion I-Q Mixer

The LO driver amplifier output is directed towards a Lange coupler and a pair of transformer baluns, which generate the four LO phases (0°, 90°, 180°, 270°) required for the I and Q mixers. Each mixer employs a double-balanced Gilbert configuration (Fig. 4.7a) and incorporates impedance matching on the LO and RF ports, as well as impedance matching between the input baseband (BB) and LO switching transistors. The signal bandwidth on the baseband inputs is enhanced by series L and shunt C tuning networks. The I-Q mixers utilize output inductive shunt tuning, employing short-circuited transmission line sections. It is important to consider that at 280 GHz, imbalances in the interconnect length within the (I, Q) Gilbert cell mixer core can result in amplitude or phase discrepancies between the I and Q channels. Even a short interconnect length of 5-10 μm can introduce a 2-4° phase delay at 280 GHz. Consequently, the transistor and interconnect spacings within the mixer core are designed to comply with the minimum specifications outlined by the process design rules, and the layout is optimized to minimize asymmetry between the I and Q paths (Fig. 4.7b).

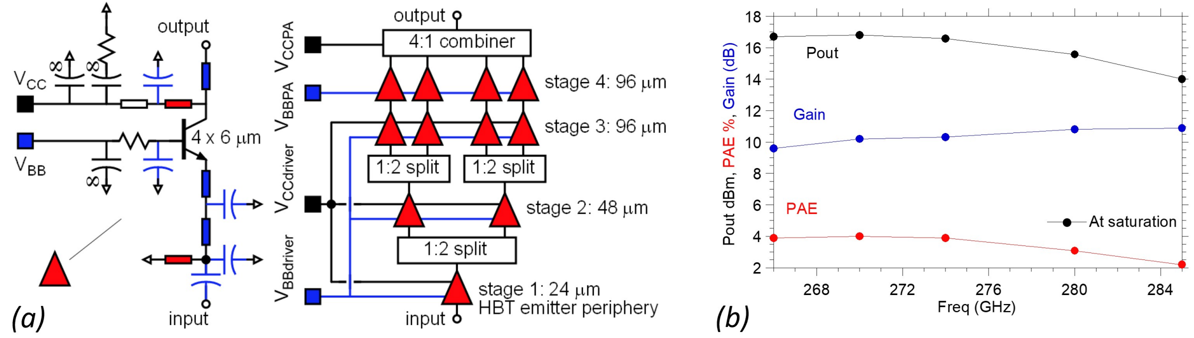


Figure 4.8: PA: (a) circuit schematic, (b) measured P_{out}, PAE and Gain vs frequency (*designed by Dr. Ahmed Ahmed*).

4.3.2 PA

The PA utilizes four capacitively linearized CB stages, which have been specifically designed for high efficiency and a compact layout (Fig. 4.8a). This PA design, previously reported in [32], demonstrates superior efficiency compared to CE or grounded CB configurations at 1 dB gain compression [52]. Four power cells, each with a 96 μm HBT periphery, are combined using a compact and low-loss 4:1 transmission line network. Shunt inductive lines are employed to tune the collector-base capacitances of the transistors. Similar to transistor stacking, the capacitively linearized common-base stages exhibit significant cascade power-combining [51], with approximately 40% of the output power contributed by stages 1-3. The measured saturated power of the reported PA [32] is 16.8 dBm at 270 GHz, achieving over 4% power-added efficiency (PAE) while dissipating 1.09 W. In the version of the PA integrated into the transmitter, the shunt inductive transmission lines used to tune the HBT output capacitances have been adjusted, specifically made shorter, to maximize the saturated output power at 280 GHz.

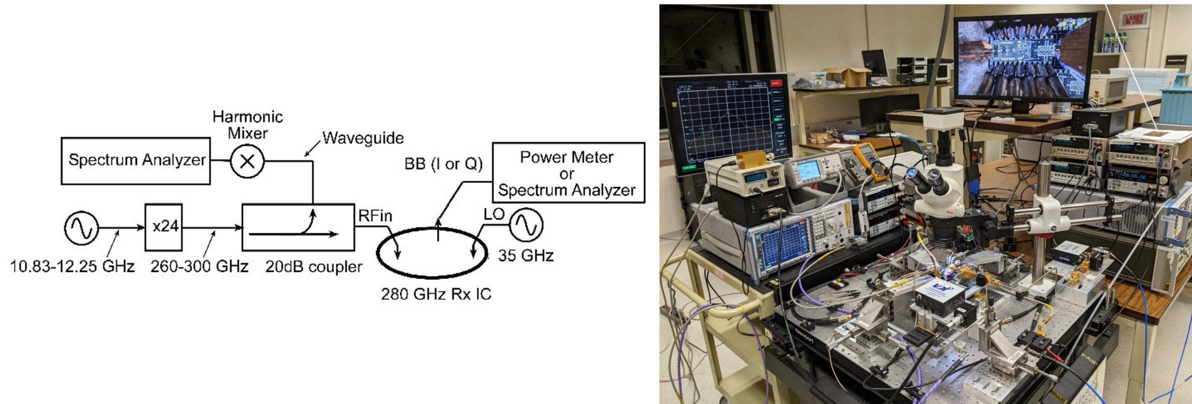


Figure 4.9: Receiver continuous wave (CW) testing setup.

4.4 Measurement Results

4.4.1 Receiver IC CW Characterization

Measurements (Fig. 4.9) were conducted on a 3 mil thinned die (Fig. 4.1a). An input signal was generated using a synthesizer and cascaded 12:1 and 2:1 VDI frequency multipliers. The signal passed through a directional coupler and a 220—330 GHz GGB wafer probe. The coupler's −20 dB port was connected to a harmonic mixer and a spectrum analyzer to monitor the input power. Before testing the IC, the input power monitor was calibrated against a VDI/Erickson THz power meter. The receiver output power was measured using a power meter, and its spectrum was monitored by a spectrum analyzer. The measurements have been adjusted to account for the input probe loss, using the loss value provided on the probe data sheet.

During operation, the 8:1 multiplier was biased with $V_{\mathrm{CC}} = 2.9$ V and $V_{\mathrm{BB}} = 1.9$ V, drawing 29.8 mA and 1.2 mA, respectively. The 4-stage LNA was biased with $V_{\mathrm{CC}} = 1.6$ V and $V_{\mathrm{BB}} = 0.85$ V, drawing 11 mA and 0.51 mA, respectively. The LO driver was biased with $V_{\mathrm{CC}} = 4.7$ V, and drew 31 mA from this supply. The mixers and output buffers drew 81 mA from $V_{\mathrm{EE}} = -2.5$ V.

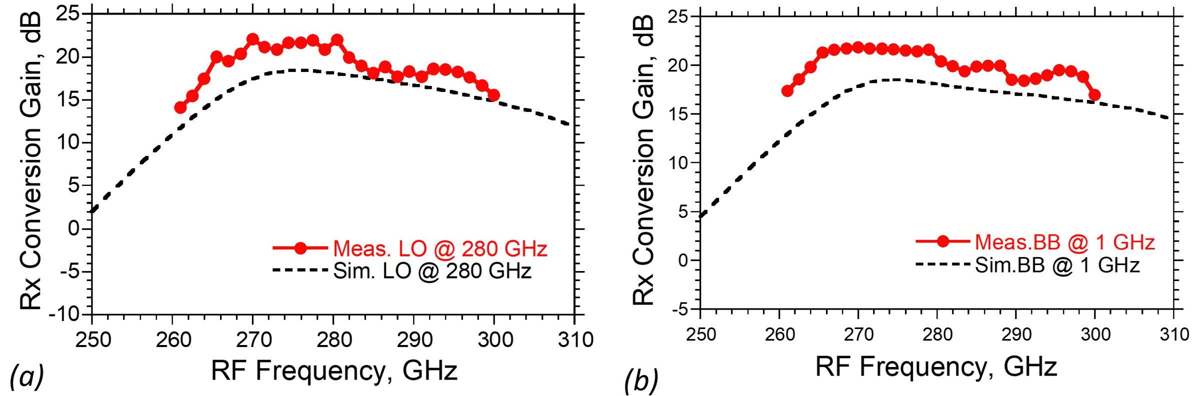


Figure 4.10: Conversion gain vs. RF frequency: (a) at a fixed 280 GHz LO frequency, (b) at a fixed 1 GHz output frequency.

The RF input frequency, was initially varied while maintaining a fixed LO frequency of 280 GHz (Fig. 4.10a). The measured conversion gain, to a single-ended output, reached a peak value of 22 dB. If the differential outputs were used, the gains would be 3 dB higher. Between 260 GHz and 280 GHz, the measured gain was approximately 2-4 dB higher than the simulated gain, while between 280 GHz and 300 GHz, it was about 1-2 dB higher. The measured 3-dB bandwidth was 16.5 GHz, and the measured 6-dB bandwidth was 34.5 GHz. It is common for CB amplifiers in this technology to exhibit higher gain than what is simulated [5].

Next, the RF and LO frequencies were swept while maintaining a fixed baseband frequency of 1 GHz (Fig. 4.10b). This resulted in a measured conversion gain of 20.4 dB at 280.5 GHz, with an LO-tuning bandwidth of approximately 40 GHz at the 6-dB points.

To assess the dynamic range, the input RF power was varied at 276 GHz while applying a 280 GHz local oscillator. The power level at which the gain drops by 1 dB (P_{in1dB}) was measured to be -23.6 dBm, dissipating 455 mW (Fig. 4.11).

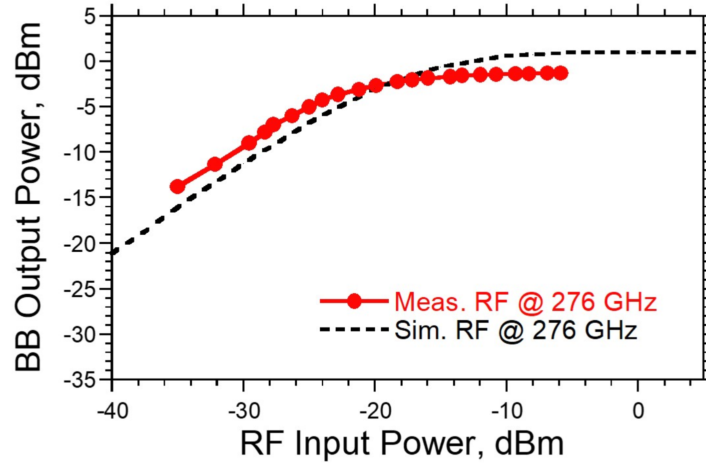


Figure 4.11: Baseband output power vs. RF input power at $f_{LO} = 280\,\text{GHz}$.

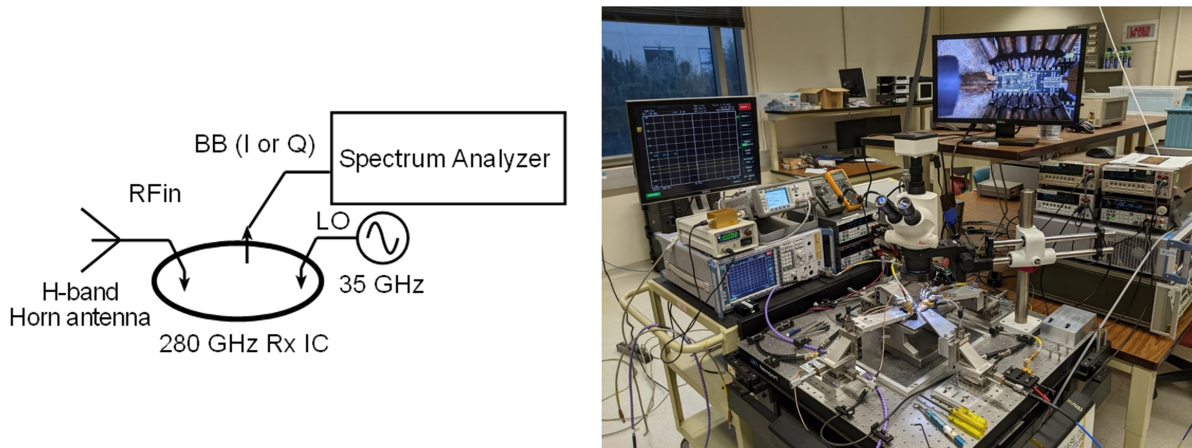


Figure 4.12: Receiver noise figure measurement by the gain method.

4.4.2 Receiver IC Noise Measurements

Due to the unavailability of a commercially accessible 280 GHz hot/cold noise source, the noise was measured using the less accurate gain method. Even with the hot/cold method, measurements can be challenging unless the temperature difference (T_{hot}–T_{cold}) is comparable to or greater than T_{DUT}. Initially, the receiver gain was measured using the configuration depicted in Figure 4.9, with input and output powers measured via power meters. Subsequently, the output noise power spectral density was measured at

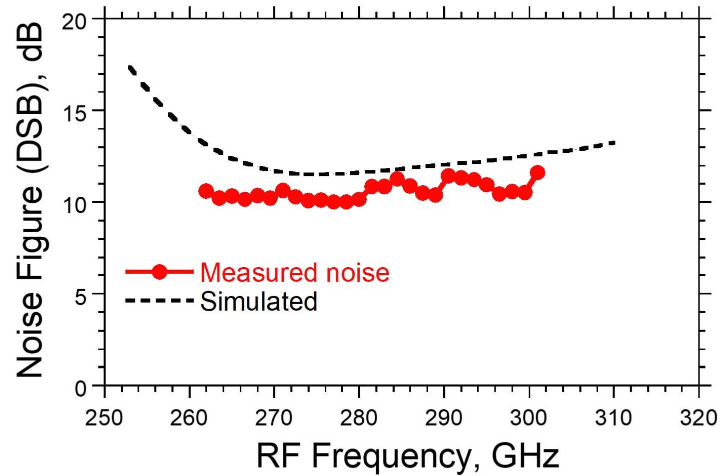


Figure 4.13: Measured vs simulated receiver DSB noise figure.

200 MHz using a spectrum analyzer (Fig. 4.12). The RF input was connected through a *WR*-3 band wafer probe to a *WR*-3 band horn antenna, providing a 50 Ω, 300 K source termination. The input-referred noise was determined by dividing the measured output noise by the measured receiver gain, then dividing by kT, and subtracting 3 dB to convert from single sideband (SSB) to double sideband (DSB) noise figure. The measured receiver DSB noise figure ranges from 10 to 11.6 dB over 261–300 GHz (Fig. 4.13). The measured noise level is approximately 1.5 to 2.5 dB lower than the original design simulations. However, over the 260–300 GHz range, the measured receiver gain is 1-4 dB higher than the simulated gain. If this difference between the measured and simulated receiver gain is attributable to a higher LNA gain than simulated, it would result in reduced contributions to the receiver noise from the mixer and the 2nd, 3rd and 4th LNA stages. A simple calculation reveals that the reduction in mixer noise alone would diminish the disparity between simulation and measurement to 1-1.5 dB, even without considering the reduced noise contributions of the 2nd-4th LNA stages. The measured DSB receiver noise (Fig. 4.13) closely resembles the noise of [53], which pertains to an LNA at the same frequency and in the same technology. It is also comparable to [54], which relates to an LNA in a

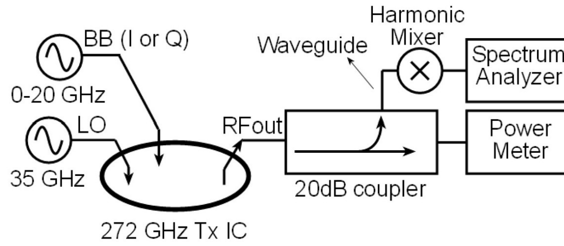


Figure 4.14: Transmitter continuous wave (CW) testing setup.

similar technology, although [53, 54] primarily present LNA results rather than receiver results.

We do not believe that an on-wafer 220–330 GHz receiver noise measurement, by the gain method, can be accurate to better than approximately ±1 dB.

4.4.3 Transmitter IC CW Characterization

Measurements were conducted on a 3 mil thinned die (Fig. 4.6a), as shown in Figure 4.14. Two synthesizers were used to generate the LO and BB input signals. The RF output signal was measured using a *WR*-3 band GGB wafer probe and a directional coupler. The −20 dB port of the coupler was connected to a harmonic mixer and a spectrum analyzer to monitor the output power. Prior to testing the IC, the output power monitor was calibrated against a VDI/Erickson THz power meter. The transmitter output power was measured using a power meter, and its spectrum was monitored by a spectrum analyzer. The measurements have been adjusted to account for the directional coupler and output probe losses, utilizing the losses provided in the datasheets.

In operation, the 8:1 multiplier was biased with $V_{\mathrm{CCx8}} = 2.9\,\mathrm{V}$ and $V_{\mathrm{BBx8}} = 2\,\mathrm{V}$,

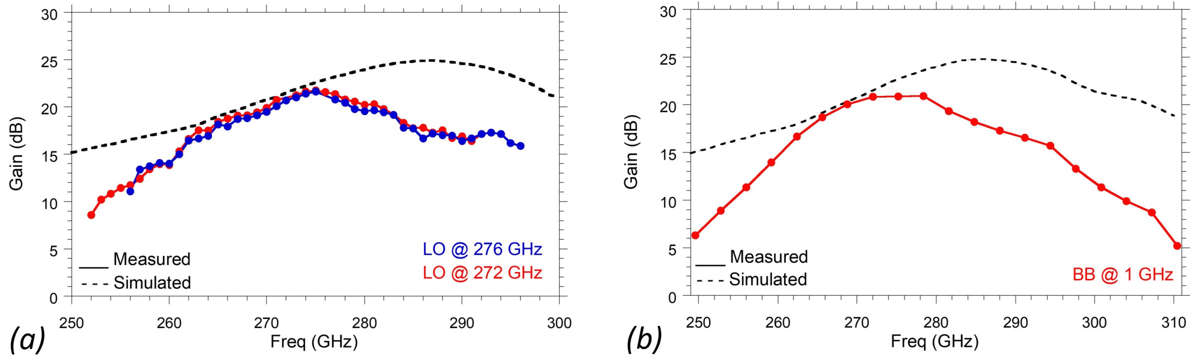


Figure 4.15: Conversion gain vs. RF frequency: (a) at a fixed LO (272, 276 GHz) frequency, (b) at a fixed 1 GHz input BB frequency.

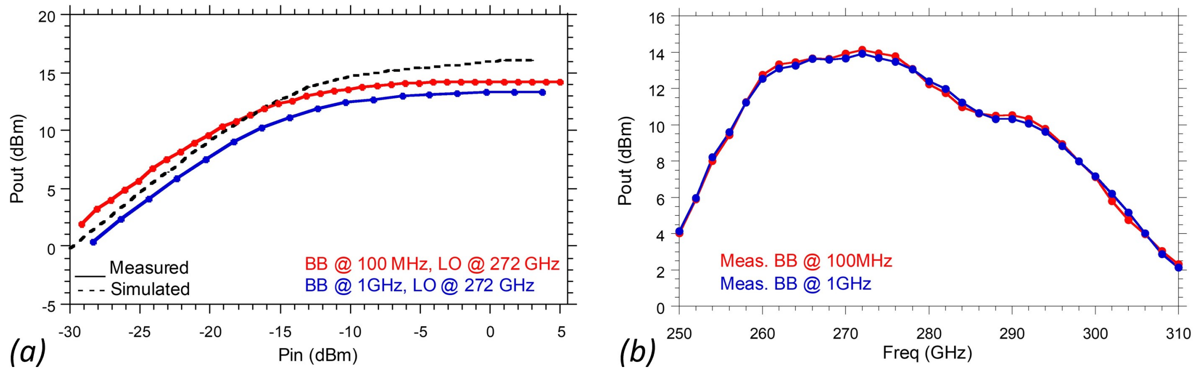


Figure 4.16: (a) RF output power vs. baseband input power, (b) saturated RF output power vs. RF frequency.

drawing 31 mA and 1.51 mA respectively. The 4-stage PA was biased with $V_{\mathrm{CCPA}} = 2.5\,\mathrm{V}$, $V_{\mathrm{CCdriver}} = 3.15\,\mathrm{V}$, $V_{\mathrm{BBPA}} = 2.3\,\mathrm{V}$ and $V_{\mathrm{BBdriver}} = 1.76\,\mathrm{V}$ drawing 155 mA, 179 mA, 9.5 mA and 10.6 mA respectively. The LO buffer amplifier was biased with $V_{\mathrm{CCBuffer}} = 5.2\,\mathrm{V}$, and drew 42 mA. The PA buffer amplifier was biased with $V_{\mathrm{CCBuffer}} = 5.2\,\mathrm{V}$, and drew 41 mA from this supply. The mixers drew 22 mA from $V_{\mathrm{EEMixer}} = -3.3\,\mathrm{V}$. The DC power dissipation is 1.6 W.

The input BB frequency was initially varied while maintaining fixed LO frequencies of 272 GHz and 276 GHz (Fig. 4.15a). The peak measured conversion gain was 21.7 dB, which is 3.2 dB lower than the simulated value. Additionally, the frequency at which

Table 4.1: State-of-the-art integrated receivers at and above 200 GHz.

Reference†	**Technology**	**Freq. (GHz)**	**Conv. Gain (dB)**	P_{DC} **(mW)**	**Chip Size (mm²)**	**DSB NF (dB)**
[33]	CMOS 65 nm	240	25	260	2	15
[34]	GaAs mHEMT 50 nm	220	1.5	NA	1.5	7.5
[35]	GaAs mHEMT 100 nm	220	3.5	110	4.8	7.4
[36]	SiGe HBT 130 nm	240	18	512	2.1	18
[37]	SiGe HBT 130 nm	240	32	575	4.5	10.4
[38]	SiGe HBT 130 nm	240	10.5	866	1.56	12
[39]	InP HBT 250 nm	200	25	825	2	8
[40]	InP HBT 250 nm	300	26	482	1.32	12-16.3
[41]	InP HBT 250 nm	340	14	472	3	17
This work[42]	**InP HBT 250 nm**	**280**	**22**	**455**	**1.6**	**10.8**

† Spec values for other works were extracted from their text or otherwise estimated from the plots.

the peak conversion gain occurred was 12 GHz lower than what was simulated. The measured 3-dB bandwidth was 18 GHz, while the measured 6-dB bandwidth was 36 GHz. Subsequently, the LO frequency was swept while keeping a fixed BB frequency of 1 GHz (Fig. 4.15b). This yielded a measured conversion gain of 20.8 dB at 272 GHz, with an LO tuning bandwidth of approximately 36 GHz at the 6-dB points. The breakout of the LO/PA buffer amplifier was characterized using a *WR*-3 band S-parameter on-wafer measurement setup. It was found that the LO/PA buffer amplifier has a 3-dB bandwidth that is 30% lower than what was simulated, and the frequency at which the peak gain occurs is shifted downward by 10 GHz. These deviations from the simulations become evident above 280 GHz.

To determine the transmitter's saturated output power and compression point, the input BB power at 1 GHz was varied while applying a 272 GHz LO. The measured values for P_{in1dB} and P_{out1dB} were -18.3 dBm and 8.9 dBm, respectively (Fig. 4.16a). The measured saturated output power was found to be 14.1 dBm at 272 GHz (Fig. 4.16b).

Table 4.2: State-of-the-art integrated transmitters at and above 200 GHz.

Reference†	**Technology**	**Freq. (GHz)**	$P_{\mathbf{sat}}$ **(dBm)**	$P_{\mathbf{DC}}$ **(mW)**	**Efficiency (%)**
[6]	CMOS SOI 32 nm	210	4.6	240	1.2
[43]	CMOS 65 nm	240	-0.5	220	1.2
[44]	CMOS 40 nm	265	-1.6	890	0.08
[45]	SiGe HBT 130 nm	220-255	5	960	0.33
[46]	SiGe HBT 130 nm	240	12	1237	1.28
[47]	SiGe HBT 130 nm	300	-4.1	300	0.13
[35]	GaAs mHEMT 100 nm	220	-6	110	0.23
[48]	GaAs mHEMT 50 nm	240	1	NA	NA
[49]	InP HEMT 80 nm	290	12	6600	0.24
[40]	InP HBT 250 nm	298	-2.3	452	0.13
[39]	InP HBT 250 nm	200	15.3	1250	2.71
This work[50]	**InP HBT 250 nm**	**272**	**14.1**	**1600**	**1.6**

† Spec values for other works were extracted from their text or otherwise estimated from the plots.

4.5 Summary and Conclusion

Table 4.1 presents a comparison of the performance of state-of-the-art integrated receivers operating at and above 200 GHz. According to the authors' knowledge, the work described in this study demonstrates a record noise figure for integrated receivers operating in the vicinity of 280 GHz.

Table 4.2 compares the results obtained in this study with previous findings for transmitter ICs operating at frequencies above 200 GHz. The integrated transmitter reported here sets a new record, across all technologies, for the output power of an integrated transmitter operating near 272 GHz.

Chapter 5

200 GHz Modules

5.1 Introduction

The advancements in silicon and III–V compounds have enabled the construction of high-frequency transceivers suitable for mm-wave applications, exhibiting excellent performance, reasonable power consumption, and compact size. However, it is worth noting that packaging technologies have not progressed at the same pace as semiconductor technologies. Consequently, mm-wave package designers face difficulties in obtaining a fully packaged solution without experiencing substantial chip-to-package transition losses under a reasonable price and turnaround time.

In this chapter, our focus will be on the 200 GHz module design and characterization, which utilize fully integrated InP direct-conversion Tx and Rx ICs, and corporate-fed patch antennas on a 50 μm fused silica (SiO_2) substrate. The performance of the InP ICs has already been documented in previous studies [[13, 14, 39]. We will provide brief information about the design of the 200 GHz ICs and antennas, including the measured performance results. Furthermore, we will showcase the design and assembly process of the modules and follow with the continuous wave over-the-air characterization of these

modules.

5.2 Module Design

Ball bonding is a widely accepted technology used in the construction of IC package transitions, where a thin wire made of gold, copper, or aluminum is connected from the chip pad to the printed circuit board (PCB). The ball bond can be represented as an inductance, although this inductance is generally considered insignificant at lower frequencies (below 5 GHz). However, for high-frequency applications, matching the impedance of the ball bond becomes more challenging, resulting in increased insertion loss. Recent efforts have demonstrated transition losses exceeding 2 dB in W-band ball bond transitions [55]. Similarly, in D-band applications, a CMOS transmitter was bonded to a low-cost PCB and integrated with a series-fed patch antenna through wirebond routing, resulting in a transition loss of 2.5 dB [56, 57]. This increased insertion loss at mm-wave frequencies and high parasitic inductance make wirebond transitions less suitable for mm-wave packaging.

Unlike ball bonds, wedge bonds do not involve the use of a ball. The absence of a ball in wedge bonding allows for significantly shorter wire bond lengths. Consequently, the wedge bond exhibits lower parasitic inductance compared to the ball bond, making it a more favorable choice for IC package transitions at mm-wave frequencies. In the design process of 200 GHz Tx and Rx modules, two critical principles are taken into consideration: designing for manufacturability and designing for shorter lead times. Wedge bonds adhere to industry standards with high packaging yield and can be provided with shorter turnaround times.

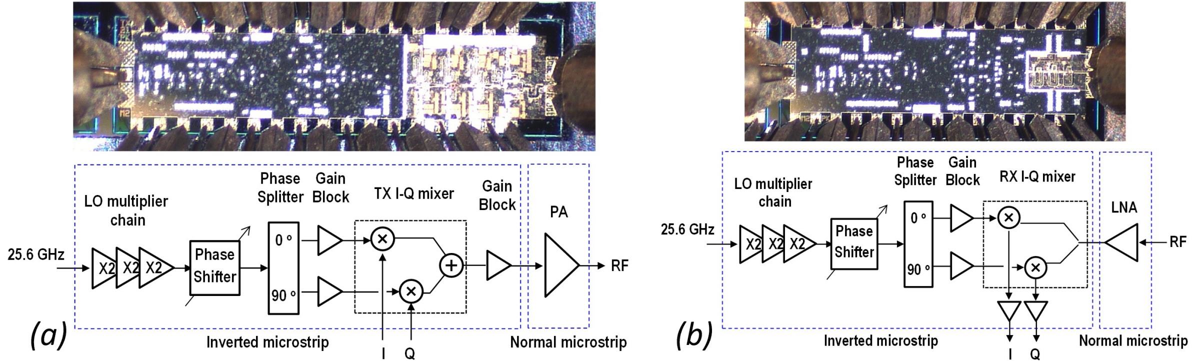


Figure 5.1: (a) A 200 GHz direct-conversion transmitter: chip photo (top) and block diagram (bottom). Chip size: $2.9\,mm \times 0.75\,mm$. (b) A 200 GHz direct-conversion receiver: chip photo (top) and block diagram (bottom). Chip size: $2.3\,mm \times 0.85\,mm$ (*designed by Prof. Munkyo Seo*).

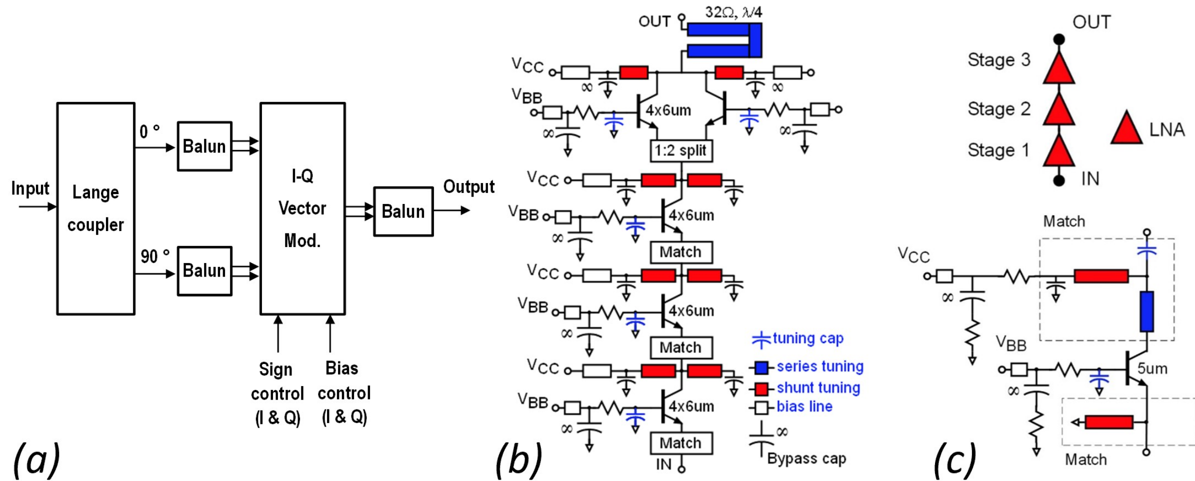


Figure 5.2: Circuit schematics: (a) phase shifter, (b) PA, (c) LNA.

5.2.1 200 GHz Transmitter and Receiver ICs

The 200 GHz transmitter consists of a LO multiplier (8:1), phase shifter, phase splitter, I-Q up-conversion mixer, and power amplifier (PA) (Fig. 5.1a). The 200 GHz receiver contains the same LO chain, I-Q down-conversion mixer, an input low noise amplifier (LNA), and 50 Ω output amplifiers for the differential (I-Q) outputs (Fig. 5.1b). The ICs were fabricated in 250 nm InP HBT technology [5]. Two types of transmission lines are utilized: inverted microstrip (IMSL) and normal microstrip lines (MSL). IMSLs are

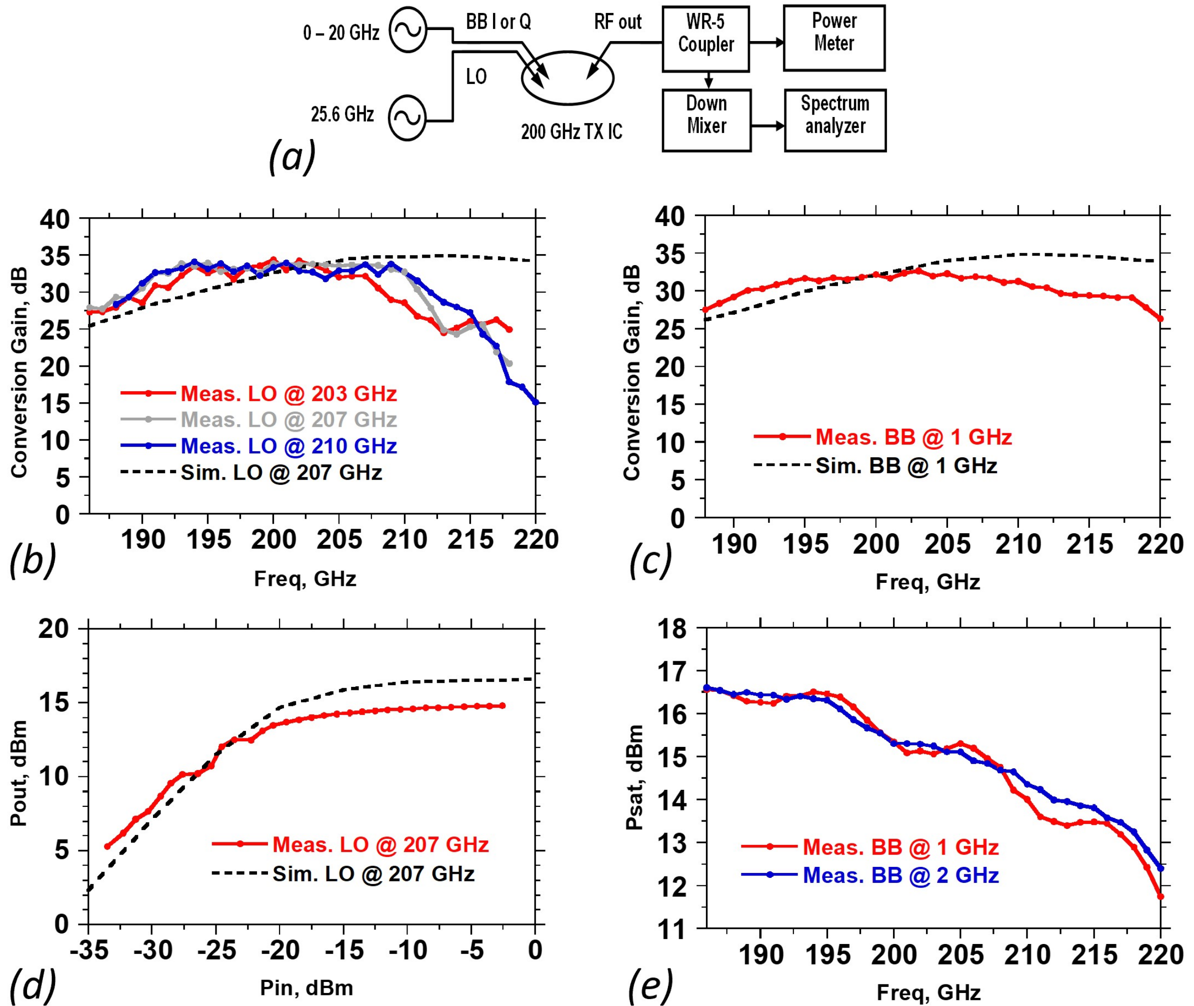


Figure 5.3: (a) On-wafer transmitter IC testing setup. Transmitter IC measurement results: (a) conversion gain vs. baseband frequency at a fixed LO, (c) conversion gain vs. LO frequency at a fixed baseband frequency, (d) RF output power vs. baseband input power at 1 GHz, (e) saturated RF power vs. RF frequency.

employed in the LO circuits, mixer, and gain block, where device density is relatively high. The top-metal layer (M4) ensures a continuous ground plane, regardless of device contacts at M1, thereby preventing performance degradation such as reduced bandwidth, gain, and cross-talk caused by ground plane holes. This design approach reduces uncertainty in layout electromagnetic (EM) modeling, although it incurs additional line loss of 2.5 dB/mm and 1.1 dB/mm at 200 GHz for IMSL and MSL, respectively. On the other

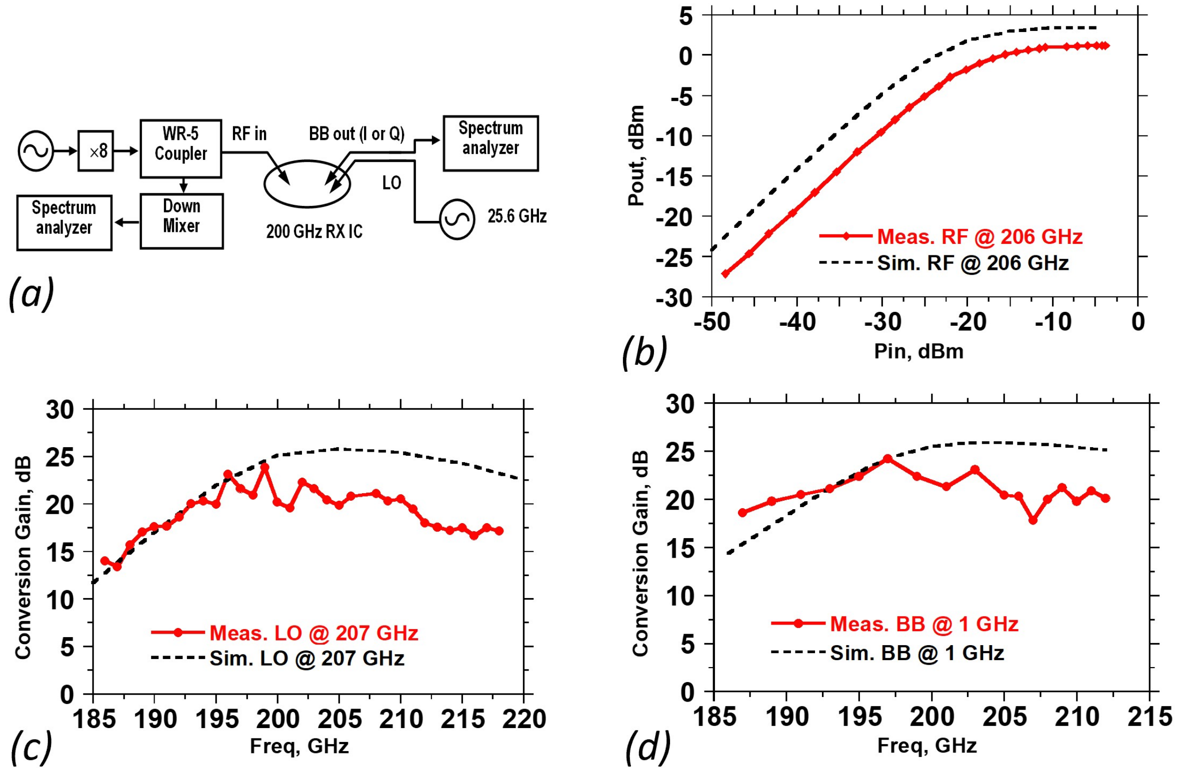


Figure 5.4: (a) On-wafer receiver IC testing setup. Receiver IC measurement results: (b) baseband output power vs. RF input power, LO is at 207 GHz, (c) conversion gain vs. RF frequency at a fixed LO, (d) conversion gain vs. RF frequency at a fixed baseband frequency.

hand, the PA and LNA are implemented using MSL to maximize PAE and minimize NF. The simulated loss of an IMSL-MSL transition is less than 0.1 dB. Figure 5.2 shows the circuit schematic of the phase shifter, PA and LNA.

The transmitter IC was measured using an on-wafer test setup depicted in Figure 5.3a. For simultaneous spectrum and power measurement, a *WR*-5 directional coupler was utilized. The baseband frequency was varied while keeping the LO frequency fixed. In Figure 5.3b, the measured peak conversion gain was 34 dB, with approximately 20 GHz of 3-dB bandwidth (only the I-channel was driven). The LO frequency was swept in conjunction with the baseband frequency set at 1 GHz. The measured conversion gain remained above 25 dB within the 190–220 GHz range (Fig. 5.3c). Figure 5.3d illustrates

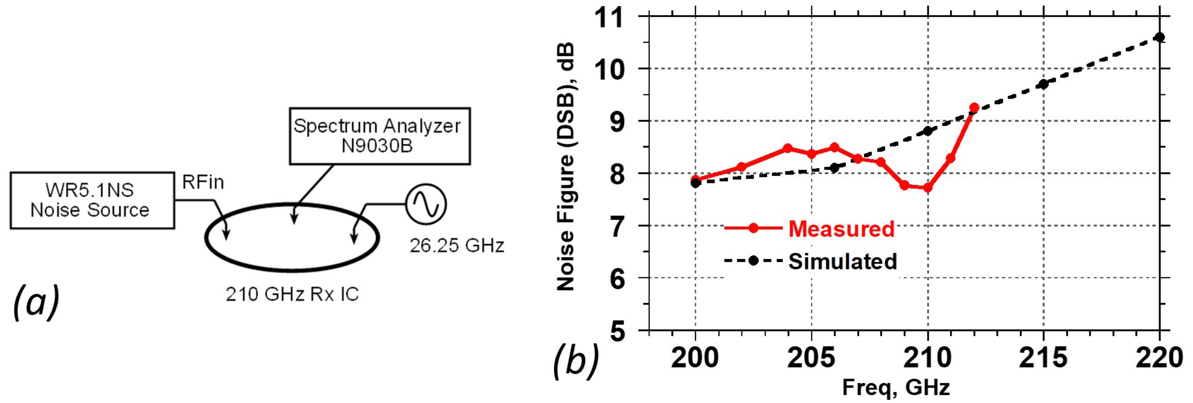


Figure 5.5: (a) Receiver IC noise testing setup. (b) Measured noise figure.

the variation of baseband input power at 1 GHz and the corresponding RF output power. At an RF frequency of 195 GHz, the measured saturated output power was 16.5 dBm, while at 200 GHz, it was 15.3 dBm (Fig. 5.3e). The transmitter IC's power consumption was 1,250 mW.

The receiver IC was measured using an on-wafer setup depicted in Figure 5.4a. The measured input power at 1 dB compression point (P_{in1dB}) for the receiver was −24 dBm (Fig. 5.4b), with a power dissipation of 825 mW. The peak conversion gain was 25 dB (Fig. 5.4c). The receiver IC exhibits a LO tuning bandwidth that exceeds 25 GHz (Fig. 5.4d). To determine the receiver noise figure, a VDI-WR5.1NS hot/cold noise source was connected to the receiver input (Fig. 5.5a). The measured noise figure ranged from 7.7 dB to 9.3 dB across the frequency range of 200–212 GHz (Fig. 5.5b). The receiver's output noise power spectral density was measured at 100 MHz using a low noise post-amplifier with approximately 20 dB gain, and a spectrum analyzer. During all the measurements conducted, the reference plane was set at the probe tip. The losses associated with components such as GGB probes, couplers, waveguides, cables, etc., were de-embedded.

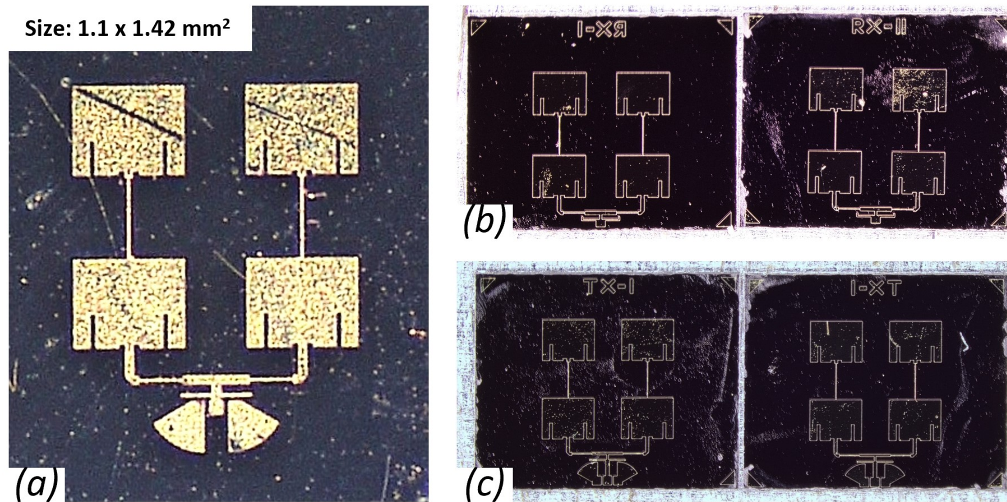


Figure 5.6: (a) A photograph of the 50 Ω matched corporate-fed 2×2 series patch antenna array on 2 mil fused silica substrate. Tuned antennas for (b) receiver module, (c) transmitter module (*designed by Dr. Amirreza Alizadeh, and fabricated by UCSB cleanroom*).

5.2.2 200 GHz Antennas

The mm-wave on-chip antennas have been extensively reported [58, 59, 60]. The main concern associated with on-chip antennas is the high dielectric constants (ϵ_r) found in III–V and Silicon substrates. Because of the high ϵ_r, most of the field is confined within the substrate, leading to poor radiation efficiency and gain. As an alternative solution, antennas on the package or LTCC offer higher radiation efficiency due to the lower ϵ_r of organic substrates [56, 61]. However, they tend to be more expensive and require longer turnaround times.

A single patch antenna achieves a theoretical gain of approximately 6 dB. In order to enhance the gain and focus the beam, we have implemented a 2×2 array of slotted patch antennas, as shown in Figure 5.6. As our initial objective is to test the design before integrating it into the module, the input port of the antenna array is matched to 50 Ω. Additionally, two $\lambda/4$ radial stubs have been placed near the signal pad at the input for on-wafer probing (Fig. 5.6a). This enables us to land GSG probes to the antenna array

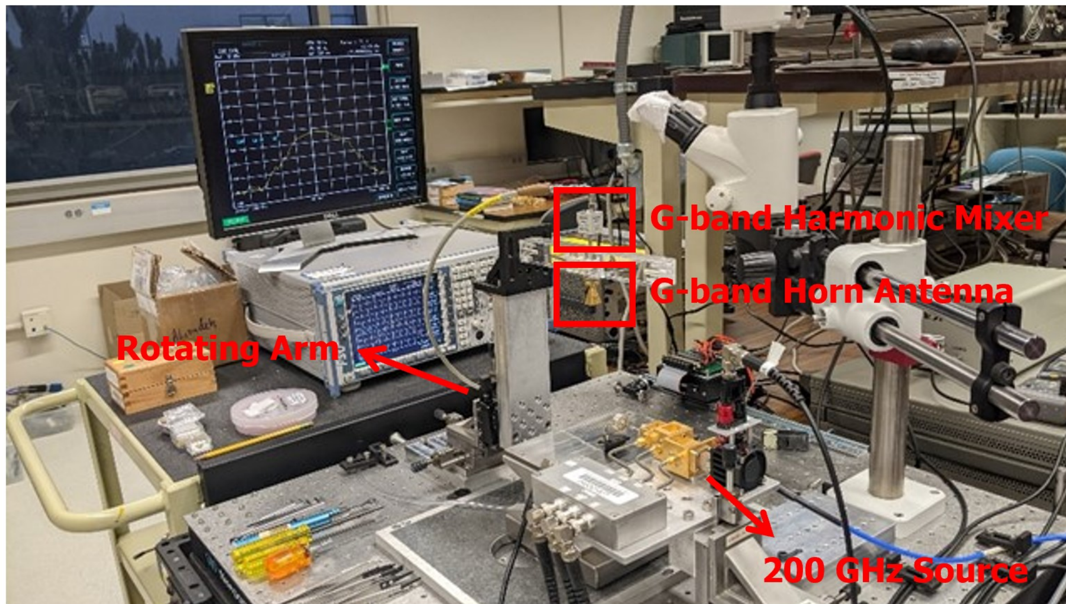


Figure 5.7: Over-the-air antenna testing setup.

and measure its performance, as depicted in Figure 5.7. A G-band horn antenna and harmonic mixer are attached to a rotating arm to measure the antenna beam pattern. A 200 GHz signal is generated using the VDI 8:1 frequency multiplier and applied to the antenna using the GGB G-band on-wafer measurement probe. The antennas are tuned to ensure proper IC-antenna transition, accounting for the wedge bond inductance (Fig. 5.6(b–c)).

Figure 5.8a illustrates the gain and $S11$ of the 50 Ω matched corporate fed 2×2 patch antenna array across the frequency range. The measured $S11$ remains better than -10 dB over a bandwidth of more than 40 GHz. However, the 3-dB gain bandwidth is approximately 20 GHz (192-–212 GHz), with a peak gain of 8.1 dB at 200 GHz. The measured peak gain at 200 GHz is 2 dB lower than the simulated peak gain at 210 GHz. This difference can be attributed to fabrication tolerances and inaccuracies in EM simulations. Figure 5.8b presents the simulated and measured gain in terms of θ at $\phi = 0°$ and 90° cuts. The measured 3 dB beamwidth is approximately 35°.

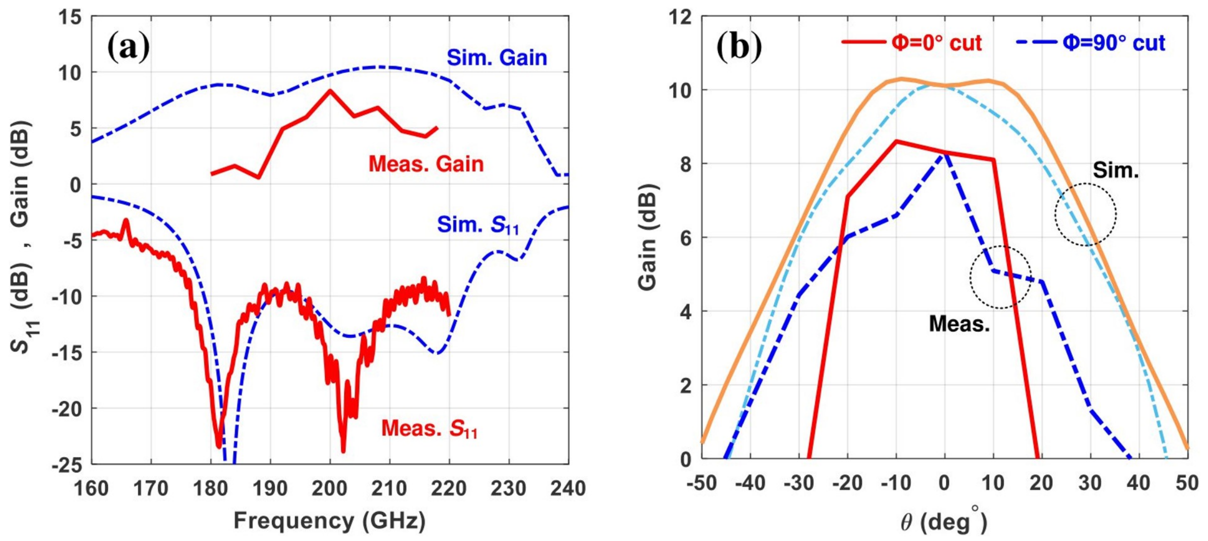


Figure 5.8: 50 Ω matched 2 × 2 patch antenna array results: (a) simulated and measured gain and $S11$ vs. frequency, (b) gain vs. θ for $\phi = 0°$ and 90°.

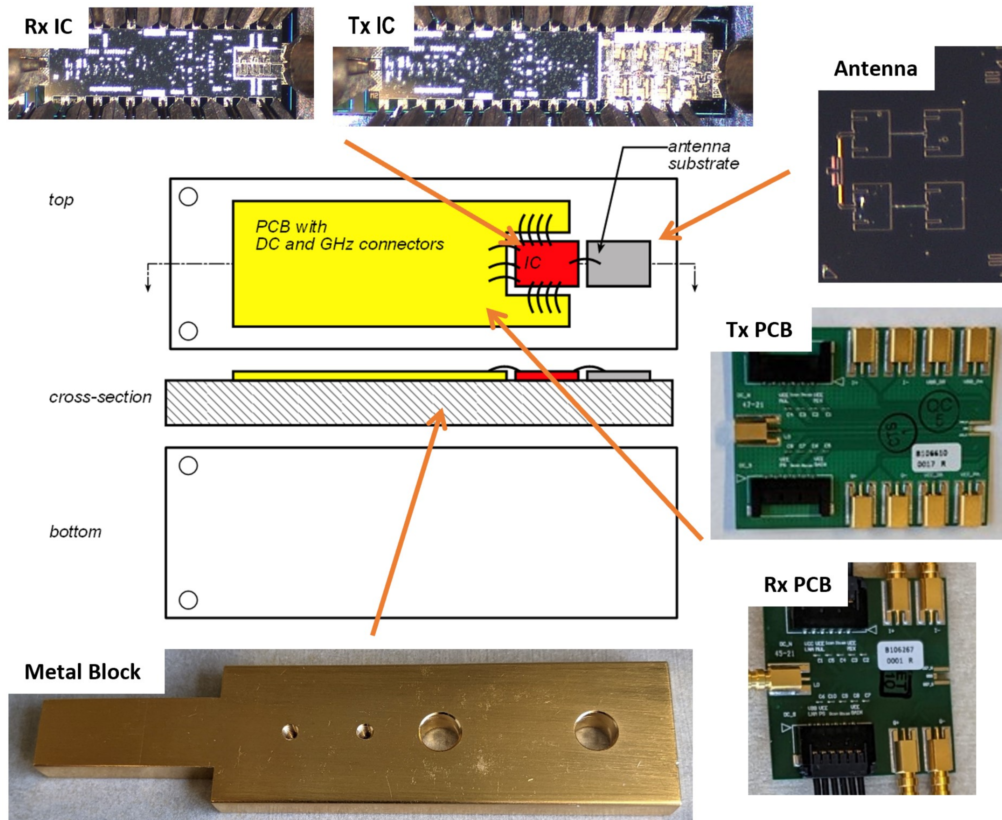


Figure 5.9: Module cartoon drawing for the top and side views.

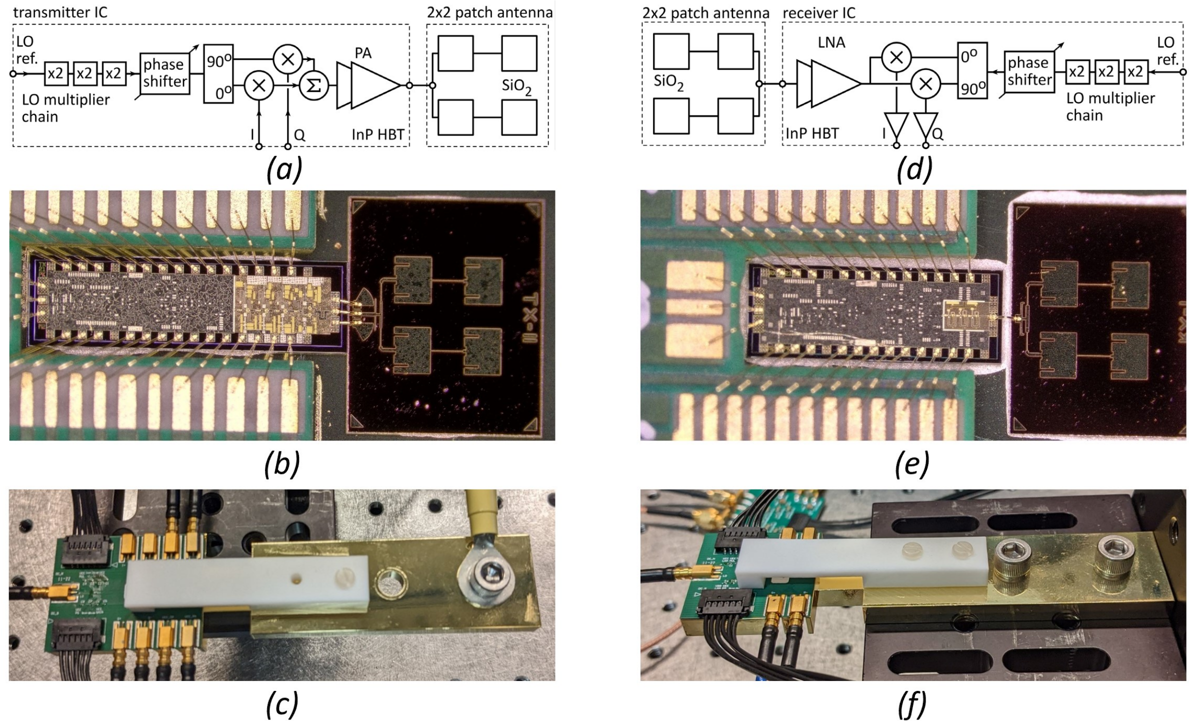


Figure 5.10: 200 GHz transmitter module: (a) block diagram, (b) photograph showing the InP HBT transmitter IC and the patch antenna array on fused silica, and (c) view of the full module, showing the PCB, connectors, heat sink, and PTFE radome. 200 GHz receiver module: (a) block diagram, (b) photograph showing the InP HBT receiver IC and the patch antenna array on fused silica, and (c) view of the full module, showing the PCB, connectors, heat sink, and PTFE radome.

5.2.3 Transmitter and Receiver Modules

Figure 5.9 shows the cartoon drawing of the module for the top and side views. The IC, PCB, and SiO_2 antenna substrate are bonded, with a high thermal conductivity adhesive, to an (Au, Ni)-plated copper heat sink and support. The PCB substrate is made of high-performance I-Tera MT40 material and has a total thickness of 8 mil. The PCB includes a cavity where the IC is placed and has a direct connection to a metal carrier for heat-sinking purposes. A wedge-bonder connected the ICs to the antennas using 1 mil diameter Au bond wires. We simulated the full IC-antenna interface, including the antennas, wire bonds, InP through substrate vias, and even the LNA input-matching

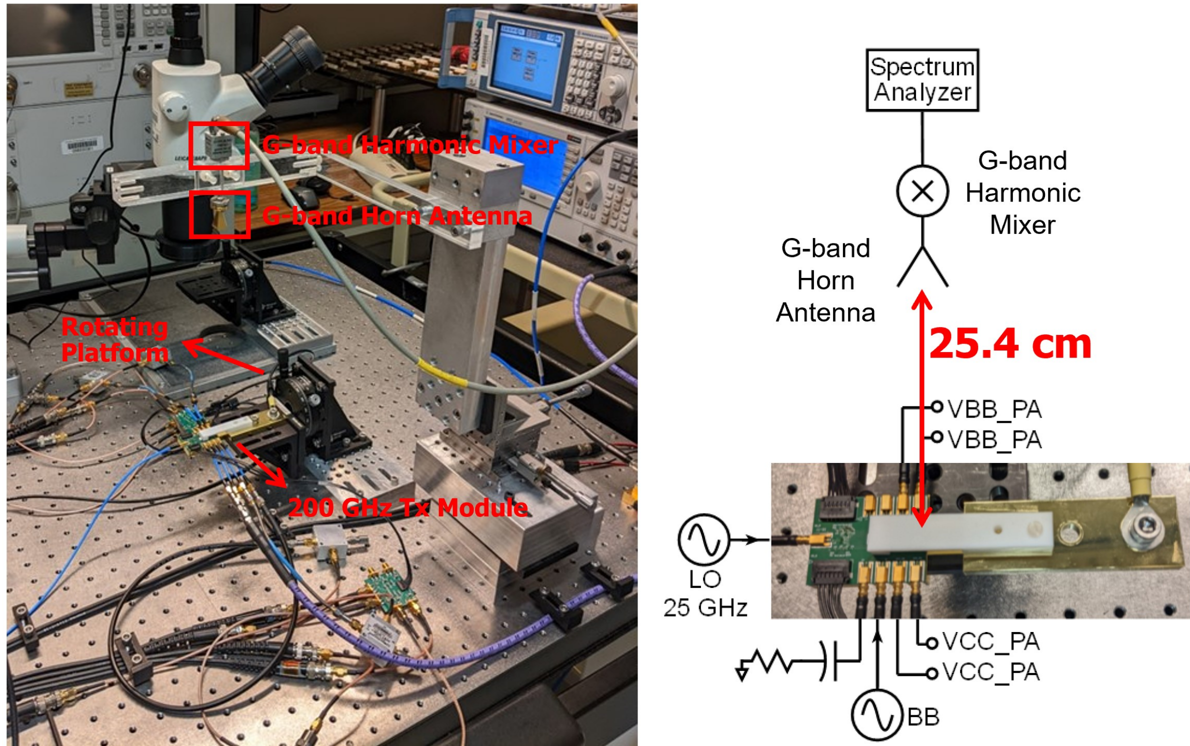


Figure 5.11: Over-the-air transmitter module testing setup.

network and the PA output-matching network. To compensate for bond wire parasitics and adjust the center frequencies of the receiver LNA and transmitter PA to the desired 200 GHz operating frequency, tuning elements were added to the SiO_2 antenna substrate. In the transmitter module, the ground transition occurs from the ground pad on the IC to $\lambda/4$ radial stubs on the antenna via 1 mil diameter Au bond wires. The transmitter (Fig. 5.10(a–c)) and receiver modules (Fig. 5.10(d–f)) consist of an InP HBT transmitter or receiver IC, a 2×2 microstrip patch antenna array on a SiO_2 substrate, and a low-frequency PCB that provides power, LO reference, and (I,Q) interface connections. To safeguard the IC and wire bonds against mechanical damage, a PTFE cover with an ϵ_r=2.1 is employed.

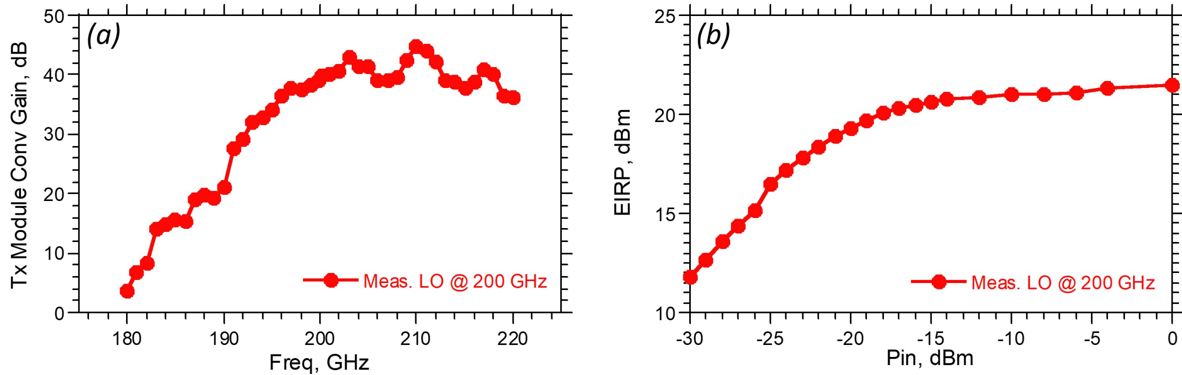


Figure 5.12: (a) Measured conversion gain of the Tx module vs. RF frequency. (b) Measured EIRP of the Tx module vs. baseband input power at 1 GHz.

5.3 Measurement Results

5.3.1 Transmitter Module CW Characterization

Figure 5.11 shows the over-the-air transmitter module measurement setup. The transmitter module is excited through the I channel, and the radiated LO leakage and LO±BB signals are captured by a G-band horn antenna, then down-converted by a G-band harmonic mixer and monitored with a spectrum analyzer. The harmonic mixer is calibrated against a power meter using a directional coupler and a 200 GHz source.

Figure 5.12a presents the conversion gain of the Tx module versus the RF frequency with f_{LO} at 200 GHz. The measured peak conversion gain is 45 dB at 210 GHz. However, due to the gain ripple around 210 GHz, the 3-dB bandwidth is limited. Nevertheless, with post-equalization, this module can be used for high-data-rate wireless transmission experiments. In Figure 5.12b, the EIRP of the Tx module is shown versus the baseband input power at 1 GHz, with f_{LO} at 200 GHz. The peak measured EIRP is 22 dBm, which is a highly competitive number for single-channel transmitter modules. The input 1 dB compression point of the Tx module is −21.1 dBm, with a corresponding EIRP of 18.9 dBm. This value is 3 dB lower than the saturated EIRP.

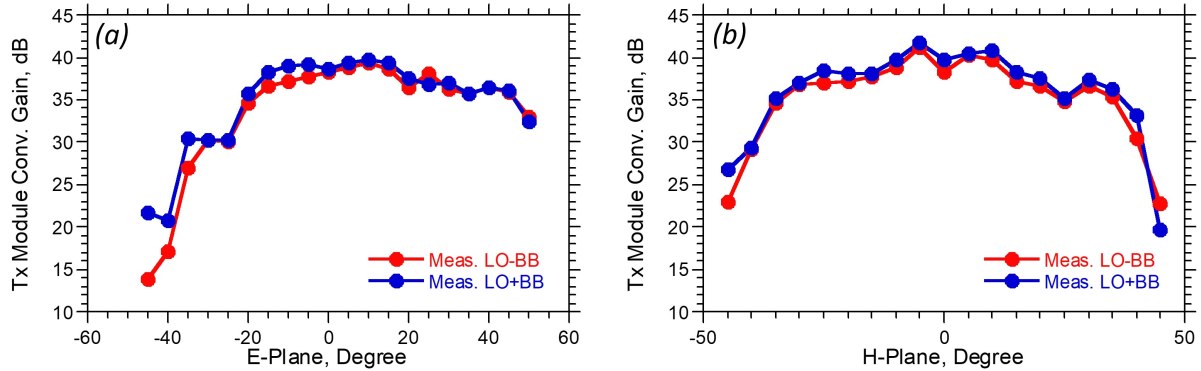


Figure 5.13: Measured conversion gain of the Tx module vs. θ for (a) $\phi = 0°$ and (b) 90°.

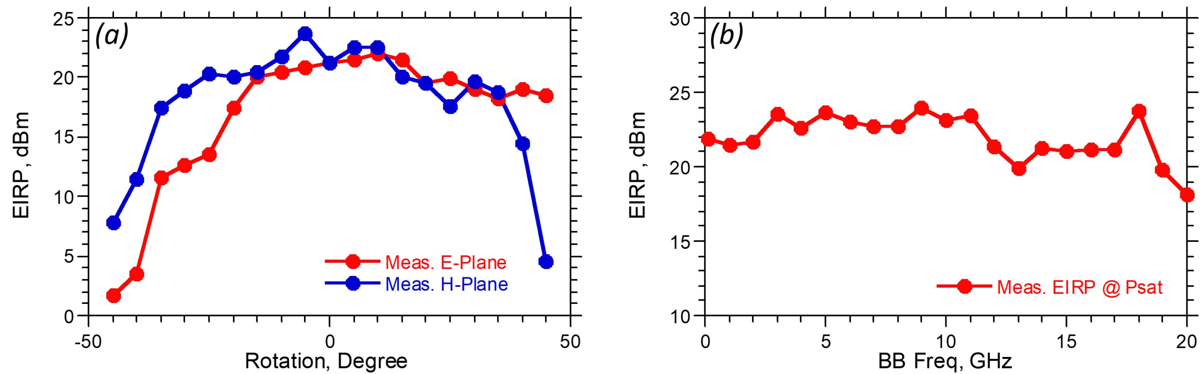


Figure 5.14: Peak EIRP of the Tx module vs. (a) θ for $\phi = 0°$ and 90°, and (b) baseband frequency.

Figure 5.13 shows the module beam pattern measurements. The beam is tilted by 10° on the E-plane, and the measured 3-dB beamwidth is about 62° (Fig. 5.13a). On the H-plane, there is no beam tilt, and the measured 3-dB beamwidth is also around 62° (Fig. 5.13b).

The Tx module is saturated, and its peak EIRP beam pattern is measured (5.14a). The peak EIRP beam is also tilted by 10° on the E-plane. The measured peak EIRP 3-dB beamwidth is about 62° on the E- and H-planes (Fig. 5.13a). The measured EIRP of the TX module vs. baseband frequency is depicted in Figure 5.14b with f_{LO} at 200 GHz. The peak measured EIRP remains higher than 20 dBm over the DC-to-18 GHz baseband frequency range.

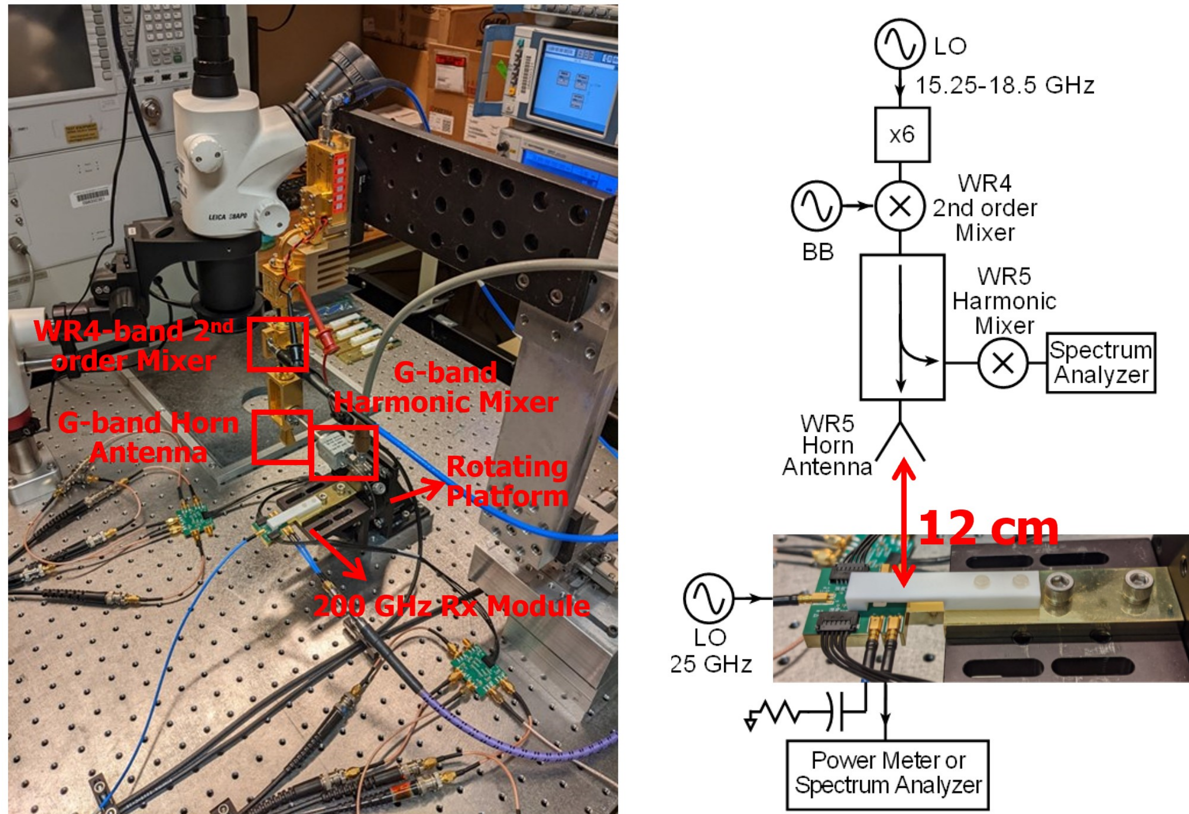


Figure 5.15: Over-the-air receiver module testing setup.

5.3.2 Receiver Module CW Characterization

Figure 5.15 shows the over-the-air receiver module measurement setup. 200 GHz signal is generated using VDI WR-4 2nd order harmonic mixer and 6:1 multiplier chain. The radiated power is monitored using a directional coupler and a WR-5 band harmonic mixer. This allows us to simultaneously measure the radiated power by the VDI WR-4 2nd order harmonic mixer and the down-converted signal by the receiver module, providing an accurate way to measure the receiver module gain.

Figure 5.16a presents the conversion gain of the Rx module versus the RF frequency with f_{LO} at 200 GHz. The measured peak conversion gain is 29 dB and 3-dB bandwidth ranges from 194 to 208 GHz. In Figure 5.16b, the conversion gain of the Rx module is

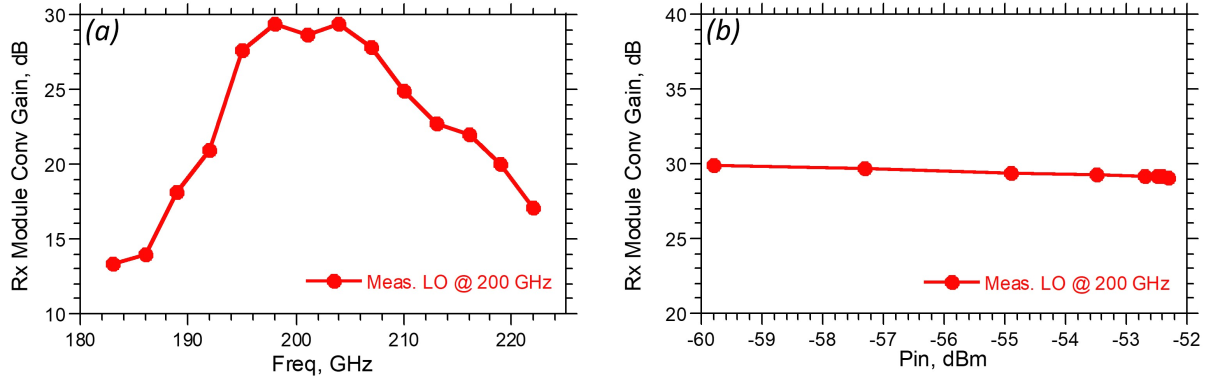


Figure 5.16: Measured conversion gain of the Rx module vs. (a) RF frequency, and (b) RF input power at 201 GHz.

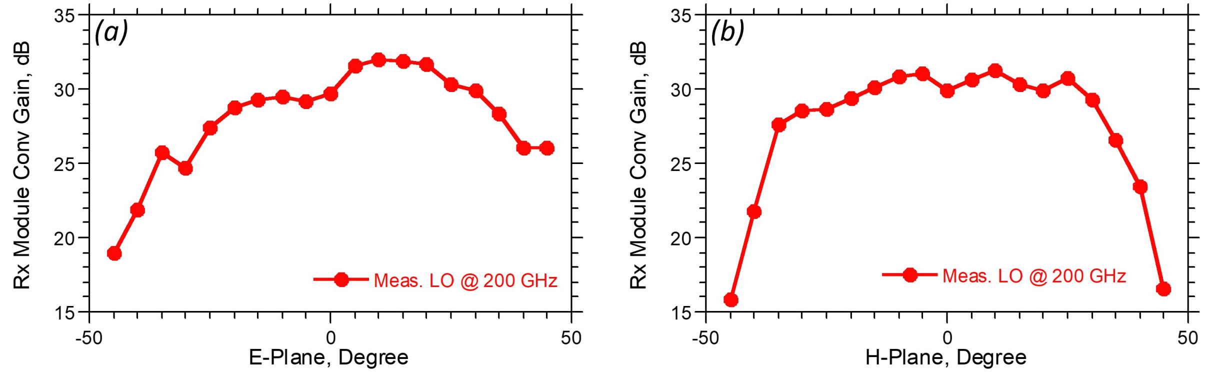


Figure 5.17: Measured conversion gain of the Rx module vs. θ for (a) $\phi = 0°$ and (b) 90°.

shown versus the RF input power at 201 GHz, with f_{LO} at 200 GHz. The VDI *WR*-4 2nd order harmonic mixer does not produce enough power to saturate the receiver module. As will be shown in Chapter 6, the Tx module can easily saturate the Rx module (Fig.6.13b).

Figure 5.17 shows the module beam pattern measurements. The beam is tilted by 10° on the E-plane, and the measured 3-dB beamwidth is about 62° (Fig. 5.17a). On the H-plane, there is no beam tilt, and the measured 3-dB beamwidth is also around 62° (Fig. 5.17b).

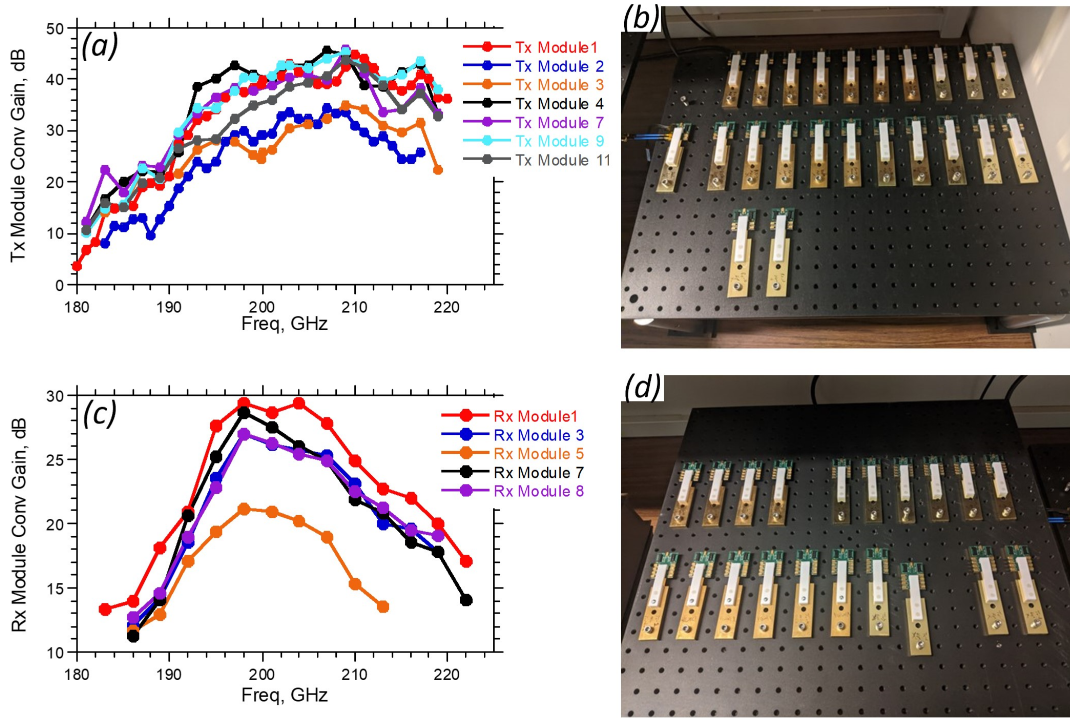


Figure 5.18: (a) Measured conversion gain of all the working Tx modules, (b) photo of all the assembled Tx modules. (c) Measured conversion gain of all the working Rx modules, (b) photo of all the assembled Rx modules.

5.4 Summary and Conclusion

Figure 5.18 shows the measured conversion gain of all the working modules. Due to assembly difficulties, certain modules exhibit less gain than simulated or totally damaged, resulting in an overall assembly yield that is less than 50%. For optimal performance, it is crucial to minimize the length of the high-frequency wedge bond. Therefore, it is critical that the edges of the antenna die and InP IC make direct contact when glued to the metal carrier. While the antenna and InP die mounting were performed perfectly for the Tx module, the Rx module has an additional unwanted spacing (approximately 100 μm) between the Rx antenna and the InP Rx IC, as shown in Figure 5.10e. This spacing degrades the matching between the Rx antenna and the Rx IC, resulting in narrower bandwidth and degraded performance.

Chapter 6

200 GHz Link Experiments

6.1 Introduction

Wireless backhaul links operating within the frequency range of 150–300 GHz offer significant data transmission capacity due to their wide bandwidth and the ability to support 4-8 channels of spatial multiplexing (MIMO) even with short arrays [62]. Extensive progress has been made in the development of transceiver ICs, modules, and links within the 150–300 GHz range [63]. Notable achievements include demonstrations with InP HBT ICs at 142 GHz [64], SiGe HBT ICs at 135 GHz [65] and 230 GHz [45],including results using InGaAs HEMT ICs at 240 GHz [66, 48, 67] and 300 GHz [68, 69, 70, 49, 71].

A considerable number of the transceivers and links that have been reported, particularly those operating at or above 200 GHz, have employed limited levels of integration. In such cases, the transmitter and receiver ICs are constructed by combining multiple waveguide modules, each containing a separate IC. Manufacturing waveguide modules within the 150–300 GHz range requires meticulous dimensional tolerances, resulting in high production costs. In a previous study [39], we introduced integrated 200 GHz transmitter and receiver ICs. In Chapter 5, we detailed the designs of 200 GHz transmitter

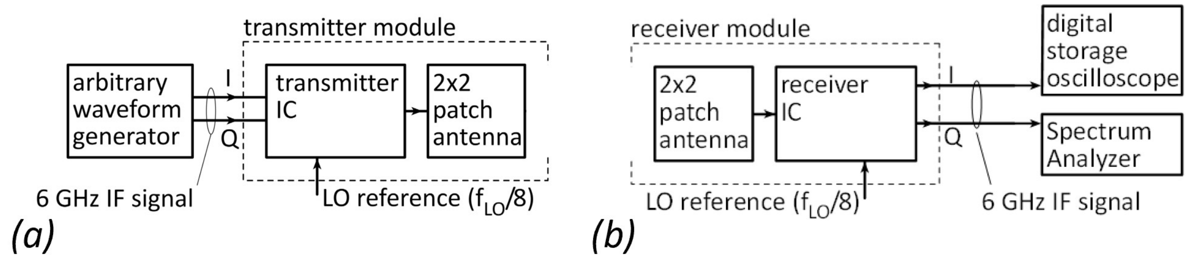


Figure 6.1: Block diagram of the transmission setup. (a) The transmitter is driven by a 6 GHz (I, Q) IF signal carrying QAM or QPSK modulation. (b) The receiver's 6 GHz (I, Q) IF output is captured by a digital storage oscilloscope.

and receiver modules, which were assembled using planar packaging to eliminate the need for waveguide interfaces. We also provided continuous wave characterization of these modules. In this chapter, we present short-range (52.5 cm) and long-range (7.15 m) wireless communication links using these transmitter and receiver modules operating at 200 GHz and validate their functionality through data transmission experiments.

6.2 Transmission Experiments

In the transmission experiments, an arbitrary waveform generator (Keysight M8195A) generates the I and Q signal pair on the channel-1 and channel-2 outputs with 6 GHz intermediate frequency (IF) carrier frequency (Fig. 6.1a). This signal pair is then applied to the I and Q channels of the transmitter module for single-sideband transmission at the upper sideband. Both the transmitter and receiver modules utilize the LO reference from the same source, and the receiver module produces the demodulated 6 GHz I and Q output (Fig. 6.1b). The transmission experiments were performed using QPSK, 16 QAM, 32 QAM, and 64 QAM transmission.

Figure 6.2 illustrates the external optics that can improve the directivity of the transmission, thereby extending its range. A single lens with a 50 mm diameter and a focal point of 75 mm possesses an acceptance angle of $\theta_{lens} = 37°$, which is smaller than the

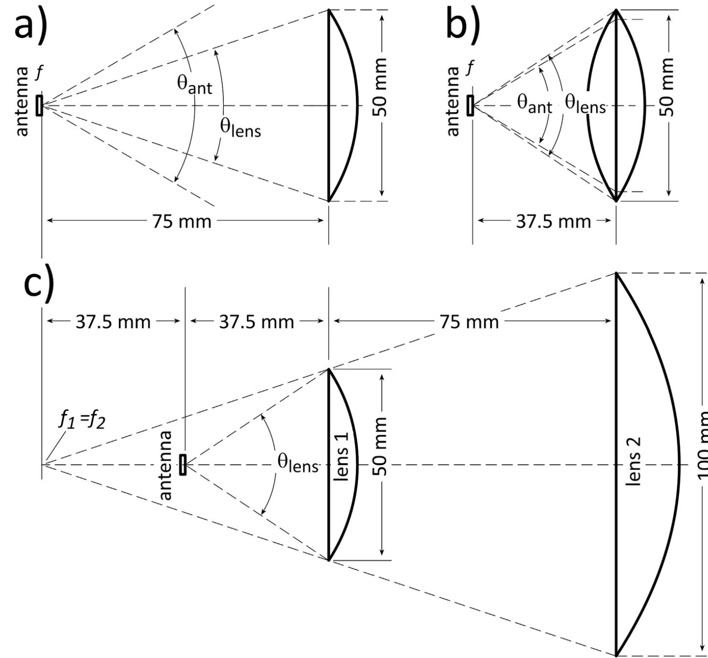
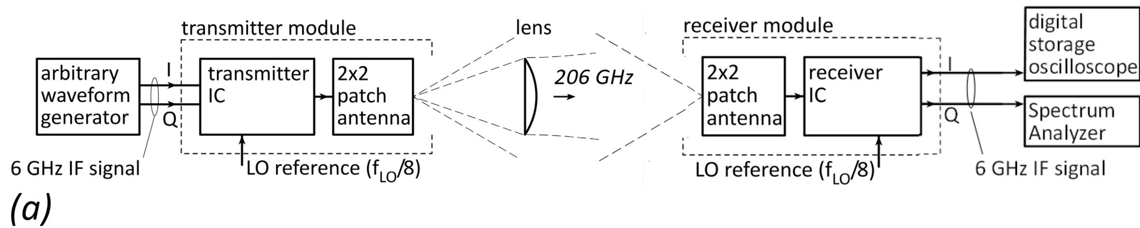
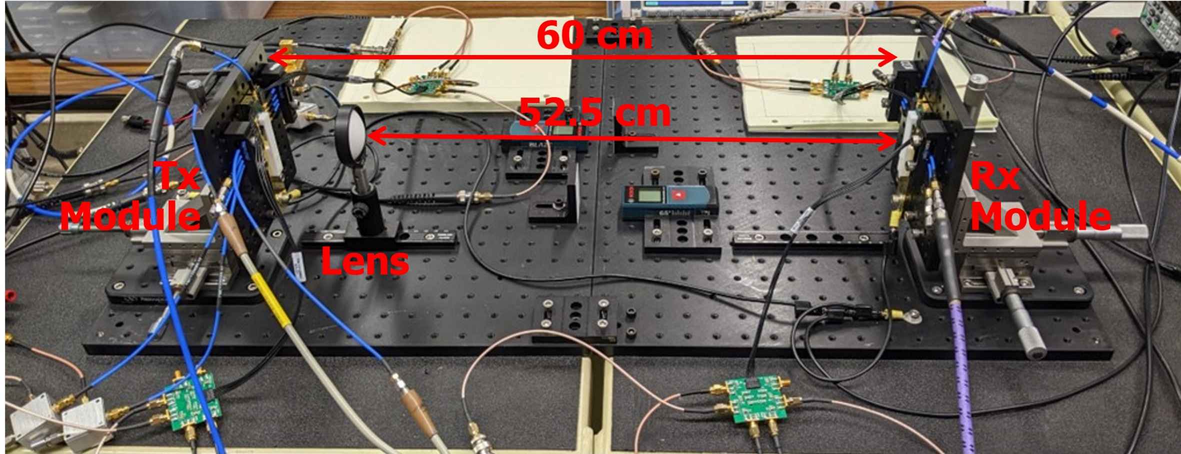


Figure 6.2: External optics: (a) A single 50 mm diameter lens whose maximum acceptance angle, $\theta_{lens} = 37°$, is smaller than the antenna 3 dB beamwidth ($\theta_{ant} = 62°$). (b) Back-to-back lens, using 50 mm diameter lenses, increasing θ_{lens} to 68°, larger than the antenna 3 dB beamwidth. (c) Double lens, using 50 mm and 100 mm diameter lenses, increasing θ_{lens} to 68°, larger than the antenna 3 dB beamwidth.

antenna's 3 dB beamwidth ($\theta_{ant} = 62°$). Consequently, it captures only a fraction of the radiated power (Fig. 6.2a). By employing a back-to-back lens configuration consisting of two 50 mm diameter lenses, the focal point distance is halved to 37.5 mm, resulting in an increased lens acceptance angle of 68°. This arrangement enables the capture of approximately 4.5 dB more of the radiated power compared to the single lens arrangement (Fig. 6.2b). Alternatively, utilizing a double lens setup comprising a 50 mm lens and a 100 mm lens, with focal points at 75 mm and 150 mm respectively, can increase the lens acceptance angle to 68° and also provide an additional ∼6 dB of directivity compared to the back-to-back lens (Fig. 6.2c). However, implementing the double lens configuration shown in Figure 6.2c necessitates precise alignment of the lenses, thereby introducing complexity and making the transmission experiment more tedious.



(a)



(b)

Figure 6.3: (a) Block diagram and (b) photo of the 206 GHz wireless link. The transmitter is driven by a 6 GHz (I, Q) IF signal carrying QAM or QPSK modulation and radiation from the transmitter patch antenna is partially captured and collimated by a PTFE lens. The receiver is at 52.5 cm distance. The receiver 6 GHz (I) IF output is captured by a digital storage oscilloscope.

6.2.1 Short-range Transmission Setup

In the experiment conducted for short-range transmission (Fig. 6.3), an arbitrary waveform generator (Keysight M8195A) is utilized to generate a pair of 6 GHz IF signals, representing the (I=in-phase, Q=quadrature) components. These signals are modulated using QAM or QPSK modulation. The transmitter's local oscillator (LO) port is driven by a 25 GHz input, resulting in the generation of a 200 GHz LO signal. Consequently, the transmitter acts as a single-sideband frequency upconverter, producing a 206 GHz modulated carrier. On the receiving end, the receiver is also driven by a 25 GHz LO signal from the same source, allowing for the demodulation of the 6 GHz (I, Q) output. The I

output signal is captured using a digital storage oscilloscope (Keysight DSAV134A) (Fig. 6.3a). Signal processing algorithms (Keysight VSA2022) are employed to implement adaptive equalization using an 80-tap filter. The transmitted waveforms employ root-raised-cosine shaping with a parameter α set to 0.35. To measure image suppression, a 6 GHz tone is applied to a 90° hybrid, and the resulting outputs from the hybrid are fed back to the transmitter module. The modulated signal is then down-converted using a *WR*-5 OML harmonic mixer. The power levels at 194 GHz and 206 GHz, which are calibrated against a power meter, are continuously monitored. The image suppression is determined to be approximately 17 dB. It is worth noting that a transmitter module with improved I and Q amplitude/phase balance has the potential to provide better image suppression.

The setup for the short-range transmission experiment is depicted in Figure 6.3b. The modules are affixed to aluminum breadboards, which are mounted on XYZ positioners to ensure precise alignment. The distance between the apertures of the transmitter patch antenna and the receiver patch antenna is 60 cm. In order to achieve significantly higher antenna gains than those provided by the 2×2 patch antennas alone, the transmitter antenna is coupled to an external PTFE lens with a diameter of 50 mm and a focal length of 75 mm, as illustrated in Figure 6.3a. An ideal, uniformly illuminated aperture of 50 mm diameter exhibits a directivity of 40.6 dB at 206 GHz. It is worth noting that the antenna's beamwidth of 62° is wider than the lens's maximum acceptance angle, which is calculated to be $(2 \times \arctan(\frac{25\,mm}{75\,mm}) = 37°)$ (Fig. 6.2a). In this particular short-range transmission experiment, no lens is required on the receiver side.

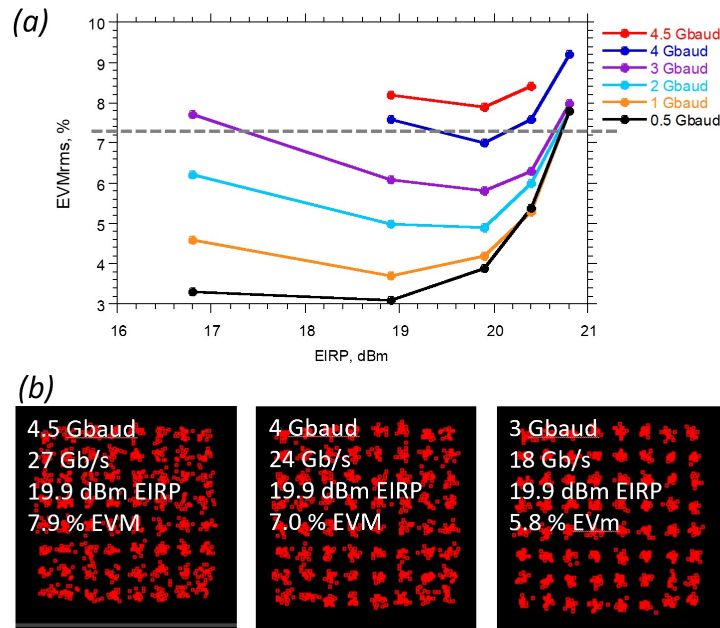


Figure 6.4: (a) Measured EVM_{RMS}, at the receiver, as a function of the transmitter peak EIRP, for 64 QAM modulation, with symbol rates varying from 0.5 Gbaud to 4.5 Gbaud. The gray dotted line indicates the EVM corresponding to 10^{-3} BER. (b) Received data constellations, after adaptive equalization.

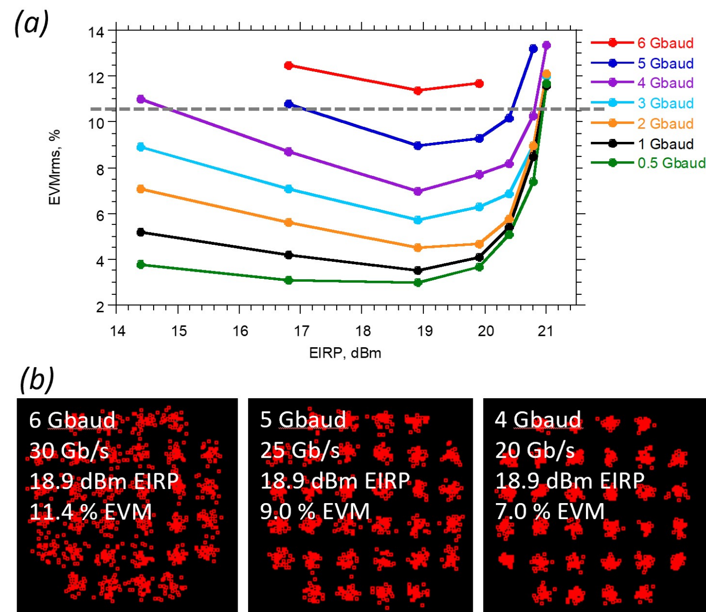


Figure 6.5: (a) Measured EVM_{RMS}, at the receiver, as a function of the transmitter peak EIRP, for 32 QAM modulation, with symbol rates varying from 0.5 Gbaud to 6 Gbaud. The gray dotted line indicates the EVM corresponding to 10^{-3} BER. (b) Received data constellations, after adaptive equalization.

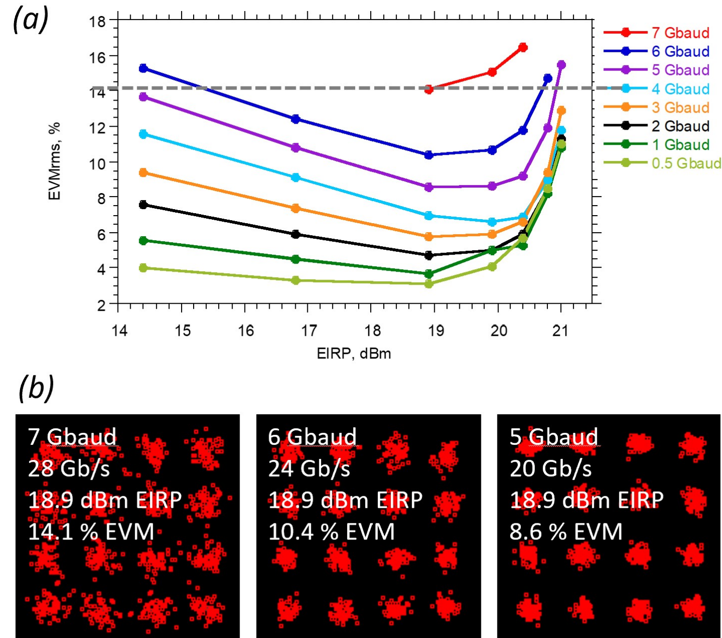


Figure 6.6: Measured EVM_{RMS}, at the receiver, as a function of the transmitter peak EIRP, for 16 QAM modulation, with symbol rates varying from 0.5 Gbaud to 7 Gbaud. The gray dotted line indicates the EVM corresponding to 10^{-3} BER, (b) Received data constellations, after adaptive equalization.

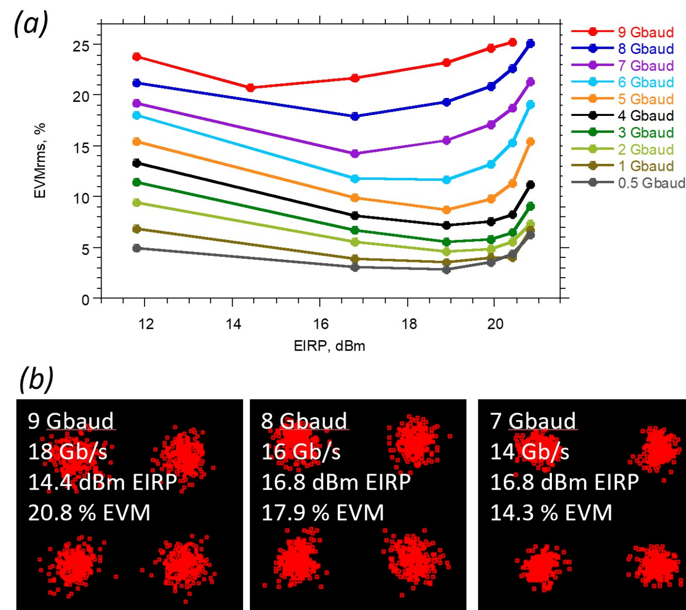


Figure 6.7: Measured EVM_{RMS}, at the receiver, as a function of the transmitter peak EIRP, for QPSK modulation, with symbol rates varying from 0.5 Gbaud to 9 Gbaud. (b) Received data constellations, after adaptive equalization.

6.2.2 Short-range Transmission Experiments

Figures 6.4, 6.5, 6.6, 6.7 show the RMS error vector magnitude (EVM) for 64 QAM (Fig. 6.4), 32 QAM (Fig. 6.5), 16 QAM (Fig. 6.6), and QPSK (Fig. 6.7) data transmission. The gray dotted lines indicate the EVM corresponding to 10^{-3} bit error rate for (BER) for additive white Gaussian noise.

For 64 QAM, $\mathrm{EVM_{RMS}}$ should be less than 7.3% to achieve BER better than 10^{-3}. 4 Gbaud (24 Gb/s) transmission is demonstrated for 64 QAM. Figure 6.4b shows measured received data constellations, after adaptive equalization, for 4.5 Gbaud (7.9% RMS EVM), 4 Gbaud (7.0% RMS EVM), and 3 Gbaud (5.8% RMS EVM) 64 QAM with 19.9 dBm peak EIRP.

For 32 QAM, $\mathrm{EVM_{RMS}}$ should be less than 10.6% to achieve BER better than 10^{-3}. 5 Gbaud (25 Gb/s) transmission is demonstrated for 32 QAM. Figure 6.5b shows measured received data constellations, after adaptive equalization, for 6 Gbaud (11.4% RMS EVM), 5 Gbaud (9.0% RMS EVM), and 4 Gbaud (7.0% EVM) 32 QAM with 18.9 dBm peak EIRP.

For 16 QAM, $\mathrm{EVM_{RMS}}$ should be less than 14.1% to achieve BER better than 10^{-3}. 7 Gbaud (28 Gb/s) transmission is demonstrated for 16 QAM. Figure 6.6b shows measured received data constellations, after adaptive equalization, for 7 Gbaud (14.1% RMS EVM), 6 Gbaud (10.4% RMS EVM), and 5 Gbaud (8.6% EVM) 16 QAM with 18.9 dBm peak EIRP.

For QPSK, $\mathrm{EVM_{RMS}}$ should be less than 31.6% to achieve BER better than 10^{-3}. 9 Gbaud (18 Gb/s) transmission is demonstrated for QPSK. Figure 6.7b shows measured received data constellations, after adaptive equalization, for 9 Gbaud (20.8% RMS EVM) QPSK with 14.4 dBm peak EIRP, 8 Gbaud (17.9% RMS EVM) QPSK with 16.8 dBm peak EIRP, and 7 Gbaud (14.3% EVM) QPSK with 16.8 dBm peak EIRP. The Digital

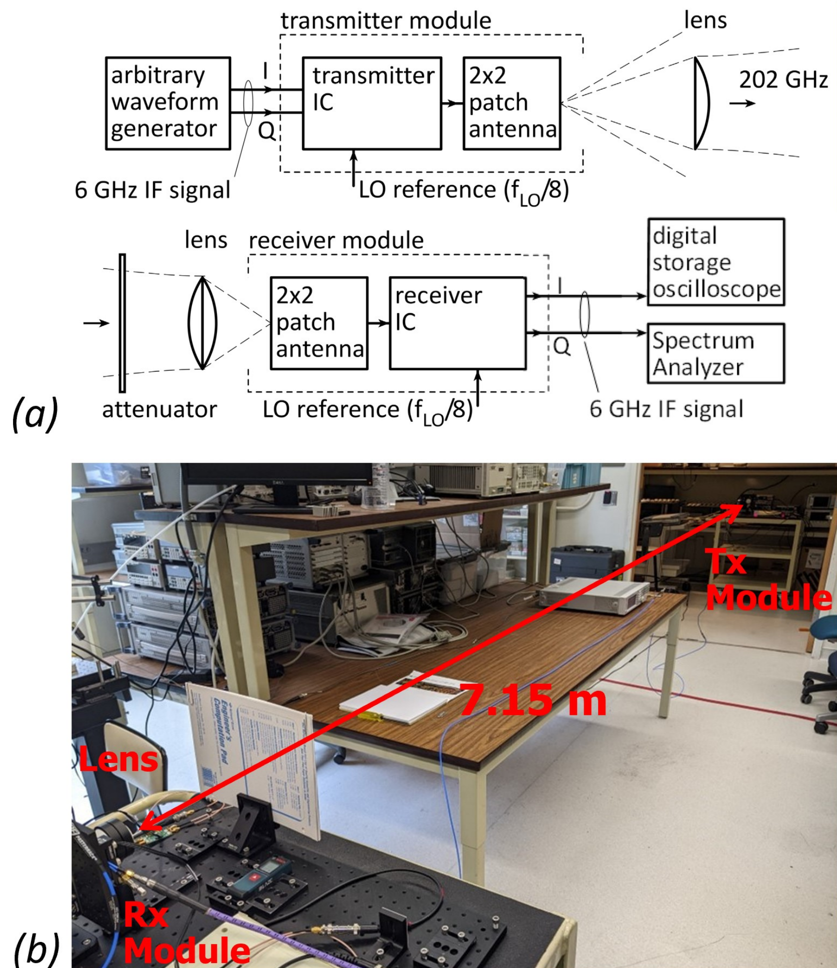


Figure 6.8: (a) Block diagram and (b) photo of the 202 GHz wireless link. The transmitter is driven by a 6 GHz (I, Q) IF signal carrying QAM or QPSK modulation, and radiation from the transmitter patch antenna is partially captured and collimated by a PTFE lens. The receiver, at 7.15 m distance, has a 10.4 dB attenuator and a collimating lens. The receiver 6 GHz (I) IF output is captured by a digital storage oscilloscope.

storage oscilloscope (Keysight DSAV134A) has a bandwidth of 13 GHz, higher data rates can be achieved with QPSK constellation by using a wider bandwidth oscilloscope.

6.2.3 Long-range Transmission Setup

In the long-range transmission experiment (Fig. 6.8), a setup similar to the short-range transmission experiments was employed with one key difference. The LO frequency was shifted from 200 GHz to 196 GHz to ensure that the actual carrier frequency (202 GHz) falls within the flat gain response range of the receiver module (Fig. 5.16a). This adjustment was made to achieve higher data rate transmission. The arbitrary waveform generator (Keysight M8195A) generates a pair of 6 GHz (I, Q) IF signals which carry QAM or QPSK modulation. The transmitter's LO port is driven by a 24.5 GHz signal (compared to 25 GHz in the short-range transmission experiment), resulting in a 196 GHz LO. The transmitter functions as a single-sideband frequency upconverter, producing a 202 GHz modulated carrier. On the receiving end, the receiver is also driven by a 24.5 GHz LO reference signal from the same source, producing demodulated 6 GHz (I, Q) output. The I output signal is recorded using a digital storage oscilloscope (Keysight DSAV134A). Signal processing algorithms (Keysight VSA2022) are utilized to implement adaptive equalization with an 80-tap filter. The transmitted waveforms employ root-raised-cosine shaping with a parameter α set to 0.35.

In order to achieve significantly higher antenna gains than those provided by the 2×2 patch antennas themselves, both the transmitter and receiver antennas are coupled to external PTFE lenses with a diameter of 50 mm and a focal length of 75 mm. It is important to note that an ideal, uniformly illuminated aperture of 50 mm diameter exhibits a directivity of 40.5 dB at 202 GHz. At the receiver, a pair of back-to-back PTFE lenses are arranged to form a composite lens with half the focal length, measuring 37.5 mm. This configuration results in a lens acceptance angle of 68°, allowing the antenna to couple effectively with the lens (Fig. 6.2b).

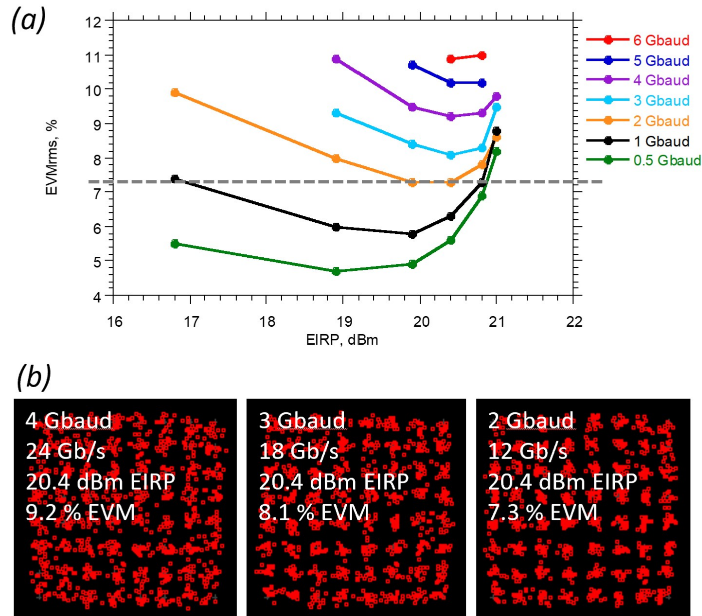


Figure 6.9: (a) Measured EVM_{RMS}, at the receiver, as a function of the transmitter peak EIRP, for 64 QAM modulation, with symbol rates varying from 0.5 Gbaud to 6 Gbaud. The gray dotted line indicates the EVM corresponding to 10^{-3} BER. (b) Received data constellations, after adaptive equalization.

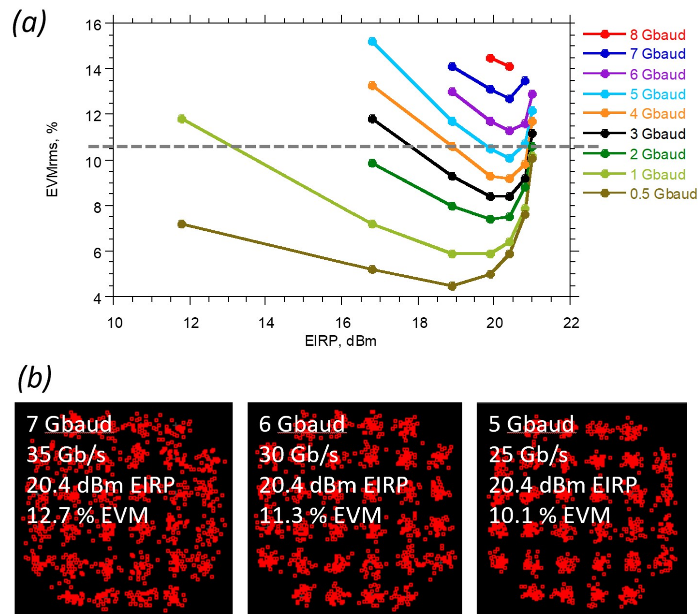


Figure 6.10: (a) Measured EVM_{RMS}, at the receiver, as a function of the transmitter peak EIRP, for 32 QAM modulation, with symbol rates varying from 0.5 Gbaud to 8 Gbaud. The gray dotted line indicates the EVM corresponding to 10^{-3} BER. (b) Received data constellations, after adaptive equalization.

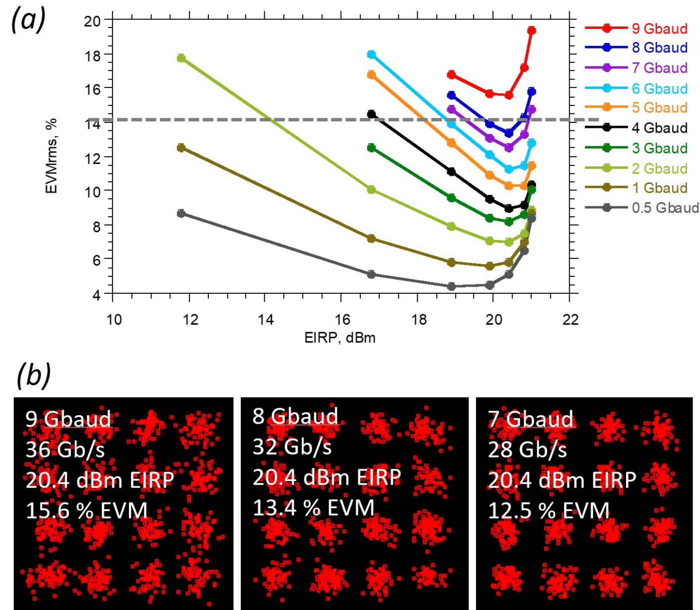


Figure 6.11: Measured $\mathrm{EVM}_{\mathrm{RMS}}$, at the receiver, as a function of the transmitter peak EIRP, for 16 QAM modulation, with symbol rates varying from 0.5 Gbaud to 9 Gbaud. The gray dotted line indicates the EVM corresponding to 10^{-3} BER (b) Received data constellations, after adaptive equalization.

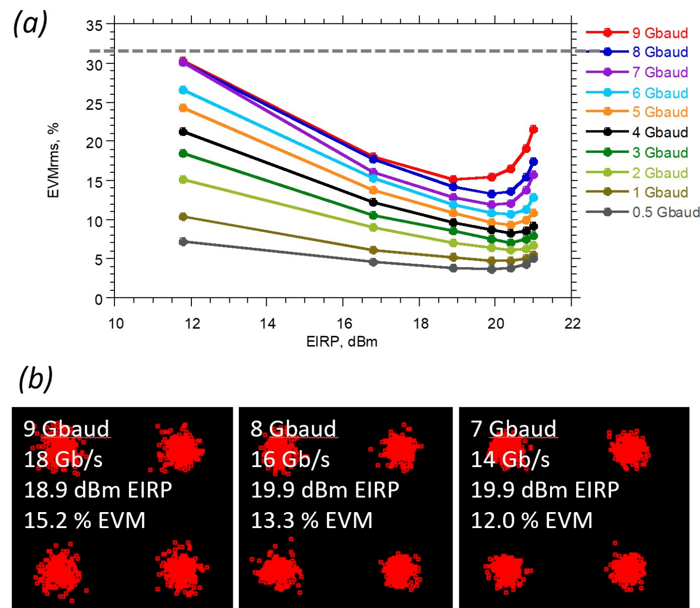


Figure 6.12: Measured $\mathrm{EVM}_{\mathrm{RMS}}$, at the receiver, as a function of the transmitter peak EIRP, for QPSK modulation, with symbol rates varying from 0.5 Gbaud to 9 Gbaud. The gray dotted line indicates the EVM corresponding to 10^{-3} BER (b) Received data constellations, after adaptive equalization.

6.2.4 Long-range Transmission Experiments

Figures 6.9, 6.10, 6.11, 6.12 show the RMS error vector magnitude (EVM) for 64 QAM (Fig. 6.9), 32 QAM (Fig. 6.10), 16 QAM (Fig. 6.11), and QPSK (Fig. 6.12) data transmission. The gray dotted lines indicate the EVM corresponding to 10^{-3} BER for additive white Gaussian noise.

For the 64 QAM data transmission, a 2 Gbaud (12 Gb/s) rate is demonstrated. Figure 6.9b shows the measured received data constellations, after adaptive equalization, for 4 Gbaud (9.2% RMS EVM), 3 Gbaud (8.1% RMS EVM), and 2 Gbaud (7.3% RMS EVM) 64 QAM, with a peak EIRP of 20.4 dBm.

Similarly, a 5 Gbaud (25 Gb/s) transmission is demonstrated for 32 QAM, as shown in Figure 6.10b. The measured received data constellations, after adaptive equalization, are presented for 7 Gbaud (12.7% RMS EVM), 6 Gbaud (11.3% RMS EVM), and 5 Gbaud (10.1% EVM) 32 QAM, with a peak EIRP of 20.4 dBm.

Figure 6.11b illustrates the measured received data constellations, after adaptive equalization, for 16 QAM at an 8 Gbaud (32 Gb/s) transmission rate. The constellations are shown for 9 Gbaud (15.6% RMS EVM), 8 Gbaud (13.4% RMS EVM), and 7 Gbaud (12.5% EVM) 16 QAM, with a peak EIRP of 20.4 dBm.

Lastly, Figure 6.12b displays the measured received data constellations, after adaptive equalization, for QPSK at a 9 Gbaud (18 Gb/s) transmission rate. The constellations are shown for 9 Gbaud (15.2% RMS EVM) QPSK with a peak EIRP of 15.2 dBm, 8 Gbaud (13.3% RMS EVM) QPSK with a peak EIRP of 19.9 dBm, and 7 Gbaud (12.0% EVM) QPSK with a peak EIRP of 19.9 dBm. It is worth mentioning that the digital storage oscilloscope used in the experiment, specifically the Keysight DSAV134A, has a bandwidth of 13 GHz. To achieve higher data rates with QPSK constellations, a wider bandwidth oscilloscope can be utilized.

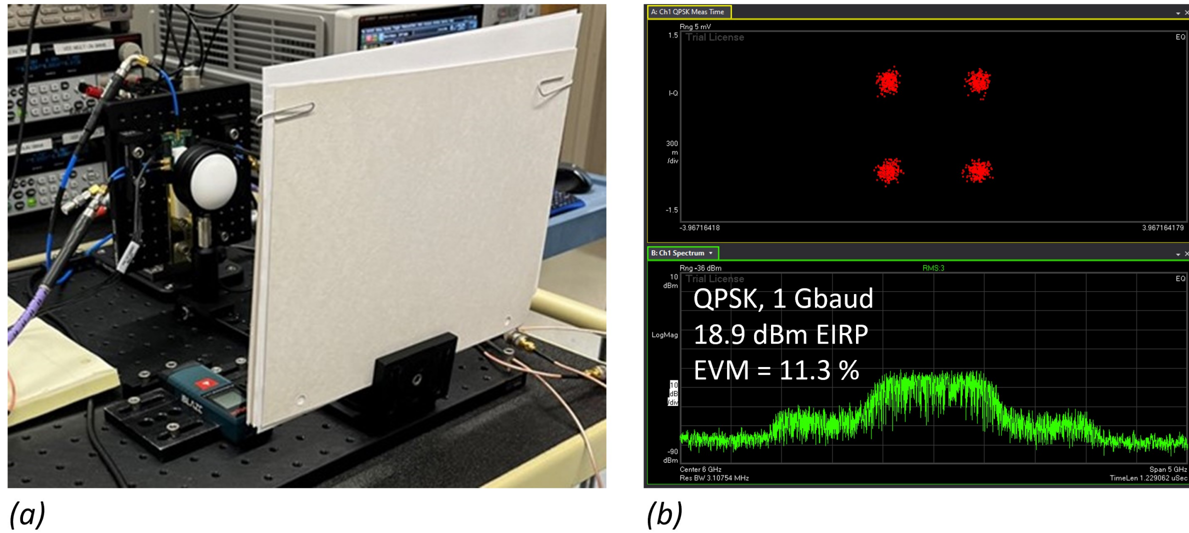


Figure 6.13: (a) Receiver module with several stacked cardboard sheets placed in front. (b) Received QPSK constellation without stacked cardboard. The receiver module is saturated, 3rd order intermodulation products can be observed on the power spectrum.

6.3 Summary and Conclusion

At a transmission range of 7.15 meters, using the lens arrangements depicted in Figure 6.2b at both the transmitter and receiver results in an increase in the EVM at the receiver due to the limited dynamic range of the receiver. To address this issue and reduce the received power by 4.5 dB, the transmitter utilizes the lens arrangement shown in Figure 6.2a, while the receiver employs the arrangement depicted in Figure 6.2b. This combination helps achieve a balanced signal-to-noise ratio.

Additionally, in order to further reduce the received power, several stacked cardboard sheets were placed in the beam path as an attenuator (Fig. 6.13a). Without the stacked cardboard, the receiver module saturates (Fig. 6.13b). These sheets provided an additional attenuation of 10.4 dB. Consequently, the total introduced attenuation is 14.9 dB. Without this attenuation, the same signal-to-noise ratio obtained at a range of 7.15 meters can be achieved at a distance of 40 meters. This calculation is based on the formula: $(7.15\, meters \times 10(\frac{14.9\, dB}{20\, dB}) = 40\, meters)$.

Table 6.1: Comparison of 140–300 GHz transceivers and link experiments.

Ref.†	**Technology**	**Freq. (GHz)**	**Rate (Gb/s)**	**Range (m)**	**Mod.**	$P_{\mathbf{sat}}$ **(dBm)**	**Noise (dB)**	**Antenna-IC connection**
[65]	SiGe HBT	145	36	NA	64QAM	13	8.5	radio-on -glass
[45]	SiGe HBT	230	100	1	16QAM	8.5	11	antenna-on -IC
[66]	InGaAs HEMT	240	40	96	8PSK	-3.6	6	IC-WG bond
[48]	InGaAs HEMT	240	NA	NA	NA	1	4.8	NA
[67]	InGaAs HEMT	240	64	850	8PSK	-4.5	11	IC-WG bond
[68]	InGaAs HEMT	300	10	1.5	32QAM	9.5	10	IC-WG bond
[69]	InGaAs HEMT	300	100	15	16QAM	-1.2	8.5	IC-WG bond
[70]	InGaAs HEMT	300	50	1	QPSK	-7	6.7	IC-WG bond
[49]	InGaAs HEMT	300	120	9.8	16QAM	12	15	IC-WG bond
This work	**InP HBT**	**202**	**32**	**7.1**	**16QAM**	**15**	**8.5**	**IC-antenna bond**

† Spec values for other works were extracted from their text or otherwise estimated from the plots.

Table 6.1 provides a comparison between the current results and previously published transceivers and link experiments operating in the frequency range of 140–300 GHz. The modules utilized in this study demonstrate significantly higher levels of integration compared to the transceiver modules that rely on InGaAs HEMTs. Additionally, the transmitter output power achieved in this study shows favorable performance when compared to other technologies in the same frequency range.

Chapter 7

Conclusions and Future Work

This thesis presents the key components for building an mm-wave communication system, specifically focusing on low noise amplifiers and frequency multipliers. The design fundamentals of low noise amplifiers are covered, and a design technique is proposed to achieve optimal noise performance. This technique involves selecting a bias condition that minimizes the noise measure, scaling the device area to reduce input-matching network losses, and matching the device for the minimum noise measure impedance.

Additionally, the fundamentals of frequency multipliers are studied, and a design technique is presented to minimize the overall DC power consumption of a frequency multiplier chain by avoiding inter-stage amplifiers. The thesis showcases 8:1 and 16:1 frequency multiplier chains that demonstrate exceptional spectral purity and low DC power consumption.

Next, we presented our procedure for constructing 280 GHz transceivers using Teledyne's 250 nm InP HBT technology. Notably, we achieved a remarkable output power and noise performance for transceivers operating in the vicinity of 280 GHz. These results indicate that it is indeed possible to obtain moderate power levels with reasonable efficiency and satisfactory noise performance at such high frequencies. This capability

is crucial for enabling long-range communication links. We discussed the key design features that contributed to achieving these results.

Furthermore, we addressed the transition from the chip level to the packaging level, recognizing that millimeter-wave packaging poses significant challenges in realizing a practical communication system. To tackle this, we showcased the development of 200 GHz planar transceiver modules. These modules utilized fully integrated InP direct-conversion Tx and Rx ICs, along with corporate-fed patch antennas on a 50 μm fused silica substrate.

In addition, we successfully demonstrated a wireless link using a single transmitter and a single receiver module. Notably, we achieved a 32 Gb/s 16 QAM wireless transmission over a distance of 7.15 meters. This accomplishment proves a significant advancement in high-speed wireless communications.

Moving forward, our future endeavors will focus on enhancing data rates over extended distances. In our wireless link measurements, the data rate is limited by the DSO bandwidth and the receiver module assembly. We plan to explore the implementation of a 2×2 MIMO experiment and we aim to support higher data rates while ensuring reliable communication over longer distances. This research direction holds promise for achieving significant advancements in wireless data transmission capabilities.

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