UNIVERSITY OF CALIFORNIA

Santa Barbara

Self-Aligned InGaAs Channel MOS-HEMTs for High Frequency Applications

A dissertation submitted in partial satisfaction of the

requirements for the degree Doctor of Philosophy

in

Electrical and Computer Engineering

by

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September 2023

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ACKNOWLEDGEMENTS

My four years at UCSB were the most rewarding years of my life thus far and they could not have been possible without the countless people who have touched my life. Here I will attempt (and fail) to give them the immense amount credit they deserve.

First, I'd like to thank my committee chair Mark Rodwell for this incredible opportunity. Mark's unique background of circuits and devices provides invaluable insight into the world of electronics. More importantly, Mark's support through the rough times of the project kept me sane. I would also like to thank the rest of my committee Professor Umesh Mishra, Professor Jonathan Klamkin, and Professor Jim Buckwalter for taking the time to listen and provide feedback throughout this process.

As the last in a long line of talented transistor designers in the Rodwell group, I was only able to get this project to work with the accumulated knowledge of previous students. First, thank you to the developers of the digital III-V MOSFET process: Uttam Singisetti, Andy Carter, Sanghoon Lee, and Cheng-Ying Huang. Second, thank you to the developer of the first generation of III-V MOS-HEMTs: Brian Markman. Brians original plan to hand over process modules during the summer of 2020 was thrown out due to covid. While he could have simply said "oh well", Brian volunteered hours of his time to chat with me. This project never would have gotten off the ground without his help. Additionally, Hsin-Ying and Yihao Fang took the time to advise me on my early processing issues even though they were on completely different projects than me. Finally, thank you to the circuits team: Ahmed Ahmed, Ali Farid, Utku Soylu, Amir Alizadeh, Seungchan Lee, and Ceylin Bormali for teaching me about circuits in our weekly group meetings.

So many thanks are owed to the UCSB electronics community. First, the army of staff in the cleanroom that keep our world class facilities running are the lifeblood of electronics at UCSB. Thank you to Brian Thibeault for working so hard to get us back in the lab during covid. Thank you to Don Freeborn, Demis John, Biljana Stamenic, and Bill Mitchell for your help with various tools and process development.

Next, thank you to the incredible MOCVD staff: Mike Iza, Brian Carralejo, and David Whitlatch for keeping the MOCVD lab up and running. Also, a huge thank you to Simoné Tommaso Šuran Brunelli and Bei Shi from the Klamkin group for teaching me the ways of semiconductor growth.

I'd also like to thank Matt Guidry and Christopher Clymore from the Mishra Group for helping me with device testing. The vast majority of the results presented in this work were on their test set-ups with their training and guidance.

Last, I'd like to thank my girlfriend Reema. You convinced me to get on my first plane and fly across the country to follow my dream of making really small stuff; you took care of the other love of my life (my cat Lana) while I was away; and eventually you came out to California to join me on this adventure. I can never thank you enough for the emotional support you provided during my late nights and long weekends in the cleanroom.

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PUBLICATIONS

[1] **Logan Whitaker**, Brian Markman, Mark JW Rodwell, "Self-Aligned InGaAs Channel MOS-HEMTs for High Frequency Applications," *DRC,* 2023.

[2] M. Rodwell, B. Markman, Y. Fang, **L. Whitaker**, H.-Y. Tseng and A. S. H. Ahmed, "Transistors for 100-300GHz Wireless," *DRC,* 2021.

[3] B. Markman, S. T. Š. Brunelli, M. Guidry, **L. Whitaker** and M. J. Rodwell, " Lg = 40nm Composite Channel MOS-HEMT Exhibiting fτ = 420 GHz, fmax = 562 GHz," *DRC,* 2021.

[4] Tyler A Growden, DF Storm, EM Cornuelle, **LM Whitaker**, Brian P Downey, WD Zhang, JW Daulton, R Molnar, ER Brown, Paul R Berger, David J Meyer, " Pulsed characteristics for high current, large area GaN/Ain resonant tunneling diodes*,* 2019.

[5] Tyler A Growden, Evan M Cornuelle, David F Storm, Weidong Zhang, Elliott R Brown, **Logan M Whitaker**, Jeffrey W Daulton, Richard Molnar, David J Meyer, Paul R Berger, " 930 kA/cm2 peak tunneling current density in GaN/AlN resonant tunneling diodes grown on MOCVD GaN-on-sapphire template," *Applied Physics Letters,* vol. 114, no. 20, 2019.

ABSTRACT

Self-Aligned InGaAs Channel MOS-HEMTs for High Frequency Applications

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This work presents the efforts pursued to improve InGaAs/InP FET technologies for high frequency applications. Self-Aligned MOS-HEMTs were developed using a sacrificial InP layer and a diluted HCl sacrificial etch. The new process removes the previous issue of misalignment in MOS-HEMT technology. In addition, the self-aligned process results in a new "V-gate" as opposed to the tradition "T-gate". This new gate technology no longer requires the bi-layer resist used in traditional HEMT technology and allowed for gate footprint scaling from 50 nm to 20 nm.

To improve processability and high frequency performance, a theory on the effects of topside link thickness on resistance, capacitance, and cut off frequency was proposed. Traditionally, HEMTs have thick link regions to keep the donor ions far from the mobile charge in the channel. This keeps scattering and resistance in the source low; however, this places more material in between the source and the gate and increases capacitance. Simply, the theory states that as transistors continue to scale, the mobility of the link becomes less dominant than the extrinsic source gate capacitance when considering optimal link thickness.

In the new process, $C_{GS} + C_{GD}$ was reduced by a total of 40% compared to previous MOS-HEMTs. With these improvements, a L_g = 20 nm device, exhibiting f_τ = 525 GHz, f_{max} = 709 GHz, and a L_g = 36 nm device, exhibiting f_τ = 479 GHz, f_{max} > 1 THz were demonstrated.

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1. Introduction

As consumers demand higher bandwidth and higher data rates, industry is rolling out 5G communication in the 20-80 GHz regime. While industry works to meet the demand of consumers today, researchers must explore design challenges to expand to >100 GHz communication for the future [1]. Communication at higher frequencies requires amplifiers that exhibit gain at these high frequencies. Because transistor gain rolls off at 20 dB/decade at high frequencies, it is advantageous to build amplifiers with cutoff frequencies (f_τ, f_{max}) much greater than the operating frequency of the system.

This work is specifically focused on developing transistors with low noise characteristics for Low Noise Amplifiers (LNAs), for which Field Effect Transistors (FETs) are the preferred device. FETs outperform Heterojunction Bipolar Transistors (HBTs) in noise performance because of their lower parasitic resistances ($[R_S+R_G]*g_m<R_{bb}*g_m$). Current state of the art LNAs utilize a High Mobility Electron Transistor (HEMT) using an InGaAs channel on an InP substrate [2, 3]. The low effective mass InGaAs channel allows high injection velocity (v_{inj}) and therefore high transconductance (g_m) [4]. State of the art HEMTs optimized for f_τ exhibit f_τ = 750 GHz, f_{max} = 1.1 THz, and HEMTs optimized for f_{max} exhibit f_τ = 610 GHz, f_{max} = 1.5 THz [2, 3].

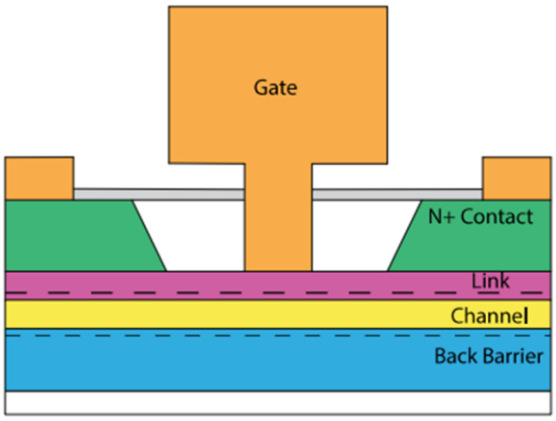


Figure 1.1: Illustration of typical HEMT cross section

Previous improvements in RF performance were attained by scaling transistor gate lengths (L_g). Scaling the transistor gate length improves performance by minimizing the intrinsic transit time but has the unintended effect of reducing the gate to channel capacitance $\left(C_{G-ch} = L_g \left[\frac{t_b}{\epsilon_b} + \frac{t_{ch}}{2\epsilon_{ch}}\right]^{-1}\right)$. Output conductance ($g_{ds}$) is roughly proportional to the ratio of the gate to channel capacitance and drain to channel capacitance (C_{G-ch}/C_{D-ch}) at short gate lengths. Because $C_{G\text{-}ch}$ does not scale with gate length, decreasing gate length by itself can dramatically increase output conductance.

Intelligent designers developed and followed scaling laws to maintain good output conductance as gate lengths scaled [5]. These scaling laws state that if the gate length is cut in half the gate insulator must also be cut in half to maintain channel capacitance and therefore output conductance. Unfortunately, state of the art HEMTs use an InAlAs barrier that has already been aggressively scaled to sub 5 nm thickness. Further scaling of the barrier would result in unacceptable amounts of gate leakage [6]. To address this problem, a new barrier with a larger bandgap and/or a larger dielectric constant would be advantageous.

Work in the Rodwell group from 2009 to 2015 utilized insulators with higher dielectric constants known as “high-k” materials such as Hafnium oxide (HfO_2) and Zirconium oxide (ZrO_2) to build highly scaled transistors for digital applications. These materials provided bandgaps greater than 5.0 eV that allowed sub 3 nm insulator scaling. Additionally, dielectric constants greater than 20 resulted in even high gate to channel capacitances. Because these devices were optimized for digital circuits, die area was of upmost importance [7, 8, 9, 10]. Large gate-contact overlap capacitances prevent these devices from overtaking the state-of-the-art HEMTs for high frequency applications.

To combine the benefits of the high-k with the low capacitance of a HEMT, a MOS-HEMT design was created like illustrated in Figure 1.2 [11]. Markman *et al* reported extrinsic transconductance on par with the state of the art (g_{me} ~ 3 mS/μm) and output conductance roughly 1/3 of the state of the art (g_{ds} ~ 0.25 mS/μm) showing the potential benefit of a MOS-HEMT. Unfortunately, large overlap capacitances resulted from the gate-link overlap limited this design to f_τ = 400 GHz, f_{max} = 600 GHz [12].

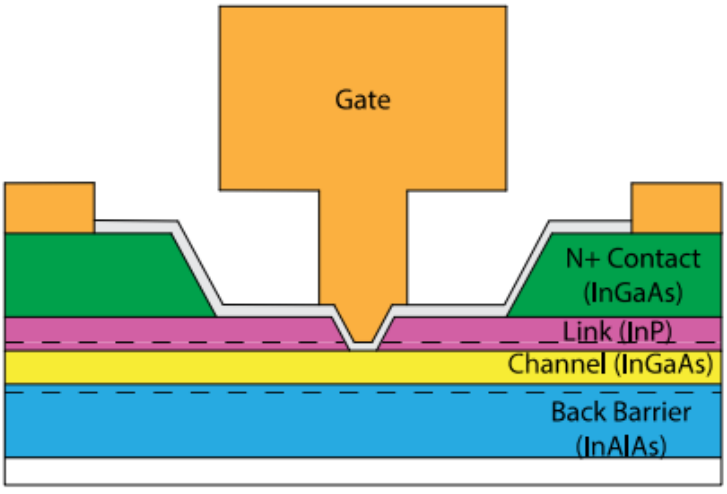


Figure 1.2: Illustration of MOS-HEMT cross section by Markmen et al

Overlap in this design was a result of the T-gate footprint being larger than the gate opening. Because T-gate stems shorter than 50 nm could not be filled with the thermal evaporator set up available, all gate openings shorter than 50 nm needed at least a 50 nm stem attached. Additionally, stems had to be aligned to the gate opening, and to allow for ~25 nm of misalignment in either direction, the gate stems had to be 50 nm larger than the gate openings to ensure complete gating of the channel.

To minimize the overlap capacitance of the previous MOS-HEMT design, this thesis outlines the work to develop a self-aligned process flow and a structure that is easier to fill with metal like seen in Figure 1.3.

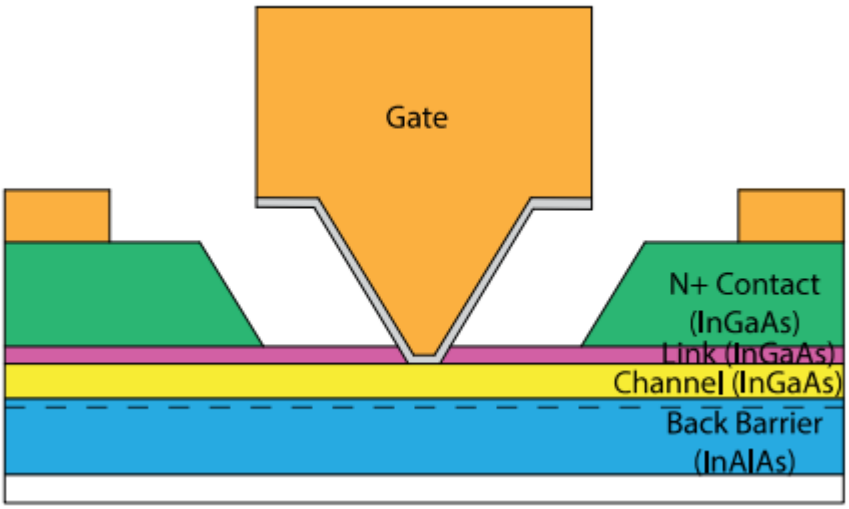


Figure 1.3: Illustration of self-align MOS-HEMT cross section proposed in this work

Chapter 2 (Fet Theory and Design) begins with overviews of basic FET, ballistic FET, and MOS operation. Chapter 2 also includes sections on Gate Design and Link Design within the new device structure. Chapter 3 (RF Testing and Small Signal Modeling) focuses on device testing, characterization, and modeling. Chapter 4 (Processing) overviews the process modules used to build the devices as well as various processing decisions and tradeoffs.

Chapter 5 (Generation 2.1) outlines efforts for the first generation of self-aligned MOS-HEMTs with a L_g = 10 nm device, exhibiting f_τ = 116 GHz, f_{max} = 137 GHz. Results in these devices were extremely limited in part due to high source resistance attributed to poor link end resistance. Additionally, gate-source and gate drain capacitance was limited by incomplete remove of the InP sacrificial layer.

Chapter 6 (Generation 2.2) outlines the second generation of self-aligned MOS-HEMTs with a L_g = 26 nm device, exhibiting f_τ = 196 GHz, f_{max} = 308 GHz. The InGaAs link regrowth was replaced with an InAlAs topside barrier as a part of the epi. This reduced link end resistance by removing the nonplanar regrowth and reduced link sheet resistance by increasing charge confinement. Removal of the InP sacrificial layer proved difficult in this design because the InAlAs link etched in the HCl chemistry.

Chapter 7 (Generation 2.3) outlines the third generation of self-aligned MOS-HEMTs with a L_g = 20 nm device, exhibiting f_τ = 525 GHz, f_{max} = 709 GHz, and a L_g = 36 nm device, exhibiting f_τ = 479 GHz, f_{max} > 1 THz. The InAlAs link was switched back to InGaAs to improve etch selectivity (as in Generation 2.1), but the deposition method was kept the same as Generation 2.2. Additionally, gates were rotated 45 degrees to increase InP undercut etching. Complete removal of the InP resulted in significant improvements in C_{GS} and C_{GD}.

Chapter 8 (Conclusion) summarizes the theoretical and experimental work outlined in this thesis. It also compares results to other work on MOS-HEMTs and HEMTs and gives an avenue for future performance improvements within this technology.

2. Fet Theory and Design

In this chapter, FET theory and design will be discussed. FET theory will start with traditional long gate length theory and then build into the ballistic limit. Next, individual design parameters, specifically the gate and link, will be discussed along with their relation to relevant equivalent circuit parameters and their effect on total RF performance.

A. Drift-Diffusion FET Theory

Field effect transistors (FETs) are variable resistors whose conductance from source to drain is controlled by applying voltage at the gate electrode. Applying a gate voltage increases charge on the surface of the metal gate which then induces opposite charge in the channel.

For the sake of clarity, an nMOS device will be discussed; therefore, a positive bias is applied to positively charge the gate and induce negative charge in the channel. Current in a FET is dominated by the drift of majority carriers due to an electric field between the source and drain, and in general, is equal to the charge times its velocity.

$$J_D(x) = Q_n(x) * v_n(x) \tag{2.1}$$

The velocity and charge are easiest to determine in the "ohmic" or "linear" region of operation, when $V_{GS} > V_{th}$, and V_{DS} is positive but less than V_{GS}-V_{th} . The charge at any point under the channel is equal to the capacitance times the voltage at that point.

$$Q_n(x) = q * C_{gs}\left(V_{gs} - V_{th} - V(x)\right) \tag{2.2}$$

For a long gate length device, the velocity can be estimated using the mobility of the channel and the electric field at that given point.

$$v_n(x) = \mu_n \frac{dV(x)}{dx} \tag{2.3}$$

Plugging in equations (2.2) and (2.3) into (2.1), multiplying by dx, and taking the integral from x=0 to x=Lg, we can find the relationship between current density and applied biases in the linear region.

$$\int_{x=0}^{x=L} J_n = \int_{V(x=0)=0}^{V(x=L)=V_{DS}} qC_{gs}\left(V_{gs} - V_{th} - V(x)\right)\mu_n dV \tag{2.4}$$

$$J_n = \frac{qC_{gs}\mu_n}{L}\left[\left(V_{gs} - V_{th}\right)V_{DS} - \frac{V_{DS}^2}{2}\right] \tag{2.5}$$

Current will continue to increase with increasing V_{DS} until the channel is pinched off. After pinch off, the device is in the "saturation" region. To first order, the drain current does not increase as V_{DS} is increased past V_{GS}-V_{th}. Replacing V_{DS} with V_{GS}-V_{th} results in the equation below.

$$J_n = \frac{qC_{gs}\mu_n}{L}\left[\frac{\left(V_{gs} - V_{th}\right)^2}{2}\right] \tag{2.6}$$

To the second order, the drain current increases with increasing V_{DS} because of the shrinking of the effective gate length. This can be handled with the addition of another term as seen in the equation below.

$$J_n = \frac{qC_{gs}\mu_n}{L}\left[\frac{\left(V_{gs} - V_{th}\right)^2}{2}\right][1 + \lambda V_{ds}] \tag{2.7}$$

If the gate bias is less than the threshold voltage, the device is in the "Subthreshold" region. In this region, the previous charge equation no longer applies, and the charge is now determined by thermal physics. Also, because V_{GS} is less than V_{th}, the channel has very few electrons and is now limited by diffusion current, not drift.

$$J_n = -q * D_n * \frac{dn}{dx} \tag{2.8}$$

If all current is assumed to be due to diffusion of electrons (a good approximation), then the gradient of electrons is constant and can therefore be written simply as:

$$-\frac{dn}{dx} = \frac{\Delta n(0) - \Delta n(L)}{L} = \frac{\Delta n(0)}{L}\left(1 - \exp\left(\frac{qV_{DS}}{kT}\right)\right) \tag{2.9}$$

Charge at the source edge can be related to the background doping (np_0) and the band bending (ψ_s). Additionally, the band bending can be related to V_{GS} and V_{th} by using a constant η derived from the voltage divider between oxide and depletion capacitance.

$$\Delta n(0) = n_{p0} * \exp\left(\frac{\psi_s}{kT}\right) = n_{p0} * \exp\left(\frac{q(V_{GS} - V_T)}{\eta kT}\right) \tag{2.10}$$

Finally, combining equations (2.9) and (2.10) into equation (2.8) results in equation (2.11) below, showing how subthreshold current varies as V_{GS} and V_{DS} change.

$$J_n = \frac{n_{p0}}{L}\exp\left(\frac{q(V_{GS} - V_T)}{\eta kT}\right)\left(1 - \exp\left(\frac{qV_{DS}}{kT}\right)\right) \tag{2.11}$$

B. Ballistic Transport

State of the art transistors no longer fit into the previous assumptions, most glaringly, the mobility model used to predict velocity. As transistor gate lengths continue to shrink, the time it takes for an electron to traverse the channel decreases. As this time approaches the mean scattering time τ, the likelihood of a scattering event taking place decreases, and the validity of the mobility model diminishes. The "Ballistic FET Model" uses the E(k) diagram to predict the injection velocity of the electron from first principles.

At peak bias conditions, V_{DS} is sufficiently large such that the fermi level at the drain is below the eigen state energy in the channel. This means that only positive k states are

populated in the direction of the electron travel. Assuming parabolic bands, the fermi energy can be related to the crystal momentum:

$$q(E_f - E_1) = \frac{\hbar^2 k_f^2}{2m^*}; k_f = \frac{\sqrt{2m^* q(E_f - E_1)}}{\hbar} \tag{2.12}$$

From here, the fermi velocity is by definition related to the derivative of the energy, and therefore is readily known. Additionally, the average velocity of all positively moving electrons can be estimated.

$$v_f = \frac{1}{\hbar}\frac{\partial E_f}{\partial k_f} = \frac{\hbar k_f}{m^*} \tag{2.13}$$

$$\langle v \rangle \approx \frac{4}{3\pi} * v_f = \frac{4\hbar k_f}{3\pi m^*} \tag{2.14}$$

$$\langle v \rangle \approx \sqrt{\frac{32q(E_f - E_1)}{9\pi^2 m^*}} \quad \left(\frac{meters}{second}\right) \tag{2.15}$$

The channel is assumed to be a one-sided infinite quantum well. The charge density in such a well is estimated by using the 2-D density of states and the zero-order Fermi-Dirac integral. The 2-D density of states is divided by 2 because only the positive k state electrons are considered.

$$n_s = \frac{N_{2D}}{2} * F_0 = \frac{N_{2D}}{2} \ln\left[1 + \exp\left(\frac{q(E_F - E_1)}{k_B T}\right)\right] \tag{2.16}$$

$$if\ E_f - E_1 > 3k_B T, F_0 \approx \frac{q(E_F - E_1)}{k_B T} \tag{2.17}$$

$$n_s \approx \frac{N_{2D}}{2} * \frac{q(E_f - E_1)}{k_B T} \tag{2.18}$$

$$N_{2D} = \frac{g_v m^* k_B T}{\pi \hbar^2}; g_v = 1\ for\ InGaAs\ \Gamma - valley \tag{2.19}$$

$$n_s \approx \frac{m^* q\left(E_f - E_1\right)}{2\pi\hbar^2} \quad (meters^{-2}) \tag{2.20}$$

Because peak bias conditions are being considered, the fermi level should be sufficiently above the first eigen state energy to apply a degenerate approximation as seen in equation (2.17). When the 2-D density of states from equation (2.19) is plugged into equation (2.18), the resulting charge density formula in equation (2.20) is a function of fermi level and material parameters. Using the drift equation from the previous section, along with the charge density and average electron velocity, the current density as a function of fermi level can be written as:

$$J = q\langle v \rangle n_s = \frac{q}{\hbar^2\pi^2}\sqrt{\frac{8m^*}{9}\left(q\left(E_f - E_1\right)\right)^3} \left(\frac{Amperes}{meter}\right) \tag{2.21}$$

The current in this equation is limited by the effective mass in the quantum well as well as the maximum allowable gate overdrive ($E_f - E_1$) before:

1. The fermi-level reaches the top of the back barrier and populates a parallel 2-DEG.

   or

2. Intervalley scattering.

C. Gate Capacitance

To relate the fermi level in the channel to the gate voltage, the gate to source capacitance must first be understood. The gate to source capacitance in these devices can be understood as three capacitors in series: insulator capacitance, quantum well capacitance, and density of states capacitance. The insulator capacitance is the parallel plate capacitance from the gate insulator, and in this work, it is the series capacitance of two different oxides.

$$C_{ins} = \frac{\epsilon_{\text{ins}}}{t_{ox}} \tag{2.22}$$

The quantum well capacitance, also commonly known as the wave function capacitance, accounts for the distance between the edge of the insulator and the center of the charge distribution in the channel. The center of the charge distribution is assumed to be at the center of the channel for simplicity. The quantum well capacitance is effectively another oxide capacitance where the dielectric is half of the channel semiconductor.

$$C_{QW} = \frac{\epsilon_{ch}}{t_{ch}/2} \tag{2.23}$$

The density of states capacitance accounts for the moving of the fermi level as additional charge is provided to the channel. At peak bias conditions, the previous assumptions about channel charge are still valid here.

$$C_{DOS} = \frac{\partial(-qn_s)}{\partial(E_f - E_1)} = \frac{\partial}{\partial(E_f - E_1)}\left[\frac{m^* q^2(E_f - E_1)}{2\pi\hbar^2}\right] = \frac{m^* q^2}{2\pi\hbar^2}\left(\frac{F}{m^2}\right) \tag{2.24}$$

Now the gate overdrive can be related to the applied gate bias as a function of C_{DOS} and C_{EET} (the remaining series capacitors) and plugged back into equation (2.21) to find ballistic current as a function of gate voltage.

$$E_f - E_1 = \frac{C_{EET}}{C_{EET} + C_{DOS}} * (V_{GS} - V_{th}) \tag{2.25}$$

$$C_{EET} = \frac{C_{ox} C_{depth}}{C_{ox} + C_{depth}} \tag{2.26}$$

$$J = q\langle v \rangle n_s = \frac{q}{\hbar^2\pi^2}\sqrt{\frac{8m^*}{9}\left(q\left(\frac{C_{EET}}{C_{EET} + C_{DOS}} * (V_{GS} - V_{th})\right)\right)^3}\left(\frac{Amperes}{meter}\right) \tag{2.27}$$

From here transconductance can be found by taking the derivative of the current with respect to gate voltage:

$$g_m = \frac{\partial J}{\partial V_{GS}} = \frac{q}{\hbar^2 \pi^2} \sqrt{2m^* \left(\frac{qC_{EET}}{C_{EET} + C_{DOS}}\right)^3 (V_{GS} - V_{th})} \left(\frac{Siemens}{meter}\right) \quad (2.28)$$

D. Gate Design

Gate design is of vital importance because of its effect on gate resistance. F_{max} is the maximum frequency a transistor still displays power gain and is often expressed as equation (2.29) below [13]. This equation can be rearranged to equation (2.30) to highlight the significance of gate resistance.

$$f_{max} \approx \frac{f_\tau}{2\sqrt{G_{DS}(R_G + R_i + R_s) + 2\pi R_G C_{GD} * f_\tau}} \quad (2.29)$$

$$f_{max} \approx \frac{f_\tau}{2\sqrt{R_G(G_{DS} + 2\pi C_{GD} f_\tau) + G_{DS}(R_S + R_i)}} \quad (2.30)$$

Traditional HEMT technology uses a T-gate like the one seen in Figure 2.1 below. The stem is tall and skinny to minimize the fringe capacitance, and the head of the 'T' is wide and tall to minimize the lateral resistance.

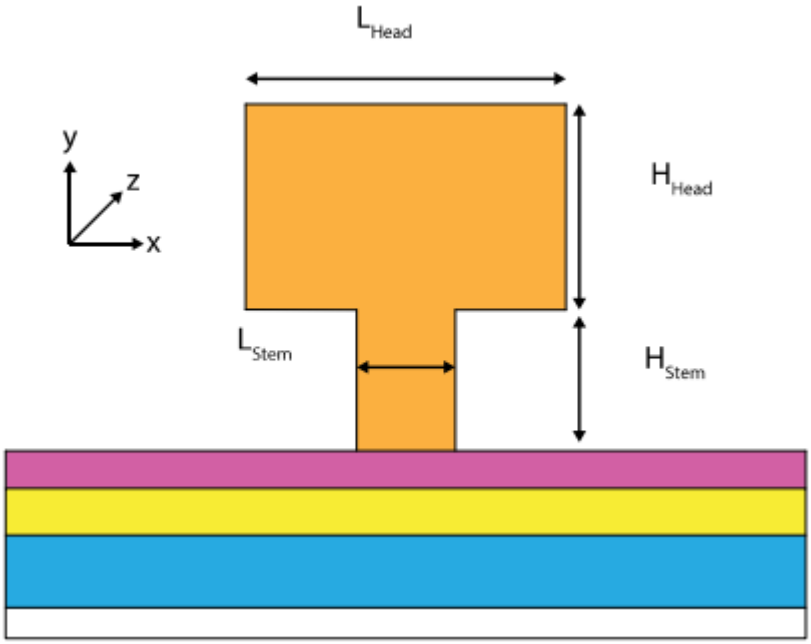


Figure 2.1: Geometric illustration of T-gate

The T-gate is commonly approximated as a series of lateral resistances and vertical admittances to create a transmission line model like seen in Figure 2.2 below [14]. $R_{lateral}$ and $R_{vertical}$ can be approximated by looking at the geometry of a T-gate in Figure 2.1.

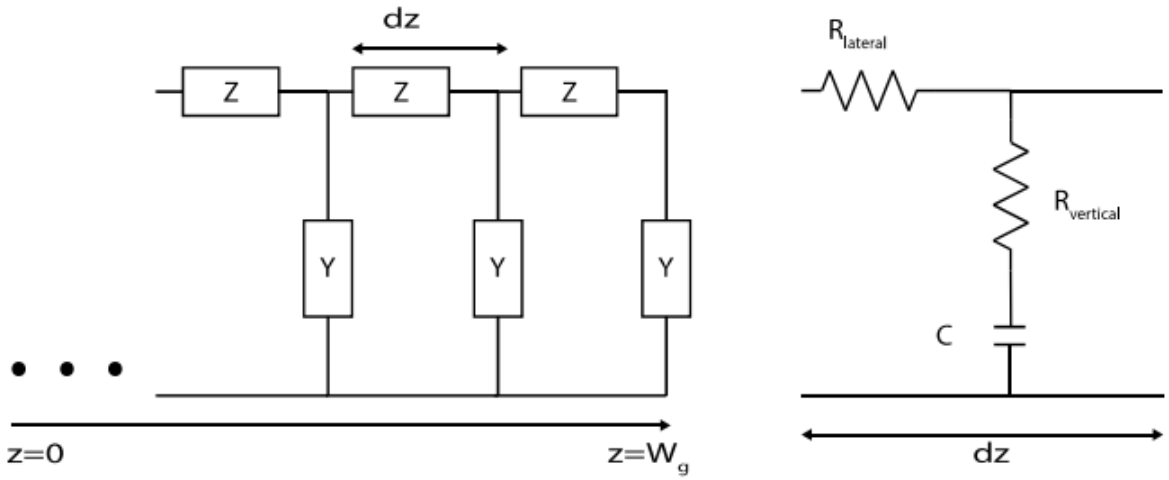


Figure 2.2: Transmission line model for gate resistance

$R_{lateral}$ is approximated using the area of the gate head and the resistivity of the material, usually gold. Technically, the effective lateral area should include some fraction of the stem area as well, but for a highly scaled and well-designed T-gate, A_{stem} should be much less than A_{head}.

$$R_{lateral} = \frac{\rho}{(A_{head} + \gamma A_{stem})} \approx \frac{\rho}{A_{head}} = \frac{\rho}{H_{head} L_{head}} \tag{2.31}$$

$$R_{lateral} = R_{end\ to\ end}/W_g \tag{2.32}$$

$R_{vertical}$ is approximated using the stem length and the stem height. Once again, the effective vertical conductance should include some fraction of the vertical resistance through the gate head, but for a highly scaled and well-designed T-gate, the vertical resistance through the head should be much smaller than through the stem.

$$R_{vertical} = \rho\left(\frac{H_{head}}{L_{head}} + \frac{H_{stem}}{L_{stem}}\right) \approx \frac{\rho H_{stem}}{L_{stem}} \tag{2.33}$$

From generalized transmission line theory, the telegraphers' equations can be written as functions of lateral resistance and vertical conductance. Assuming a one-sided gate connection, $I(W_g) = 0$ is the valid boundary condition. Simplifying the gate resistance expression results in a hyperbolic cotangent that can be estimated using the first 2 components of the Laurent series that results in the familiar expression seen in equation (2.43).

$$V(z) = V_0^+ e^{-\gamma z} + V_0^- e^{\gamma z} \tag{2.34}$$

$$I(z) = \frac{V_0^+ e^{-\gamma z} - V_0^- e^{\gamma z}}{Z_0} \tag{2.35}$$

$$Z_0 = \sqrt{Z/Y} \tag{2.36}$$

$$\gamma = \sqrt{Y * Z} \tag{2.37}$$

$$Z = R_{lateral} = \rho H_{head} * L_{head} \tag{2.38}$$

$$Y = \frac{j\omega C * L_{stem}}{1 + j\omega C * L_{stem} * R_{vertical}} \tag{2.39}$$

$$I(W_g) = 0 = \frac{V_0^+ e^{-\gamma W_g} - V_0^- e^{\gamma W_g}}{Z_0} \rightarrow V_0^+ = V_0^- e^{2\gamma W_g} \tag{2.40}$$

$$Z_g = \frac{V(0)}{I(0)} = Z_0 \frac{V_0^+ + V_0^-}{V_0^+ - V_0^-} = Z_0 \frac{e^{2\gamma W_g} + 1}{e^{2\gamma W_g} - 1} = Z_0 \coth(\gamma W_g) \approx Z_0\left(\frac{1}{\gamma W_g} + \frac{\gamma W_g}{3}\right) \tag{2.41}$$

$$Z_0\left(\frac{1}{\gamma W_g} + \frac{\gamma W_g}{3}\right) = \sqrt{\frac{Z}{Y}}\left(\frac{1}{W_g\sqrt{Y * Z}} + \frac{W_g\sqrt{Y * Z}}{3}\right) = \frac{1}{W_g * Y} + \frac{W_g * Z}{3} \tag{2.42}$$

$$R_g = Re\{Z_g\} \approx \frac{R_v}{W_g} + \frac{W_g R_L}{3} = \frac{\rho H_{stem}}{W_g L_{stem}} + W_g * \frac{\rho}{3 H_{head} L_{head}} \tag{2.43}$$

This shows that vertical gate resistance is inversely proportional to gate width, while lateral gate resistance is proportional to gate width. Current state of the art InP-HEMTs aggressively scale gate lengths to 25 nm to minimize $C_{GS,i}$ and gate widths to 4 μm to minimize the lateral gate resistance component [2]. By making reasonable assumptions about the gate geometry and the bulk resistivity, the gate resistance can be estimated. Assuming H_{head} = 300

nm, H_{stem} = 100 nm, L_{head} = 500 nm, L_{stem} = 25 nm, $\rho_{lateral}$ = 2e-7 Ω*m, $\rho_{vertical}$ = 2e-6 Ω*m, and W_g = 4 μm, the vertical gate resistance component is about 50% of the entire gate resistance.

Bulk resistivity here is estimated by using known gate resistance values. Additionally, the vertical resistivity is assumed to be an order of magnitude greater than the lateral resistivity based on experimental work on the relationship between thin film and thick film resistances [15].

As HEMTs continue to scale more aggressively, shorter gate lengths will increase the vertical component of the gate resistance. If the gate length is shrunk to 10 nm while the width is left at 4 μm, the vertical component is now about 70% of the total gate resistance. Further scaling of the gate length or the gate width would continue to exacerbate this issue. To continue scaling gate resistance, vertical resistance will need to be minimized.

A possible solution is the V-gate technology proposed in this work and illustrated in Figure 2.3. Because the differential resistance is inversely proportional to the stem length, and the stem is no longer a constant thickness, the differential resistance can be rewritten as:

$$dR_v = \rho \frac{dy}{L_{stem}(y)}; \quad L_{stem}(y) = L_{gate} + 2y\cot(\theta) \tag{2.44}$$

By taking the integral the vertical resistance can be written as:

$$R_v = \rho \int_{y=0}^{y=H_{stem}} \frac{1}{L_{gate} + 2y\cot(\theta)} dy = \frac{\rho \tan(\theta)}{2} * \ln\left[\frac{L_{gate} + 2H_{stem}\cot\theta}{L_{gate}}\right] \tag{2.45}$$

$$for\ 0 < \theta < 90$$

As θ approaches 90 degrees, R_v simplifies back to its previous formula, and as θ approaches 0 degrees, R_v approaches zero because the effective stem width approaches

infinity. Current V-gate technology has a θ of about 45 degrees which results in the convenient simplification:

$$R_v = \frac{\rho}{2} \ln \left[\frac{L_{gate} + 2H_{stem}}{L_{gate}} \right] \tag{2.46}$$

Figure 2.3 below shows the model used to compare gate resistance for different gate lengths, gate widths, and V-gate stem angles. Figure 2.4 shows the vertical resistance divided by the bulk resistivity. This shows that as gate lengths continue to scale, the vertical resistance will increase for all V-gate angles, but angles less than 90 degrees have significantly less vertical resistance.

Lastly, Figure 2.5 shows how the R_v/W_g and $W_g*R_L/3$ terms vary as the gate width, W_g, varies. This shows that current state of the art T-gate (W_g=4 μm, L_g = 25 nm, θ = 90º) could potentially reduce total gate resistance by almost 50% by switching to a 45º V-gate. Additionally, future L_g = 10 nm devices could reduce total gate resistance by approximately 70%.

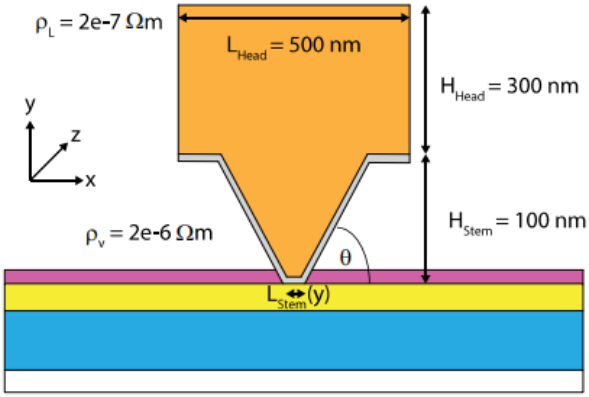


Figure 2.3: Geometric illustration of V-gate cross section

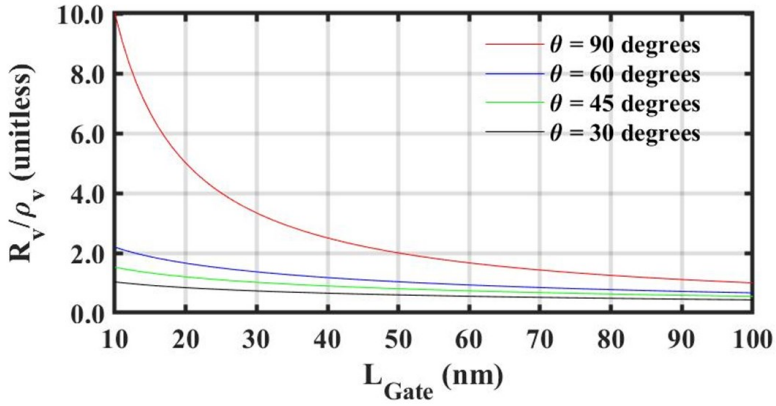


Figure 2.4: Vertical gate resistance component vs gate length for different gate stem

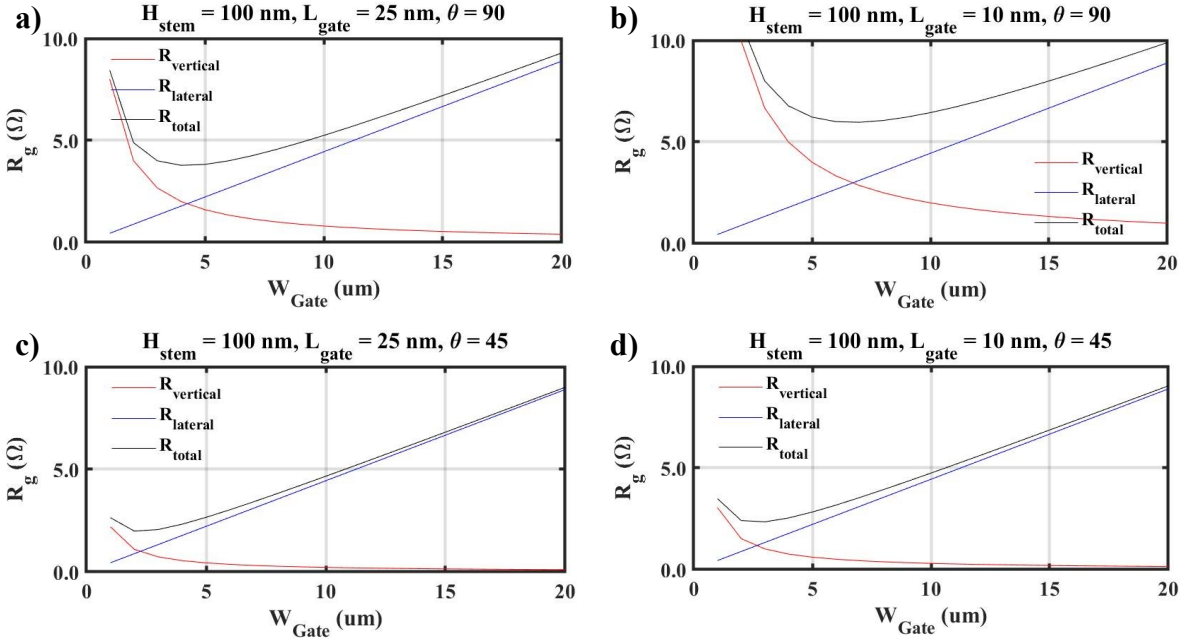


Figure 2.5: Vertical, lateral, and total gate resistance vs gate width for a) L_{gate} = 25 nm, θ = 90º b) L_{gate} = 25 nm, θ = 45º c) L_{gate} = 10 nm, θ = 90º d) L_{gate} = 10 nm, θ = 45º

E. Link Design

The link, often referred to as the access region in other works, is the region between the thick source / drain contact regions and the gated channel. In previous generations of MOS-HEMTs, the link region consisted of an InGaAs channel with a 106 nm InAlAs bottom barrier and a 16 nm InP top barrier like in Figure 2.6. Both the top and bottom barriers have thin layers of highly doped material offset from the channel by about 3 nm.

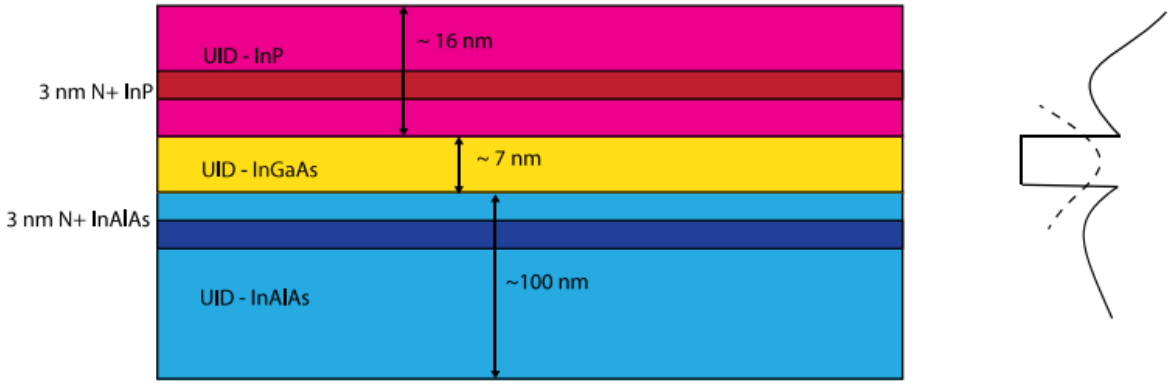


Figure 2.6: Illustration of previous MOS-HEMT link design and approximate band diagram

This type of link design keeps the donor ions far from the mobile charge in the channel and therefore minimizing impurity scattering. This results in the HEMTs signature "High Electron Mobility", generally in the 10,000-15,000 $cm^2V^{-1}s^{-1}$ range [16]. High link mobility minimizes link resistance and therefore total source resistance.

Previous work on MOS-HEMTs had limited high frequency performance in large part due to high capacitance [11]. It was hypothesized that this high capacitance was a result of the gate-link overlap circled in red in Figure 2.7.

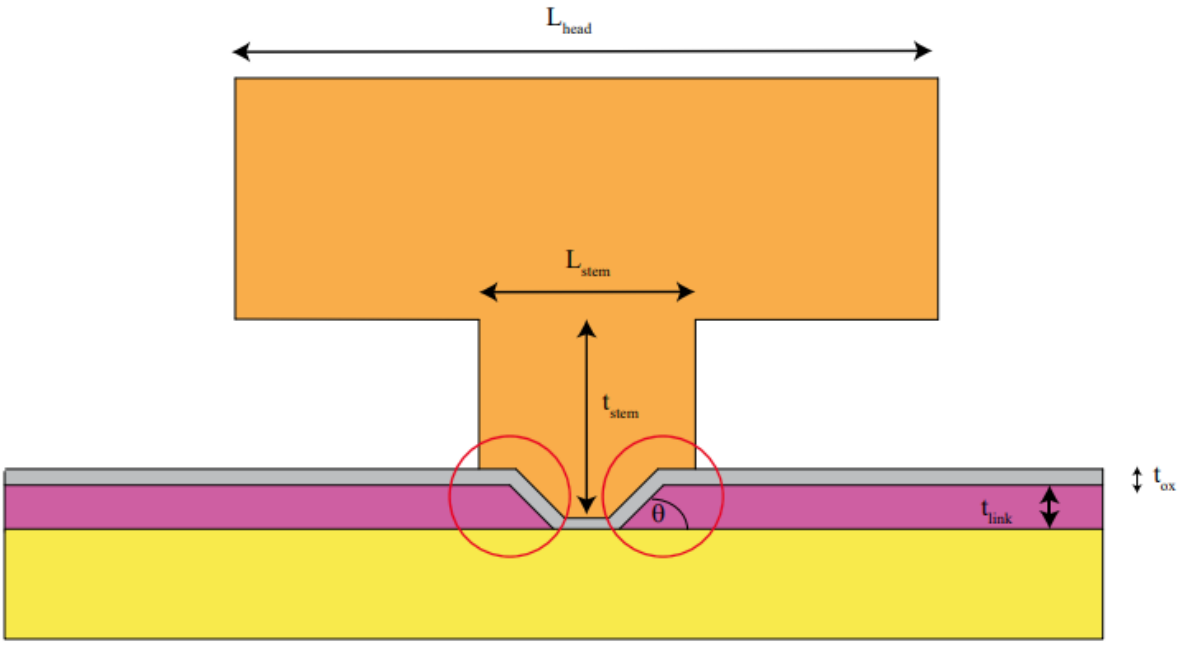


Figure 2.7: Illustration of non-self aligned MOS-HEMT gate-link overlap

To minimize the gate-link overlap, the self-aligned process outlined in this work was developed; however, a thick link still results in substantial gate-link overlap as seen in Figure 2.8.

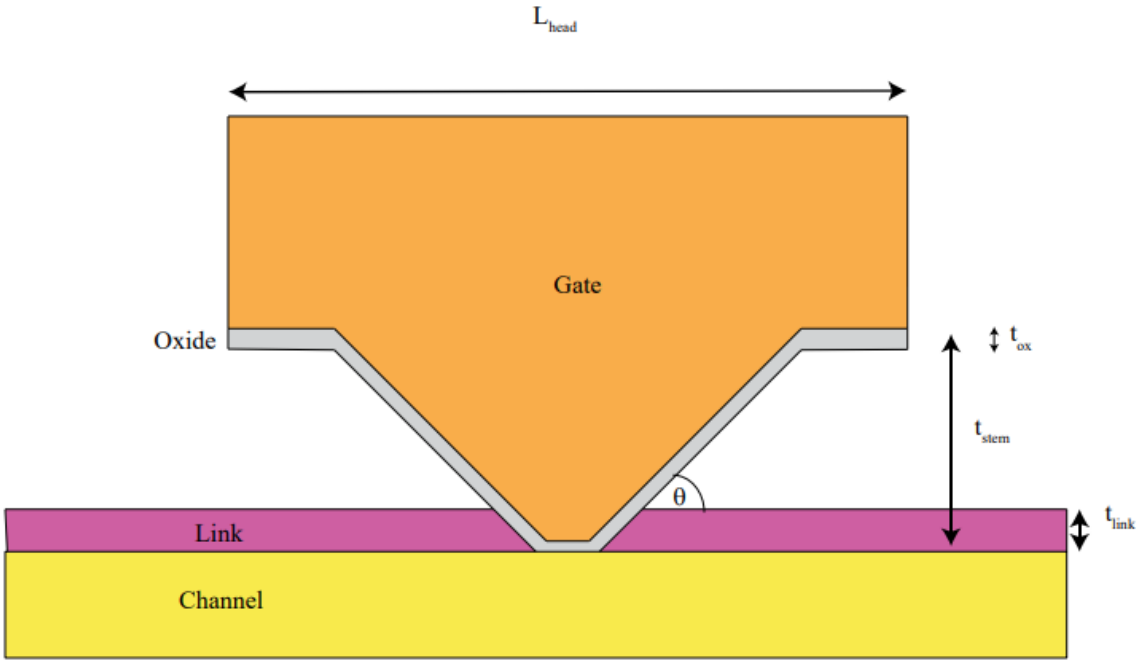


Figure 2.8: Illustration of self-aligned MOS-HEMT gate-link overlap

To further minimize capacitance, it would be advantageous to thin the topside link layer; however, aggressive scaling of the link region would require shrinking, or removing, the topside spacer. As previously mentioned, this would increase the total source resistance. Because f_τ is dependent on both gate-source capacitance and extrinsic transconductance, and by extension source resistance, both must be considered when designing the optimal link thickness.

First, the link thickness's effect on end capacitance was explored by using an HFSS model. Because HFSS is an electrostatic simulator and not a quantum simulator, band diagrams have no effect on the charge distribution in the materials. The channel (yellow) and gate (orange) are treated as metals because they are populated with mobile charge, and the oxide (grey) and link (purple) are treated as insulators because they should be depleted of charge.

The model simulated the total capacitance of the structure for a certain gate length and link thickness. To find the end capacitance, the gate length is varied from 10 nm to 50 nm and the total capacitance is plotted as seen in Figure 2.9 below.

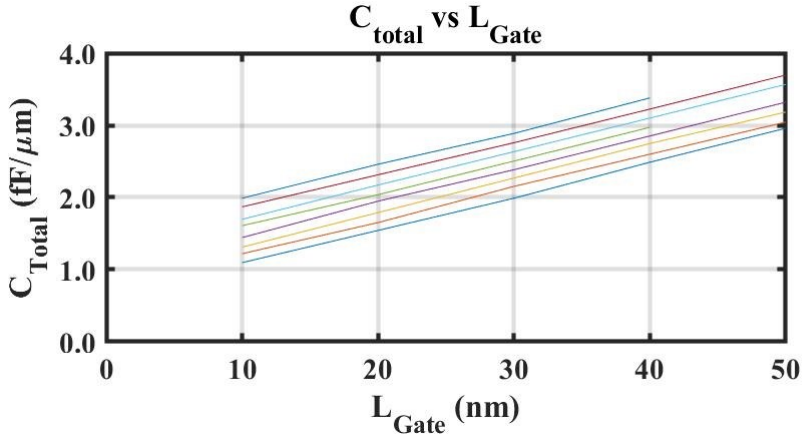


Figure 2.9: Total capacitance vs gate length for different link thicknesses

From here, the y-intercept of each line was estimated to be the total end capacitance and when divided by two, estimated to be the end capacitance for the source side. When plotted vs gate length, as in Figure 2.10, a strong linear relationship between link thickness and end capacitance is exhibited.

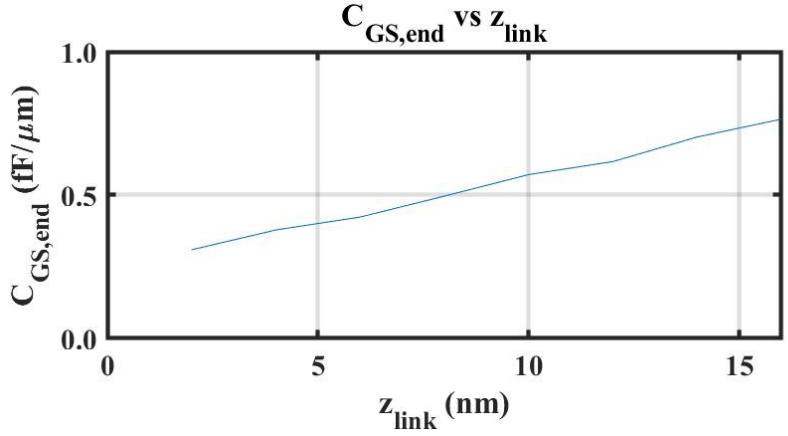


Figure 2.10: End capacitance vs link thickness graph

While $C_{GD,end}$ is also expected to shrink as $C_{GS,end}$ does, a conservative estimate of total gate-source and gate-drain capacitance can be made by simply subtracting the total benefit in $C_{GS,end}$ from the previous total capacitance.

Table 2.1: Predicted change in total capacitance for a 4 nm thick link

	Gen 1.3 MOS-HEMTS Thick link (~16 nm)	Gen 2 MOS-HEMTS Thin link (~4 nm)
$C_{GS,i}$ (fF/μm)	0.3	0.3
$C_{GS,end}$ (fF/μm)	0.7	0.3
C_{GD} (fF/μm)	0.3	0.3
C_{Total} (fF/μm)	1.3	0.9
ΔC_{Total}		-31%

Next, the dependence of source resistance on link thickness was explored experimentally. The source resistance can be broken down into components and be added up

piecewise. For simplicity, these will be combined into terms that vary with link thickness and those that do not. Terms that don't vary with link thickness come from resistance in the metal, the N+ contact layer, and any contact resistance and can be written as a constant R_C. The only term that will vary with link thickness is R_L.

$$R_L = R_{Sheet} * L_{sg} = \frac{L_{sg}}{q\mu_{link} * n_{link}} \tag{2.47}$$

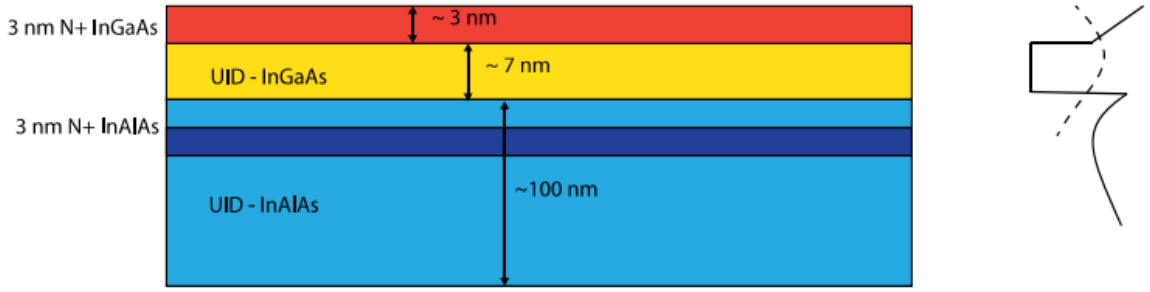


Figure 2.11: Illustration of proposed link design and approximate band diagram

The proposed 3 nm N+ InGaAs topside link, seen in Figure 2.11, was compared to previous work in the group that utilized a 16.5 nm delta-doped InP topside link. Total sheet resistance fell dramatically, in part due to the reduction in mobility. More significant was the drop in charge due to the smaller band offset between InGaAs and InAs than InP and InAs. Additionally, the InP link utilized a thick undoped layer above the delta doping to induce additional charge in the channel via the lever rule.

Table 2.2: Predicted change for total source resistance and its effect on extrinsic transconductance

Link	16.5 nm thick InP	3 nm thick InGaAs
Sheet resistance (Ω/sq)	173	654
R_L (Ω *μm)	8.65	32.7
R_C (Ω *μm)	90	90
R_S (Ω *μm)	98.65	122.7
g_{mi} (mS/μm)	4	4
g_{me} (mS/μm)	2.87	2.68
g_{me} % change	0%	-7%

Assuming the source resistance components not dependent on link thickness stay the same, total R_S increases from about 100 Ω*μm to 120 Ω*μm based on this design change. By utilizing the known intrinsic transconductance from previous MOS-HEMTs, the extrinsic transconductance can be estimated as well as its total degradation.

By examining percent change in capacitance and transconductance based on link thickness, a rise in f_τ is predicted for a thinner link region.

$$f_\tau \approx \frac{g_{m,e}}{2\pi\left(C_{gs}+C_{gd}\right)} * \frac{\downarrow 7\%}{\downarrow 31\%} = \uparrow 34\% \tag{2.48}$$

3. RF Testing and Small Signal Modeling

In this chapter, RF calibration, testing, de-embedding, and modeling will be discussed. For devices that showed promising DC characteristics, DC-67 GHz S-parameter testing was performed as described in section A (DC-67 GHz OSLT). A simple circuit model was then extracted as described in section B (Model Extraction). For device results presented in this work, more complex circuit models were used in Keysight Advanced Design Systems (ADS) and presented in their respective results section.

A. DC-67 GHz OSLT

For the DC-67GHz testing, a 2-port VNA (Keysight N5227B) was used along with a Keithley 2602A source for biasing the gate and drain. The probes used were cascade infinity probe by form factor with a 75 μm pitch and connected to the system using 24" 67 GHz semi-rigid cables. The VNA was connected to a computer via ethernet to control the testing setup. The setup was controlled via WinCal during calibration and setup and by a python script during device measurement. IF Bandwidth used was 300 Hz, power was -25dBm, averaging was 3, and frequency range was 500 MHz to 67 GHz with 250 MHz steps.

Devices that showed promise during DC testing would initially be tested from DC-67 GHz using off wafer calibration standards. A 104-783 W-band Impedance Standard Substrate is used with Open-Short-Load-Thru (OSLT) calibration to move the testing reference plane to the tip of the probes.

Once the reference plane is at the probe tip, open and short structures are tested. First, the "Open" is used to remove the capacitance from the device under test (DUT) and from the "Short".

$$Y'_{DUT} = Y_{DUT} - Y_{Open} \tag{3.1}$$

$$Y'_{Short} = Y_{Short} - Y_{Open} \tag{3.2}$$

Next, the inductance can be removed from the DUT after converting from Y parameters to Z parameters.

$$Z''_{DUT} = Z'_{DUT} - Z'_{Short} \tag{3.3}$$

The resulting Z''_{DUT} are the device characteristics with pad effects removed. Short-Open de-embedding is also used in this work, but results in higher FOM and noisier data, and is therefore ignored.

B. Model Extraction

For simple automated extraction of small signal circuit parameters, a simple FET model is used [17]. This model removes several important FET parameters, most notably source resistance. Without the inclusion of source resistance, g_m, g_{ds}, C_{gs}, and C_{gd} take on a new meaning referred to in this work as "extrinsic" usually denoted with a subscript 'e' or 'x'. Extrinsic small signal characteristics are used because they are a direct linear fit of real and imaginary parts of admittance parameters at peak bias conditions. This allows for easy and repeatable model extraction for plotting data against gate length.

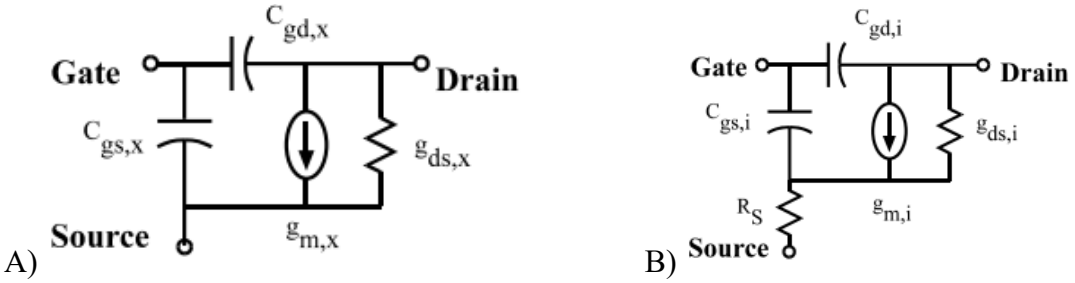


Figure 3.1 Equivilent circuit for A) extrinsic model B) intrinsic model

$$Y = \begin{bmatrix} j\omega[C_{gs,x} + C_{gd,x}] & -j\omega C_{gd,x} \\ g_{m,x} - j\omega C_{gd,x} & g_{ds,x} + j\omega C_{gd,x} \end{bmatrix} \tag{3.4}$$

$$C_{gd,x} = -\frac{Im[Y_{12}]}{\omega} \tag{3.5}$$

$$C_{gs,x} = \frac{Im[Y_{11}]}{\omega} - C_{gd,x} \tag{3.6}$$

$$g_{m,x} = Re[Y_{21}]|_{\omega=0} \tag{3.7}$$

$$g_{ds,x} = Re[Y_{22}]|_{\omega=0} \tag{3.8}$$

To estimate intrinsic parameters, first Z-parameters must be used to estimate R_S and R_G at 0 Volts V_{DS} and a large enough V_{GS} to invert the channel. From here intrinsic parameters can be estimated.

$$\mathrm{R_S} = Re(Z_{22})|_{\omega=0} - Re(Z_{11})|_{\omega=0} \tag{3.9}$$

$$\mathrm{R_G} = Re(Z_{11})|_{\omega=0} - \frac{Re(Z_{12})|_{\omega=0}}{2} - \frac{R_S}{2} \tag{3.10}$$

$$C_{gs,i} \approx C_{gs,x}(1 + R_s * g_{m,i}) \tag{3.11}$$

$$C_{gd,i} \approx C_{gd,x} \tag{3.12}$$

$$g_{m,i} \approx \frac{g_{m,x}}{1 - R_s g_{m,x}} \tag{3.13}$$

$$g_{ds,i} \approx g_{ds,x}(1 + R_s * g_{m,i}) \tag{3.14}$$

From here, figures of merit, f_τ and f_{max}, can be estimated using the extrinsic model.

$$f_\tau = \frac{\omega(H_{21} = 1)}{2\pi} \approx \frac{g_{m,x}}{2\pi(C_{GS,x} + C_{GD,x})} \tag{3.15}$$

$$f_{max} = \frac{\omega(U = 1)}{2\pi} \approx \sqrt{\frac{f_\tau}{8\pi R_G C_{gd} + 4g_{ds}(R_G + R_S)}} \tag{3.16}$$

4. Processing

In this chapter process modules and their interactions will be discussed. Entire process flows can be found in the Appendices.

A. Overview

The meat of this thesis work was spent on process development. The goal of the project was to develop a completely self-aligned process to minimize capacitance. To achieve this, the novel double regrowth design previously developed at UCSB was reversed to implement the InP sacrificial regrowth developed at Lund university [11, 18]. To achieve minimal capacitance, the link region was thinned to the acceptable extremes of less than 5 nm. In addition, a gate last process was developed to allow for pad metal connection over mesa edges. Specific implementations of the process modules will be discussed in the chapters for each specific device.

B. Alignment Marks

The self-aligned process for MOS-HEMTs eliminates the need for gate to link alignment; however, tight alignment tolerances are still required when aligning the second regrowth to the first regrowth. This work used 100 nm gate to source and gate to drain spacing. This required aligning a "Dummy Gate" hard mask of length L_g to the middle of a "Dummy link" hard mask of length Lg + 200 nm.

It is also important to note that the devices are built in a GSG structure. This means misalignment also creates asymmetric source to gate and gate to drain spacing between the left and right devices. This can be seen in Figure 4.1 below. Variations in the spacing can

cause performance variations, most notably, source resistance and output conductance. With these two things in mind, it is imperative to minimize misalignment, preferably below 20 nm.

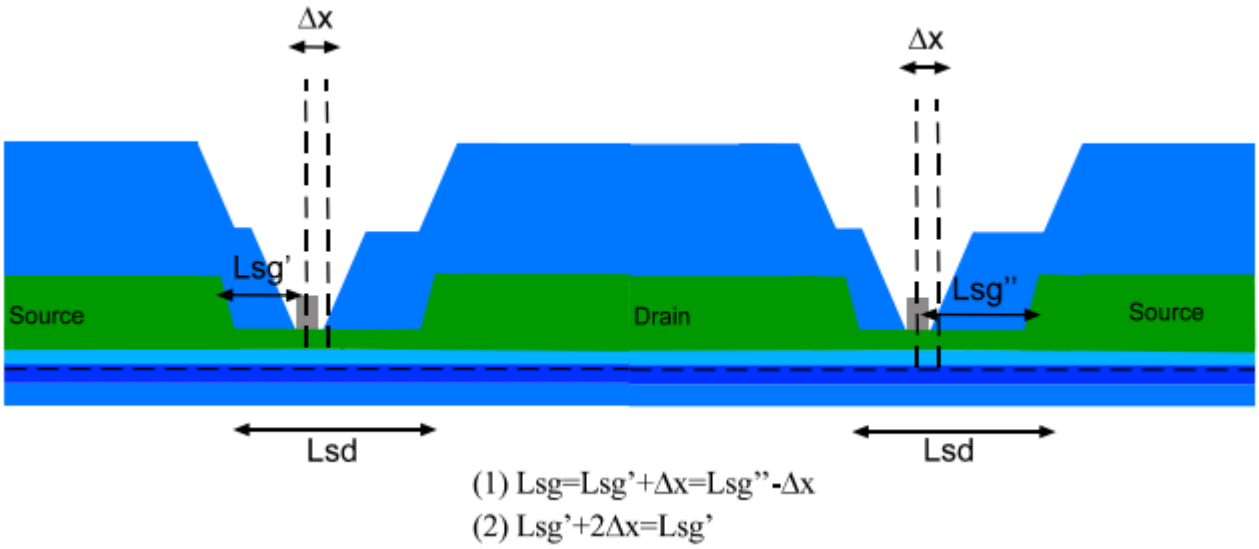


Figure 4.1: Cross-sectional illustration of device asymmetry caused by misalignment.

Good alignment marks are an important part of good alignment resolution. To make the alignment marks easier to "see" in an E-beam Lithography system, the amount of detected scattered electrons (SE) and back scattered electrons (BSE) should vary as sharply as possible at the edges of the alignment mark. This will result in a large signal to noise ratio (SNR). The level of electron scattering, and therefore SNR is most highly influenced by atomic number and step edge. Wet or dry etched alignment marks rely on step edge detection, while metal deposited alignment marks can also have the benefit of Z-contrast.

Variance in atomic number, also known as Z-contrast, is easily obtained by depositing metal alignment marks with large atomic numbers such as Tungsten, Molybdenum, Gold, Ruthenium, or Platinum [19]. Unfortunately, later regrowths in the MOCVD system limit these down to refractory metals that have high evaporation temperatures and can only be deposited via high energy processes such as sputtering or E-beam evaporation. At this point in the process, the surface is very sensitive to damage that would result in high D_{it} [20]. There

are also concerns about galvanic etching issues that come along with exposed metal during processing [21]. For these reasons metal alignment marks were avoided for this work.

A step edge resulting in a variation in scattered electrons can be achieved with an etched trench in material. To maximize SNR, the trench should be as deep as allowable, and the sidewalls should be as steep as possible [19]. To get steep walls, using a dry etch is preferred, and an anisotropic profile is easily achieved by adjusting the gas flows [22]. Unfortunately, ion bombardment damaging the surface is a concern and is avoided in this work.

This work used wet etched alignment marks to remove the concerns about damage, but this has its own drawbacks. Wet etched marks have the lowest SNR of the three options because it provides no Z-contrast, and the sidewalls are sloped. To account for this, it is best to make the trench as deep as possible [19]. In this work the trenches are 1 μm deep but could be made deeper if alignment tolerance was an issue.

The second issue with wet etched Alignment marks is resist adhesion. If the resist does not adhere well to the surface, the wet etch can undercut the resist as seen in varying degrees in Figure **4.2** below. This resulting edge roughness can hurt realignment [19]. To avoid this a hard mask is used. Exact details on etch chemistries and times can be seen in the Appendices.

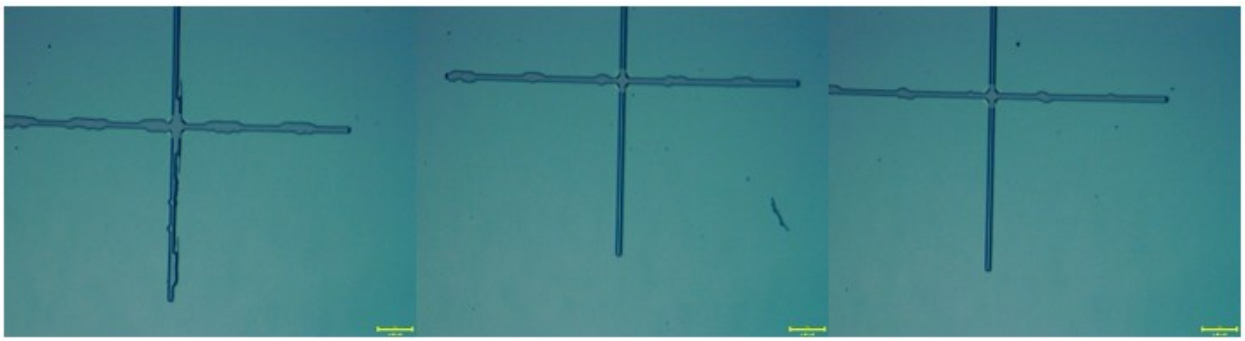


Figure 4.2: Wet etched alignment marks with poor photoresist adhesion

C. Lithography

Optical Lithography

Previous work in the group utilized an AutoStep 200. This is an i-line step and repeat exposure tool that can achieve high resolution (≥500 nm) and/or critical alignment (≥150nm) according to its specifications. The 1000-Watt Mercury arc lamp source results in very consistent exposures and requires minimal recalibration. Under normal circumstances, this would be the preferred tool for Alignment marks, mesa isolation, metal deposition, and vias.

Due to the highly fluid nature of creating a new process, constant mask changes were desired and impractical using a masked writing system like a stepper. Because of this, the optical lithography in this process was transitioned to a Heidelberg MLA150, a direct write lithography system, early in this work. The Heidelberg has longer write times, lower resolution (≥1000 nm), worse alignment (≥500nm), and shows more variation across a single wafer and different process runs.

Positive Optical Lithography

The preferred positive resist for this work is SPR-955-0.9. When spun at 3000 rpm the resist thickness is approximately 0.9 um. A prebake of 95 ºC for 90 seconds and a post bake of 110 ºC for 90 seconds are used. A 405 nm laser, dose of 105 mJ/cm2, and defocus of -3 are used for alignment marks. A 405 nm laser, dose of 240 mJ/cm2, and defocus of -6 are used for mesa isolation and InP sacrificial removal. Samples are developed in 300-MIF for 60 seconds and rinsed in DI water for 60 seconds.

Negative Optical Lithography

For negative optical lithography, HMDS and Nlof-2020 are used. Both the HMDS and nlof are spun on at 4000 rpm resulting in a thickness of approximately 1.7 um. A prebake of 110 ºC for 60 seconds and a post bake of 110 ºC for 60 seconds are used. A 375 nm laser, dose of 340 mJ/cm2, and defocus of -3 are used for vias, ohmics, and pad metal. Samples are developed in 300-MIF for 90 seconds and rinsed in DI water for 60 seconds.

Positive Electron-Beam Lithography

For positive E-beam lithography, Surpass 4000 and UV-6 are used. Surpass 4000 is dropped onto the sample surface and left to soak for 60 seconds before rinsing the sample for 30 seconds and blow drying the sample dry using N2. This is to increase photoresist adhesion. Next, UV 6-.08 is spun on the sample at 3000 rpm and baked at 115C for 90 seconds. Consistent baking is especially important for UV-6 because it is chemically amplified. This allows for a single layer liftoff with relatively high small features, thick resist, and low doses. The UV-6 is then over-exposed in the EBL to get the desired undercut profile for liftoff. Finally, the sample is post baked at 135C for 2 minutes and developed in AZ-300MIF for 60 seconds.

Negative Electron-Beam Lithography

For negative E-beam lithography, HSQ is used. The Hydrogen Silsesquioxane (HSQ) hard masks define both the minimum achievable gate length and the gate to contact spacing. Prior to HSQ, 10 cycles of TMA+H2O-300C (~1 nm Al_2O_3) are deposited on the surface to protect the channel from contamination.

Next, the HSQ in its liquid form is diluted to 2% by volume in MIBK to reduce viscosity and therefore reduce thickness when spun on a wafer to maximize resolution [22]. The HSQ is then spun at 5000 rpm to a thickness of about 40 nm (verified by ellipsometry). Then, the HSQ is cured at 200 degrees Celsius for 2 minutes.

The E-beam dose needed is highly dependent on the resolution needed and by extension, the developer used. TMAH and TMAH containing developers can be used to decrease dose and limit exposure time but have lower sensitivity and therefore minimum feature size [22]. To achieve minimum feature size less than 10 nm a "salty" developer and a base dose of 5000 $\mu C/cm^2$ is used. The salty developer is 1% NaCl and 4% NaOH by weight in water.

The NaOH can take a long time to completely dissolve and can have an undesirable effect on development if impatient. It's recommended to stir the solution every 5 minutes until it appears dissolved and then wait an additional 5 minutes before developing. The beaker is also covered with a watch glass to avoid evaporation and maintain constant concentration.

The sample is developed for 1 minute before being carefully placed in deionized water. Agitation should be avoided at all times because the HSQ can easily delaminate. After 1 minute the water is replaced and the sample is left in water for another 5 minutes. What is left is essentially a porous SiO2 mask [23].

Dark field optical microscopy is used to verify the HSQ didn't delaminate and is roughly where it should be. It is difficult to see these patterns in an SEM because of the small size and low contrast, so it is not performed. Exact instructions can be found in the Appendices.

D. First Regrowth (N+ InGaAs Contacts)

Contacts are regrown via MOCVD using the HSQ as a hard mask and using a high V/III ratio gives excellent growth selectivity between the InGaAs channel and HSQ mask. To maximize device performance the resistance of this region should be minimized.

$$R_{sheet} = (q\mu_n t N_d)^{-1} \tag{4.1}$$

Because the mobility is impurity scattering limited by the large amounts of dopants, not much attention is paid to it. The critical variables are thickness and activated doping concentrations. To keep doping concentrations high it is best to keep a high V/III ratio and high temperature [24]. The channel is strained in these devices, so the maximum allowable temperature is 600 degrees Celsius. 4e19 cm-3 is the target doping concentration for this work and is verified by a 4-point probe while assuming a constant mobility of 1000 cm/(V*s).

High doping concentration is also important for contact resistance. Contact resistance is highly dependent on the tunneling probability through the Schottky barrier at the N+ to ohmic contact interface. Higher levels of doping shrink the depletion region at this interface and improves tunneling probability.

Thickness is limited by later processing and not what is limited by MOCVD regrowth. 50 nm regrown contacts are most commonly used in this work. Increasing the thickness of the regrowth makes the sample less planar and raises concerns about the second regrowth. During run RRMH-33 the contacts were increased to 100 nm and the second regrowth showed defects that appeared to affect the V-gate yield and overall device performance as seen in Figure 4.3 below.

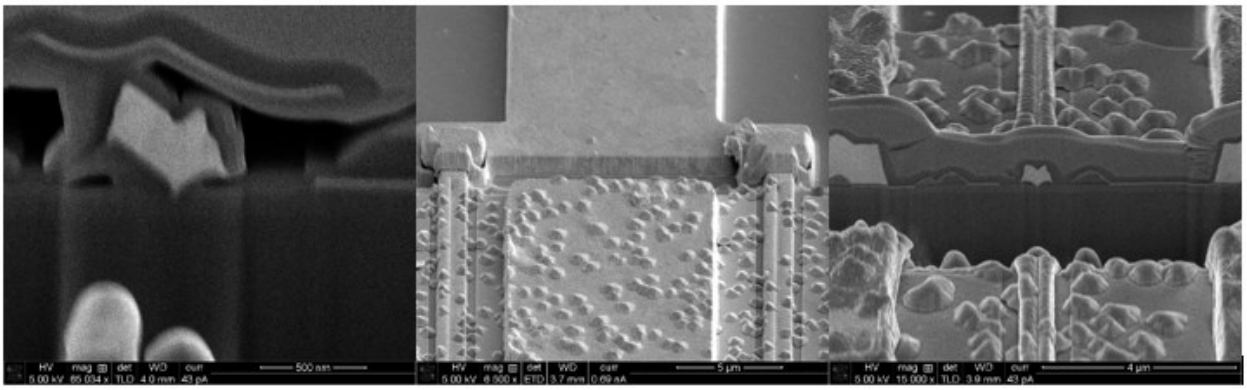


Figure 4.3: RRMH-33 angled and cross-sectional SEMs showing island regrowth.

E. Second Regrowth (Link and Sacrificial layer)

Once again, the regrowth is done via MOCVD using HSQ as a hard mask. The original idea was to regrowth both the link and the InP like in Figure 4.4 below.

Figure 4.4: Cross sectional illustration of link (pink) and sacrificial layer (blue) regrowth

Unfortunately, the TLMs showed poor end resistance for the link TLMs. Sheet link resistance ruled out concerns about doping and thickness of the link region, and good N+ contact resistance ruled out concerns about surface contamination or damage.

It is hypothesized that the non-planar nature of the sample led to the poor end resistance. The theory is the regrowth isn't perfectly conformal and there is either a lack of link doping or a lack of link material entirely in the corners near the contact region. Figure 4.5 shows the differences between the link and contact TLM structures and results.

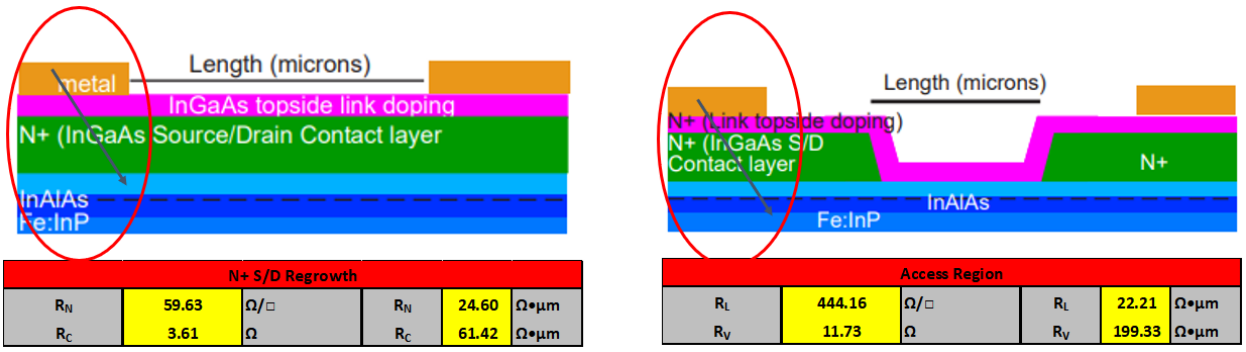


Figure 4.5: N+ contact vs link TLM structures and results

In either scenario, the election supply in these corners would be lower than intended and create a barrier to electrons that would increase the end resistance of these structures.

A specific growth experiment including SIMS and TEMs would be necessary to verify this theory and falls out of the scope of this work. To avoid this issue, the link was grown as part of the epi structure. The final design of the process still utilizes a UID-InGaAs regrowth prior to the InP regrowth to ensure the channel is fully protected during the sacrificial etch. Figure 4.6 shows the final design of the first regrowth (a) and second regrowth (b).

Figure 4.6: Cross sectional illustration of sacrificial layer (blue) regrowth

The thickness of the InP regrowth was 80 nm for all experiments in this work. Increasing the InP regrowth thickness is equivalent to increasing the T-gate height in a traditional RF-HEMT. Traditionally, increasing the stem height for a RF FET has been desired to minimize fringe capacitance from the gate; however, through hand calculation and simulations presented in this work, increasing stem height over 80 nm was shown to have

diminishing gains. Therefore, increasing the stem height only serves to decrease the stability of the gate in this work.

The angle of the InP regrowth is dependent on the growth facets. These can be controlled by the V/III ratio [25]. The high V/III ratio used to achieve good selectivity between the semiconductor and HSQ dielectric mask results in roughly a 45-degree angle like seen in Figure 4.7 below. Making the regrowth at a sharper angle could improve fringe capacitance by maximizing the distance between the gate and a channel but falls out of the scope of this work.

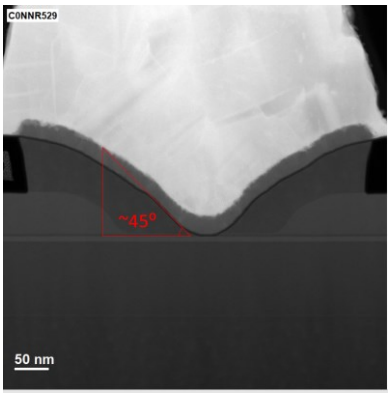


Figure 4.7: Sacrificial InP regrowth angle from RRMH-24

F. Link Etching

When the process shifted to an epitaxial link instead of a regrown link, controlled etching through the link became imperative for precise channel thickness control. In traditional InP HEMTs, the link recess etch is controlled by an etch stop [26]. This wasn't possible in this work because this would add to the thickness of thickness of the link and add complexity to the material selective etches.

Instead, "digital etches" were used to etch through the link at about 1 nm/cycle. One digital etch cycle is achieved by oxidizing the samples surface using UV-ozone for 10 minutes

followed by 60 seconds of HCl diluted with DI water 1:10 [7]. The self-limiting nature of the surface oxidation results in a very consistent etch that is reproducible sample to sample.

The downside of the link etch is gate length blowout. The digital etch also etches laterally as it etches down. This results in gate lengths longer than the written dummy-gate hard mask by about 10 nm.

G. High-k Deposition

High-k to III/V interfaces are notoriously difficult because of the high defect density. Work by the Rodwell and Stemmer group was done to develop a low defect interface between both ZrO_2 and HfO_2 and InGaAs via Atomic Layer Deposition in an Oxford FlexAl ALD system [27, 7]. The work presented in this thesis focused on ZrO_2 to minimize process complexity. The high-k deposition is as follows:

1. Removal of damaged / contaminated surface by digital etching
2. 15 cycles of CH3-TMA+100W/N*-300C for chamber preparation
3. Native oxide removal by BHF
4. Immediate loading onto a seasoned carrier wafer in a seasoned chamber
5. 9 cycles of CH3-TMA+100W/N*-300C
6. 30 cycles of CH3-TEMAZ+H2O-300C
7. 30 minutes of H2 annealing at 350C

Step 1 of the process is achieved the same as described previously in the link etching section. Careful attention is given to the channel surface during previous process steps to minimize any defect inducing damage; however, D_{it} is further reduced by at least 2 digital etches [9]. Step 3 completely removes the native oxide and provides a temporary atomic hydrogen barrier during transportation to the ALD [28].

To minimize any cross contamination from other material depositions, 15 cycles of the "CH3-TMA+100W/N*-300C" recipe is run with just the carrier wafer prior to the BHF dip. The TMA+100W/N* recipe consists of alternating N2-plasma and TMAl (trimethel aluminum) dosing at 300C resulting in about 1 Å/cycle of AlO_xN_y. This also has the added benefit of gettering the oxygen in the chamber to minimize its presence during the actual deposition. The sample is then loaded into the chamber as quickly as possible after the BHF dip to minimize any collection of oxygen.

Step 5 is achieved using the same recipe as in step 2 for the purpose of passivating dangling surface bonds to reduce defect states at the interface. Next, 30 cycles of alternating H_2O and TEMAZ (tetrakis(ethylmethylamido)zirconium) are used to deposit ~0.7A/cycles of ZrO_2. In step 7, dangling surface bonds are further passivated by a 30-minute in-situ anneal at 350C in H_2 [21]. Reducing cycles of ZrO_2 can improve C_{ox} but has a negative effect on breakdown [11]. Because of this, passivation and high-k cycles are left at 9 and 30 respectively.

H. V-Gate Deposition

In traditional RF-FETs, gate formation is a complicated process including tight alignment tolerances, multiple resist layer, and multiple exposures [26]. Changing from a T-gate to a V-gate reduces the number of resist layers and exposures to one. In addition, acceptable misalignment is increased from ~10 nm to over 50 nm. V-gate formation can be seen pictured below in Figure 4.8.

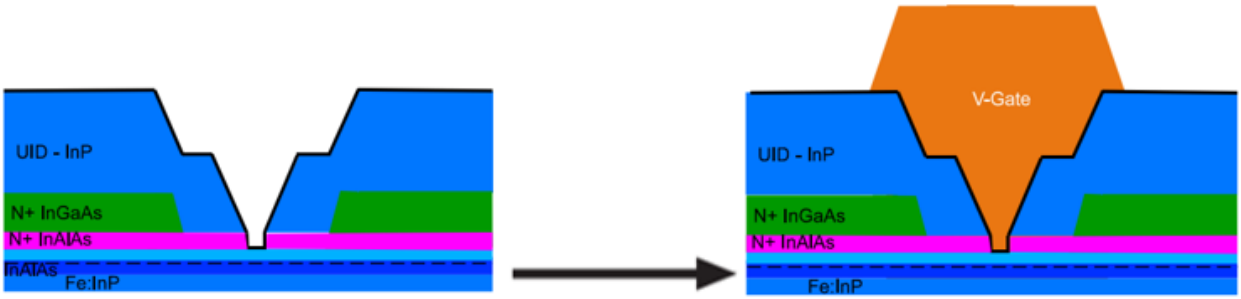


Figure 4.8: Illustration of gate formation cross section

The inclusion of the high-k adds complication for metal depositions because these can be high energy processes that add damage and increase D_{it} in the high-k. Work at UCSB has shown that thermally evaporated gates and non-plasma ALD gates provide acceptably low D_{it} [20].

Unfortunately, the only metal to be deposited via non-plasma means in the ALD at UCSB is Ruthenium. Ruthenium is notorious for galvanic etching issues because of the large difference in work function compared to gold. The large work function difference creates a local battery effect that can cause the Ruthenium or materials around it to etch in unexpected ways [21]. For this reason, thermally evaporated gates are focused on in this work.

The thermally evaporated gate metal stack at UCSB has been Ni/Au for two reasons. First, Nickel is used because it is sticky and has a work function close to Au. Second, gold is used because it is inert and has a high conductivity.

The thermal evaporator available at UCSB is not a pocket source, which means that different materials must be deposited from different locations below the sample. The sample is below the Nickel as best as possible because it is the first metal deposited and is most crucial for complete gating. Two gold sources are positioned 2.75 cm away on either side of the Nickel. With the sample 17 cm above the source, we get a 9.2º angle of acceptance. This high angle can result in buildup of gold on one edge of the gate that creates a shadowing effect on

the stem, resulting in a void in the gate. To alleviate this issue, the stage is raised from 17 cm away from the source to 39 cm away from the source. This decreases the angle of acceptance to 4.2º and reduces the shadowing effect.

The deposition rate for such an evaporation is proportional to the surface area of the sphere the sample is on where the radius is the distance from the source to the sample. The surface area grows as r^2 so increasing the radius from 17 cm to 39 cm reduces the expected deposition rate by about 5x and must be accounted for during metal deposition. Filling T-gates in this thermal evaporator set-up was previously an area of concern that was largely mitigated by the V-gate.

I. Gate Side Walling

Early process runs were plagued by parasitic Nickel gate etching as seen in Figure 4.9. To protect the Nickel during later etches, the gate is side walled with PECVD SiN [29, 21]. This is accomplished by depositing SiN via PECVD at 250º C. This is followed by a CF_4/O_2 dry etch. The dry etch is highly anisotropic because the formation of fluorocarbons on the sidewalls creates an unreactive surface [22].

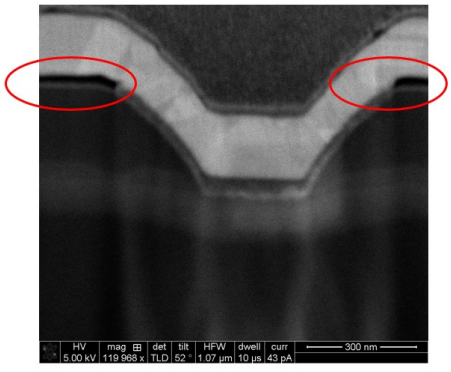


Figure 4.9: FIB/SEM cross section of device with Nickel gate etching

The exact avenue of the Nickel etching is unclear; however, there are several theories. The inclusion of the SiN sidewall eliminates the parasitic Nickel etching, so it is hypothesized that the high-k etch in BHF before the SiN is not the culprit. This leaves three main concerns.

The first concern is the HCl used for the sacrificial InP etch. HCl should only etch Nickel oxide, not elemental Nickel. To do so, one would add some type of oxidizing agent such as Nitric Acid; however, some claim empirical evidence that the oxidizing agent is not needed.

The second concern is the H_3PO_4:H_2O_2:H_2O 1:1:25 Arsenic etch used during mesa isolation. Some claim that H_3PO_4 can etch Nickel [30]. The difference in the work functions between Nickel and Gold could theoretically create a local battery effect that could etch the Nickel in the presence of phosphoric acid.

The third and final concern is the NMP (N-Methyl-2-pyrrolidone) solvent used to remove resist several times throughout the process. Some suggest that as the water content in NMP rises through extended heating, materials such as Nickel could be attacked [31]. Because of this, leaving samples in NMP overnight is not recommended. Furthermore, using heated baths is not recommended because of the potential for water spilling into the beaker by clumsy operators.

Regardless, no gate metal issues appeared after the inclusion of the SiN sidewall process, so no further investigation was warranted.

J. Sacrificial Etch

Using InP as a sacrificial support structure to be removed by HCl was inspired by the work done at Lund university by Mikael Egard *et al*. This process was a single regrowth process that can be loosely seen in Figure 4.10 below.

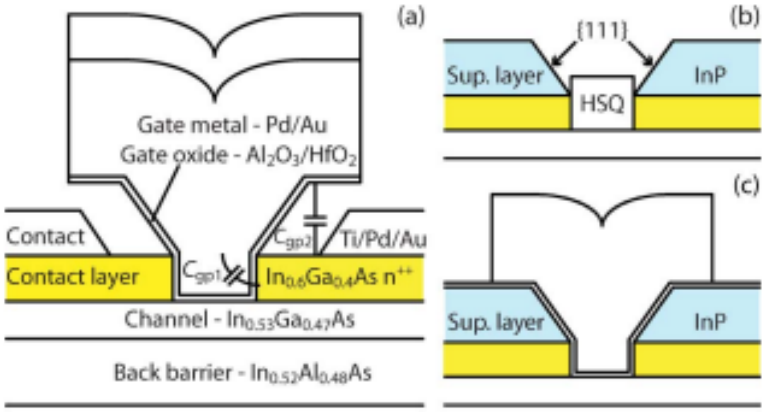


Figure 4.10: Process flow for self-aligned DC FETs by Egard *et al* [32]

The advantage of the Lund process is its single 30 nm InGaAs regrowth is highly resistant to the HCl etchant [18]. This allows for long etch times on the order of 10 minutes to completely remove the InP sacrificial layer without damaging the intrinsic device. Even with the large overlap capacitances resulting in CGS > 1 fF/um, this device achieves fmax of 292 GHz and ft of 244 GHz [32].

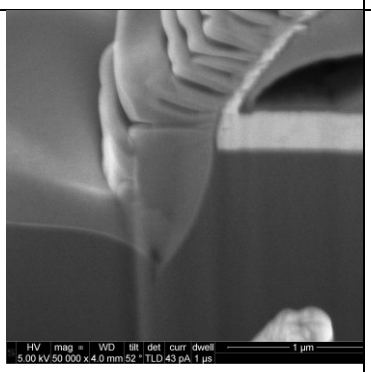
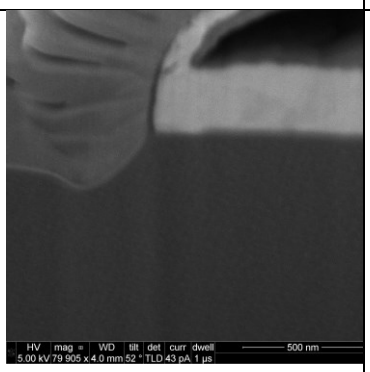
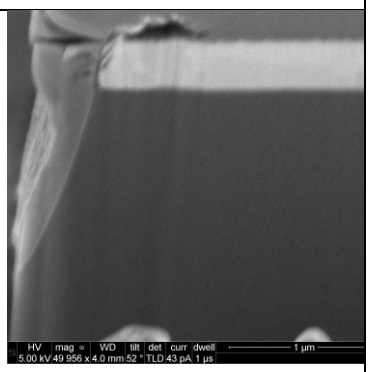
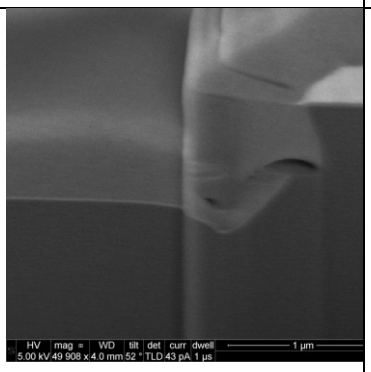
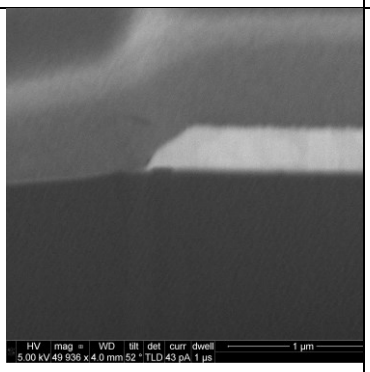
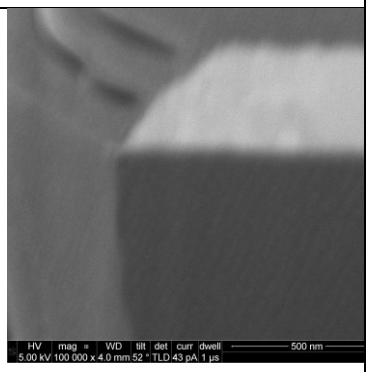
To minimize the overlap capacitance and improve high frequency performance, the regrowth etch stop must be thinned. This becomes an issue for two reasons. The first is the HCl etch is highly selective to InP over InGaAs, but not perfectly selective. This means that $In_{53}Ga_{47}As$ thicknesses on the order of 3 nm do not hold up for 10 minutes in HCl 1:1. The second issue is the highly strained $In_{80}Ga_{20}As$ channel etches quickly in HCl. This means that if the channel is exposed to HCl 1:1 at any point, catastrophic device failure occurs.

Initial attempts to etch away the sacrificial layer were unsuccessful. While InP etches rapidly in HCl 1:1 perpendicular to the surface of the wafer (the 100 direction), gate undercut etch rates are much slower. This is because the etch is highly anisotropic, meaning the etch rate is highly dependent on the crystal plane and the material the surface is bonded to [33].

The initial designs of the gates were in the $0\overline{1}\overline{1}$ and $0\bar{1}1$ directions and InP removal was not possible in times less than 10 minutes. Etch times of these lengths resulted in device failure.

Etch chemistry was initially explored as an avenue to solve this problem. Gate stacks were deposited on a blank Fe:InP substrate in the $0\overline{1}\overline{1}$ and $0\bar{1}1$ directions and etched in HCl:H_2O 1:1, H_3PO_4, and HCL: H_3PO_4 1:1 for 1 minute each. FIB/SEM cross sections were then performed to view the undercut etch rate and profile. These results can be seen in Table 4.1 below.

Table 4.1: Undercut etch profiles for different chemistries and crystallographic directions

	HCl:H_2O 1:1	H_3PO_4	HCl:H_3PO_4 1:1
$0\overline{1}\overline{1}$			
$0\bar{1}1$			

Most of the etches had a profile that sloped away from the edge of the gate and resulted in no undercutting. The only etch that showed undercut was the HCl:H2O 1:1 etch in the $0\bar{1}1$ direction at about 50 nm/minute.

From top-down SEM images it appeared that the etch might be undercutting quicker from the corners of the gates instead of the sides during the HCL 1:1 etch. To test this, the experiment was repeated with gates written in the 010 and 001 direction. This resulted in undercutting etch rates greater than 200 nm/minute. This cross section can be seen in Figure 4.11 below.

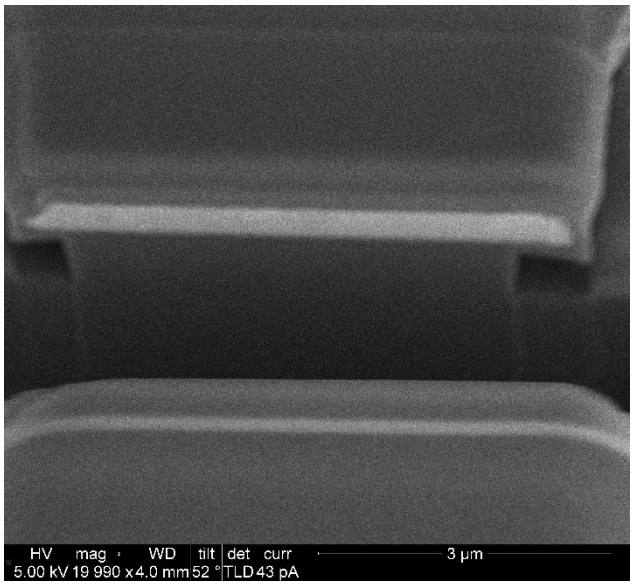


Figure 4.11: Undercut etch profile for HCl:H2O 1:1 chemistry in the 010 direction

With the guidance of these results, the main process flow shifted to gates oriented in the 010 and 001 direction and resulted in complete clearing of the InP sacrificial layer in 2 minutes without over etching the link region or attacking the channel.

K. Pad to Gate Finger Metal Breaks

After the InP sacrificial etch, the ends of the gate heads were left with a large step edge and an undercut profile that was difficult to connect pad metal over. This resulted in voids in the metal and open gates as seen in Figure 4.12 below.

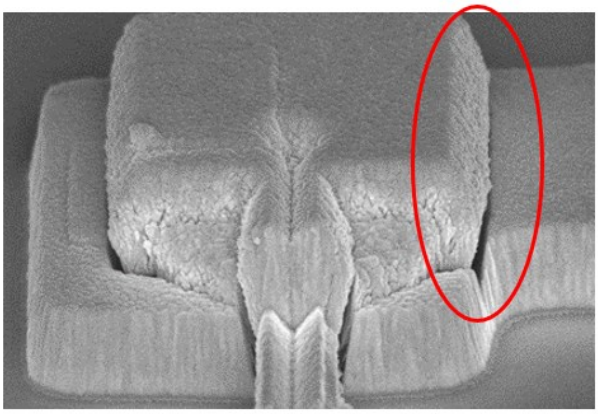
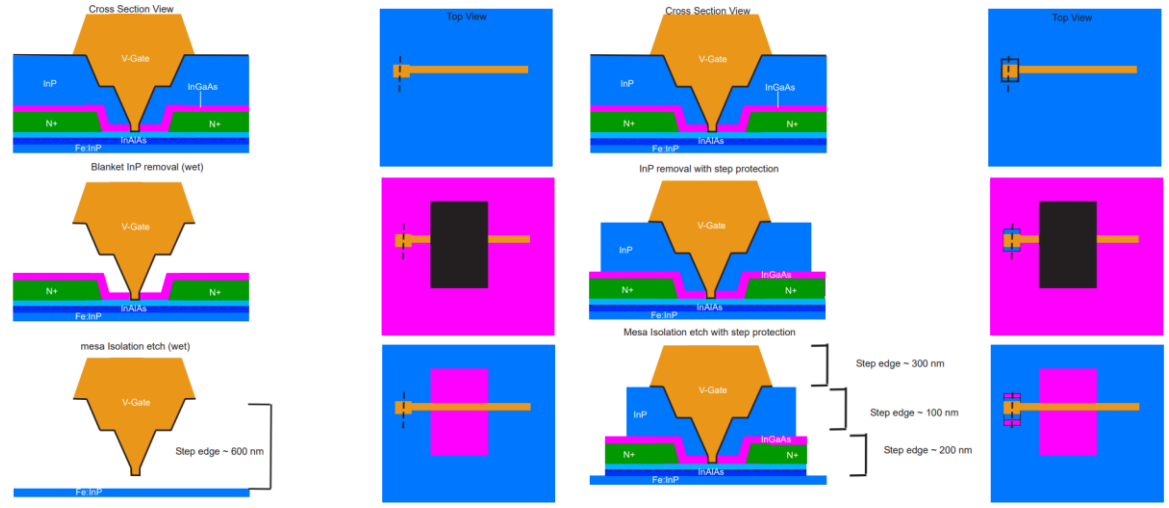


Figure 4.12: Angled SEM of gate finger to pad metal connection void

To alleviate this issue, a lithography step was added to mask the material around the ends of the gate fingers during the sacrificial etch and the mesa etch. This resulted in several small step edges with no undercut profile and fewer open gates. The top down and cross-sectional views of this can be seen before and after this change in Figure 4.13. More consistent feature shapes and sizes were achieved by integrating the InP lithography step with the SiN side walling step as seen in section I (Gate Side Walling).



(A) (B)

Figure 4.13: illustration of gate cross section outside of mesa (A) without photoresist protection (B) with photoresist protection

L. Mesa Isolation

Overview

Mesa isolation is necessary to electrically isolate devices and minimize pad capacitance, and can be achieved by dry etching, wet etching, or ion implantation. Different processing complications arise depending on if the mesa is isolated before or after gate metal deposition.

Attempting to dry etch or ion implant in a mesa first process is concerning because the channel/high-k interface is exposed. High ion energy processes can induce damage and increase the D_{it}. Dry etching in a gate first process also has complications. While the channel/high-k interface is theoretically protected from the high energy ions, The gold gate metal could be susceptible to etching and redeposition on the sample or the chamber and its undesirable. Ion implantation in a gate first process could theoretically work but would require designing new process modules and delays with vendors. For these reasons wet etching is used for both mesa first and mesa last isolation processes.

In either case, the mesa isolation etch must get completely through the 50 nm N+ InGaAs contacts, 10 nm InGaAs Channel, 106 nm InAlAs back barrier, and through the UID InP initiation layer. The Fe:InP substrate is semi-insulating because the Iron pins the fermi-level midgap, but for good quality epitaxy, a thin layer of UID InP is grown prior to the InAlAs back barrier. This layer is more conductive and results in lower RF performance. This is because coplanar waveguide capacitance increases on more conductive substrates [34].

Wet Etching

The InGaAs and InAlAs layers are etched using the "Arsenic Etch" commonly referred to throughout this thesis. This is H_3PO_4:H_2O_2:H_2O 1:1:25 stirred in a covered beaker for 10-15 minutes at room temperature. The etch rate is limited by the supply of reactants to the surface, so it is recommended to agitate the sample the entire etch to achieve a uniform etch. Previous work by Brian Markman predicts an etch rate of 2.77 nm/s for these materials [11].

The InP sacrificial layer and initial layer are etched using HCl based etches. HCl: H_3PO_4 1:4 was used at one point to attempt a more anisotropic etch to avoid undercutting, but the empirical evidence showed better results when HCl:H2O 1:1 was used. The HCl:H2O was stirred in a beaker for 10 minutes at room temperature. The mixing of HCl:H2O is exothermic, and the beaker can heat up as much as 10 degrees Celsius. Also, the etch rate of InP in HCl solutions is highly dependent on the temperature of the solution. This is because the concentration of free ions in higher at higher temperatures [35]. With these things in mind, it is important to keep the beaker, solution volume, and stir time consistent for a consistent etch rate. Previous work by Brian Markman predicts an etch rate of 8 nm/s for InP in HCl:H2O 1:1 [11].

Mesa First

Mesa first isolation has been the preferred order in the III/V MOSFET project at UCSB for the last 10 years [7, 9, 10, 11]. The main advantage to a mesa first isolation process is no metals present during the wet etching of the mesa. A common theme of this thesis is the persistence of galvanic etching issues. Isolating the mesa before depositing gate metal lowers the total time the gate metal sees any acids. It also completely prevents the gate metal from ever seeing the Arsenic etch. Initial designs utilized a mesa first process for this reason.

Unfortunately, the inclusions of the InP sacrificial layer added additional process complexity to the mesa wet etch. The first issue is adhesion. While it is not well documented or understood, this group has seen empirical evidence that photoresist adhesion to InP is much worse than to InGaAs. Because the top layer is now InP instead of InGaAs, poor photoresist adhesion results in increased mesa undercut like seen in Figure 4.14 below. Depositing a 5 nm thick ALD Al_2O_3 hard mask prior to spinning improves mesa undercutting during the first etch.

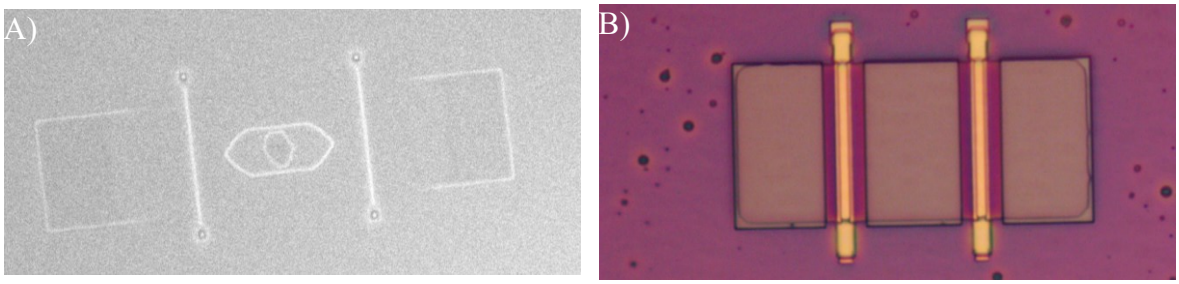
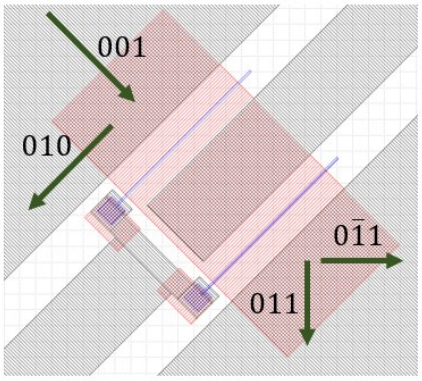


Figure 4.14: mesa undercut A) before adhesion layer B) after adhesion layer

The second major issue with mesa first isolation in the new process is difficulty connecting pad metal. At the conclusion of mesa isolation, the InP substrate is exposed. Because this is a mesa first process, the InP sacrificial layer will have to be removed later. 2 minutes in HCl result in step heights over 1 μm at the mesa edge and at the gate metal edges along with significant undercutting. This makes it extremely difficult to connect pad metal liftoff across the mesa edge and to the gate fingers. This can be seen in Figure 4.15 below.

(A) 

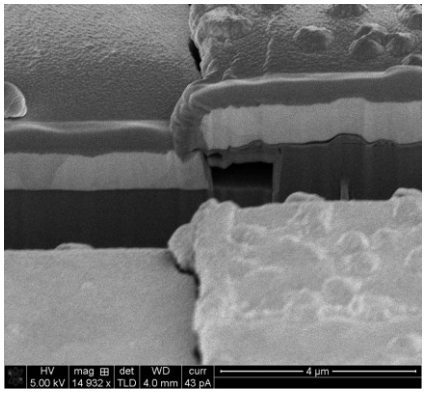
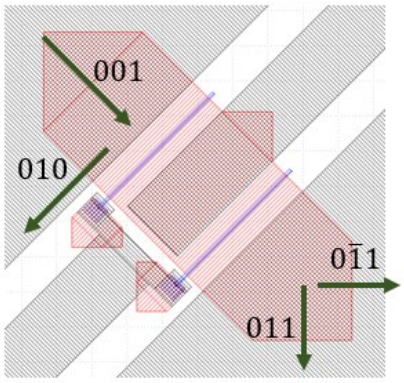
(B) 

Figure 4.15: Mesa isolation edges 1.0 (A) topdown illustration (B) cross sectional FIB/SEM

Several methods were attempted to alleviate this issue. The first method was changing the shape of the mesa to utilize the sloped mesa edges resulting from the anisotropic nature of the mesa etch along certain crystal planes. Initial tests indicated this sloped profile worked well as seen in Figure 4.16 below.

(A) 

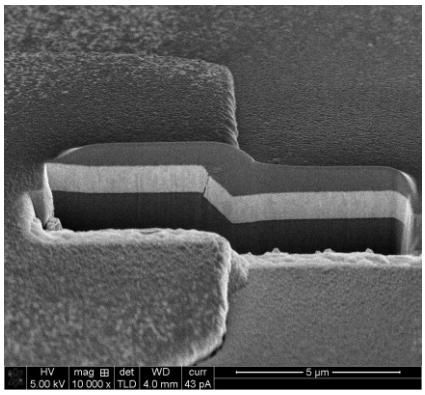
(B) 

Figure 4.16: Mesa isolation edges 2.0 (A) topdown illustration (B) cross sectional FIB/SEM

Unfortunately, this solution proved difficult to implement. Achieving this sloped profile proved more difficult as the perimeter was shrunk. This made the solution unrealistic for improving gate and drain connections as seen in Figure 4.17 below.

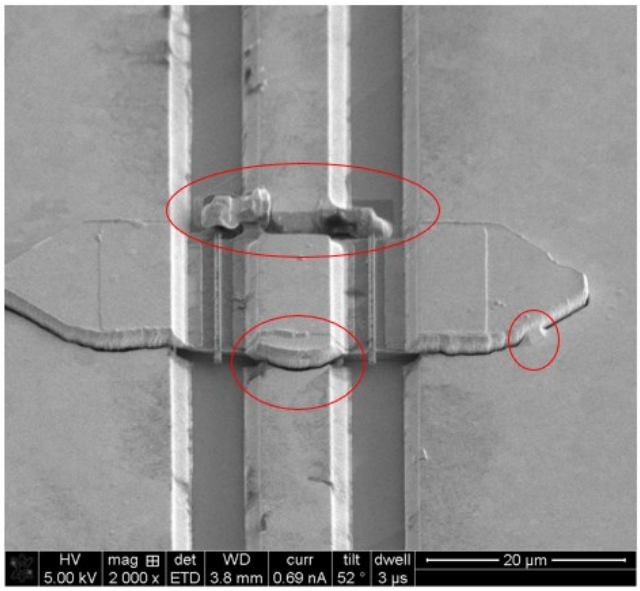


Figure 4.17: Mesa isolation edges 2.0 angled SEM

The second method utilized the InP sacrificial etch lithography step to create steps at the edge of the mesa similar to the methodology used for the gate fingers described in section K (Pad to Gate Finger Metal Breaks). This also had intermittent success because of the InP etch undercutting these features as seen in Figure 4.18 below.

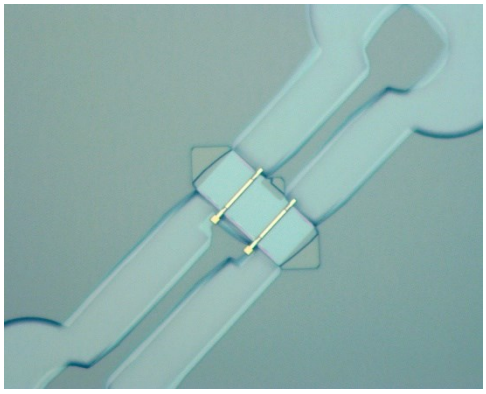
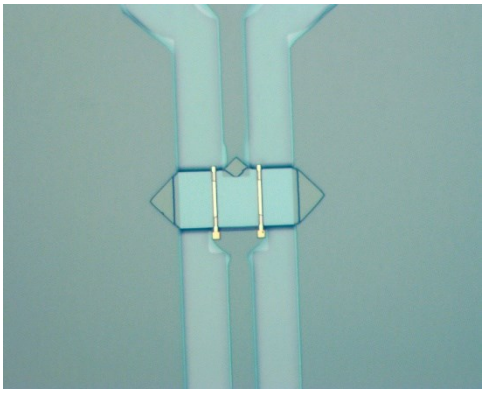
(A)  (B) 

Figure 4.18: InP etch using photomask step edges (A) 010 oriented gate (B) 011 oriented gates

Mesa Last

Mesa isolation last processes resulted in the best high frequency results. There are two key advantages to depositing gate metal before isolating the mesa. The first is the substrate is

not exposed during the sacrificial etch. This means no matter how long the sacrificial etch is, the step height at the edge of the mesa and the gate do not change. This allows for easy pad metal connections.

The second advantage of a mesa isolation last process is lower amounts of mesa undercut. First, the photoresist adheres better to the exposed InGaAs than it does the InP sacrificial layer. Second, the mesa undercut for the InGaAs is lower than for the InP. Third and most importantly, undercut compounds for each layer etched through. After a layer is etched through, the mask for the next layer is no longer the photoresist, but actually the layer that was previously etched. This means that by removing a layer from the mesa isolation etch, an avenue for mesa undercut is completely removed.

M. Source Drain Ohmics

The most important factor for ohmic contacts is contact resistance. Contact resistance is largely dependent on barrier height, barrier width, and interface traps. Barrier height depends on materials; barrier width depends on doping; and interface traps depend largely on the surface preparation. Initial processes were plagued by high contact resistance believed to stem from a poor interface.

After the inclusion of the sacrificial layer, the contact resistance went up from 6.6 Ω*μm to 43.6 Ω*μm. Because the structure was largely the same as previous designs, the interface was pointed to as the likely culprit. The theory was that an undesirable interface was left behind after the InP sacrificial layer was removed that pinned the fermi level midgap, reducing the conductivity.

Three ideas were implemented to reduce contact resistance. First, a digital etch was implemented immediately prior to loading the sample into the E-beam evaporator. The digital

etch was to remove any surface contamination, and the sample was loaded at quickly as possible to reduce the formation of a native oxide.

Second, the contact structure was changed from Ti/Pd/Au 10/10/10 nm to Pd/Ti/Pt/Au 9/15/15/15 nm based on work from Lin *et al* [36]. TEMs show Pd is highly reactive with InGaAs and is believed to reduce specific contact resistance by penetrating the native oxide. Third, the E-beam evaporation tool was allowed to pump down much longer to reach below 1e-6 torr. This should minimize the presence of oxygen during the deposition to further reduce contact resistance.

With these implementations the specific contact resistivity was reduced from 66 $\Omega^*\mu m^2$ to 12 $\Omega^*\mu m^2$ reducing total contact resistance by almost 25 $\Omega^*\mu m$. The sheet resistance of the layer is slightly increased because the thickness of the N+ contact layer is effectively reduced by the reaction with the Palladium; however, the loss in sheet conductance is far outweighed by the gain in contact conductance. A full comparison of the raw N+ TLM data and results for these two devices can be seen in Figure 4.19 and Table 4.2 respectively.

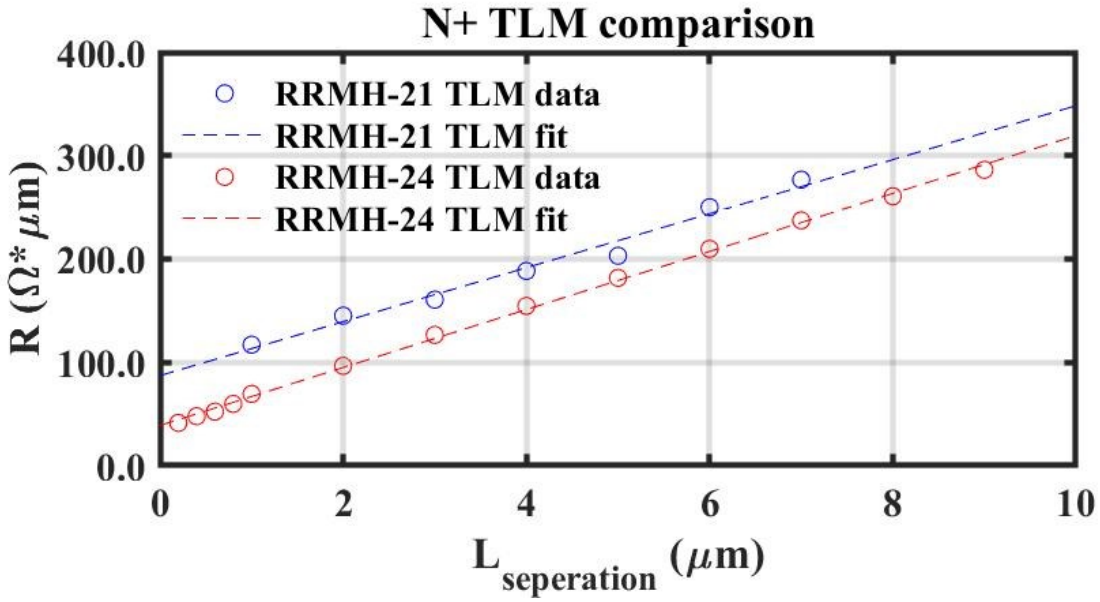


Figure 4.19: Raw N+ TLM data for RRMH-21 (before) and RRMH-24 (after)

Table 4.2: N+ TLM results for RRMH-21 (before) and RRMH-24 (after)

RRMH-21								
R_N	26.12	Ω/□	R_N	7.84	Ω•μm	L_T	1.585	μm
R_C	2.18	Ω	R_C	43.58	Ω•μm	ρ_C	65.61	$\Omega \cdot \mu m^2$
RRMH-24								
R_N	28.07	Ω/□	R_N	8.42	Ω•μm	L_T	0.658	μm
R_C	0.97	Ω	R_C	19.45	Ω•μm	ρ_C	12.16	$\Omega \cdot \mu m^2$

N. Passivation

Passivation is important in these devices to minimize sidewall leakage from dangling surface bonds. In previous III/V MOSFETs in the group, a specific passivation step was not needed. As previously discussed, the high-k process is in part to passivate dangling bonds, and in previous device iterations, coated and naturally passivated the mesa sidewalls [7, 9, 10, 11]. In this self-aligned process, the high-k gate dielectric must be removed to remove the InP sacrificial layer.

Early iterations of the process passivated before depositing ohmics. This had the benefit of using one lithography step for vias and contacts and keeping them perfectly aligned. Unfortunately, this resulted in parasitic etching of the N+ InGaAs contact layer that hurt device performance like seen in Figure 4.20 below.

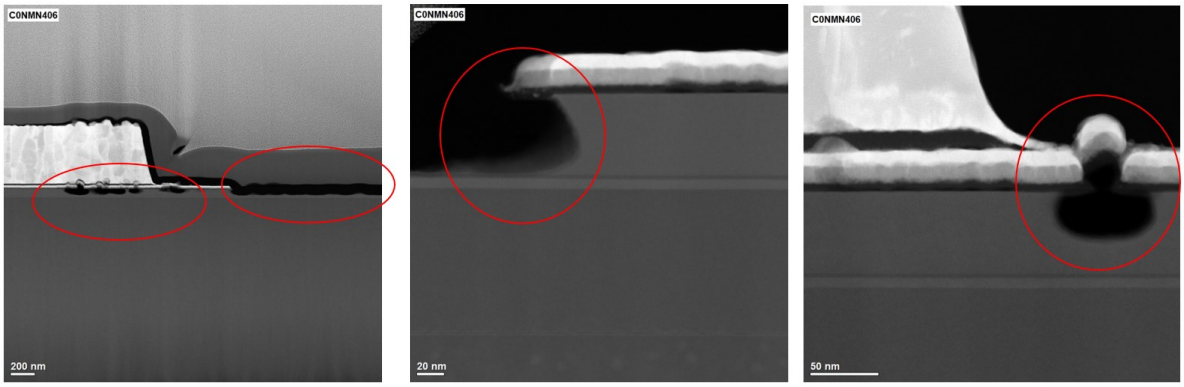


Figure 4.20: Cross sectional TEMs of paracistic etching of N+ InGaAs

Figure 4.20 shows some evidence of this etching process being masked by the ohmic contacts. This suggests the etching occurs after ohmic deposition. The only chemicals the sample sees after this point are photoresist, NMP, and 300-MIF. The obvious culprit from these chemicals is the 3% TMAH developer 300-MIF.

Previous work within the group has shown that weak bases, including 300-MIF etch InGaAs around 1 nm/minute [11]. This etching is on the order of 25 nm/min indicating some type of local battery effect. Some evidence suggests that the first layer of the passivation (AlO_xN_y) could be a source of free aluminum ions and increase the etch rate []. Also, the variation in work functions of the contacts or the gate metal could be the culprit. In an abundance of caution, and potentially paranoia, both potential galvanic sources were eliminated.

First, the passivation layer was reduced to just ZrO_2 to remove the concern of free aluminum ions. Second the passivation order was changed to contacts first, followed by passivation and vias. Also, the vias were made smaller than the contacts. This prevents the possibility of the developer ever seeing a metal other than the top metal. The top metal is always gold and is extremely inert. Removing the AlO_xN_y interfacial layer theoretically results in less passivated sidewalls; however, sidewall leakage was never revealed to be a major issue after this change.

O. Pad Metal

Pad metal lift off is accomplished in this work by optical lithography follow by E-beam deposition of Ti/Au. For robust de-embedding of S-parameters, it is important to have consistent pad metal shape and thickness. To avoid issues with liftoff it is recommended to

keep the resist 4x the thickness of the desired metal. The best results in the work were accomplished with Ti/Au 20/500 nm depositions.

Some work was done to increase the thickness and sidewall coverage of the pad metal to improve connections over tall/undercut mesa edges. Tilted evaporations were attempted to increase sidewall coverage but resulted in poor and inconsistent liftoff. To increase deposition thickness past the 1 μm system limit, the sample was moved closer to the source. This also resulted in poor liftoff. A thicker resist, nlof-2070 was used to improve the liftoff to no avail.

This work was abandoned because parallel work on mesa-last processing was a success. Further work on this should utilize a thick underlayer resist to combine the liftoff benefits of a thick resist with the resolution benefits of a thin resist.

5. Generation 2.1

This chapter will outline fabrication, design, results, and conclusions for the first successful attempt at a self-aligned regrowth reversal MOS-HEMT.

A. Fabrication

6 nm channel / spacer	UID	$In_{0.53}Ga_{0.47}As$
4 nm channel	UID	InAs
3 nm spacer	UID	$In_{0.52}Al_{0.48}As$
3 nm δ-doping	N+ (1e19)	$In_{0.52}Al_{0.48}As$
100 nm back barier	UID	$In_{0.52}Al_{0.48}As$
500 um substrate	semi-insulating	Fe:InP

Figure 5.1: Illustration of generation 2.1 MBE epitaxy

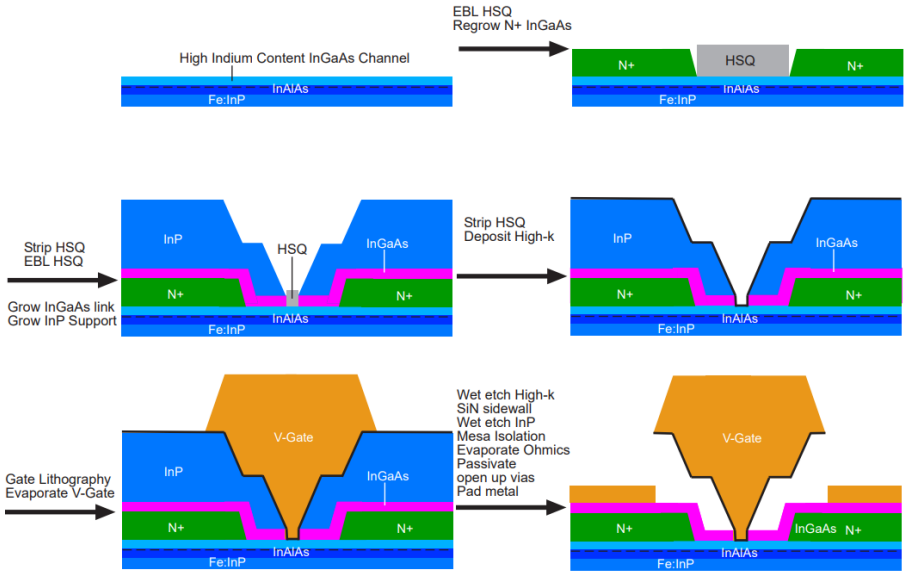


Figure 5.2: Illustration of generation 2.1 process flow.

The fabrication process started with Epi purchased from Intelligent Epitaxy and followed Figure 5.2. The layers were grown by MBE on a (100) Iron doped semi-insulating substrate. Alignment marks were define using the AutoStep 200 and wet etched as described in the Appendix. Dummy links were defined by EBL in the $0\overline{11}$ and $0\bar{1}1$ directions. 25 nm thick N+ InGaAs Source/Drain contacts were regrown in the MOCVD. After dummy gate definition, 5 nm of N+ InGaAs and 80 nm of UID InP were regrown. Source to gate and source to drain spacing was 50 nm. Regrowths resulted in 3D island growth as seen in Figure 5.3 below and had lower than expected sheet resistance as seen in Table 5.1 below.

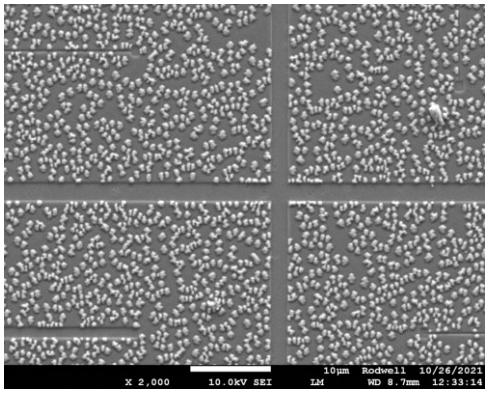


Figure 5.3: 3D island growth from regrowth

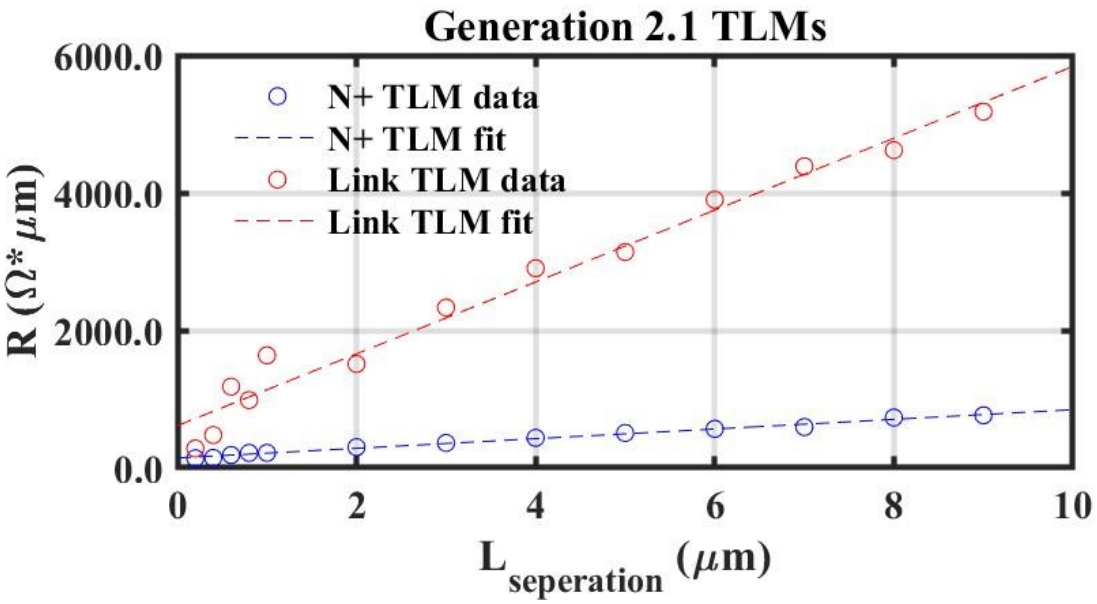


Figure 5.4: TLM plots for generation 2.1

Table 5.1: TLM data for generation 2.1

N+ (RRMH-11)								
R_N	70.15	Ω/□	R_N	21.05	Ω•μm	L_T	0.978	μm
R_C	3.61	Ω	R_C	72.25	Ω•μm	ρ_C	67.16	Ω•μm^2
Link (RRMH-11)								
R_L	522.54	Ω/□	R_L	156.76	Ω•μm	L_T	0.558	μm
R_V	15.34	Ω	R_V	306.76	Ω•μm	ρ_C	162.52	Ω•μm^2

The HSQ dummy gate was removed, and the channel was digital etched 4 times to reduce the channel thickness to about 7 nm. Next, high-k and gate deposition was performed as described in the relevant processing sections. The devices were then etched 30 seconds in HCl:H2O 1:1 for 30 seconds to remove the InP sacrificial layer followed by mesa isolation.

Source drain ohmics were defined optically and Ti/Pd/Au 10/10/10 nm was E-beam evaporated. The contact layers were kept thin in this process because some of the contacts were self-aligned. All self-aligned contacts resulted in source to drain shorts.

Devices were passivated with 50 cycles of CH3-TEMAZ+H2O-300C in the ALD. Vias were defined optically and wet etched 60 seconds in buffered HF. Pad metal was defined optically and 20 nm of Titanium followed by 500 nm of Gold were E-beam evaporated.

B. DC Results

Figure 5.5 below shows the lot DC characteristics for Generation 1 devices for 20 µm gate width devices on Die 2.

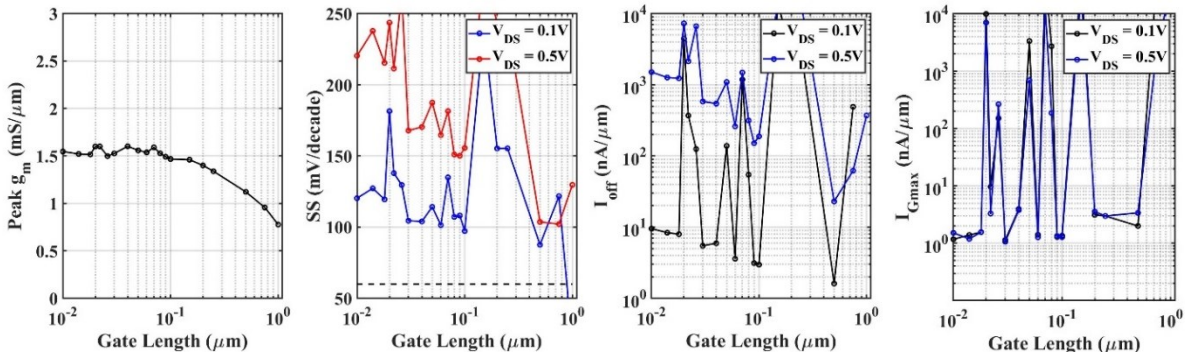


Figure 5.5: Lot DC results for RRMH-11-Die-2-Wg-20um

Devices exhibit moderate peak $g_{m,e}$ of around 1.5 mS/µm, but show inconsistent off characteristics. These yield issues appear to be caused by gate leakage as seen in the $I_{G,max}$ graph on the right. Output and transfer characteristics for a 20 nm written gate length in Figure 5.6 below further show the leaky devices are plagued by gate leakage issues.

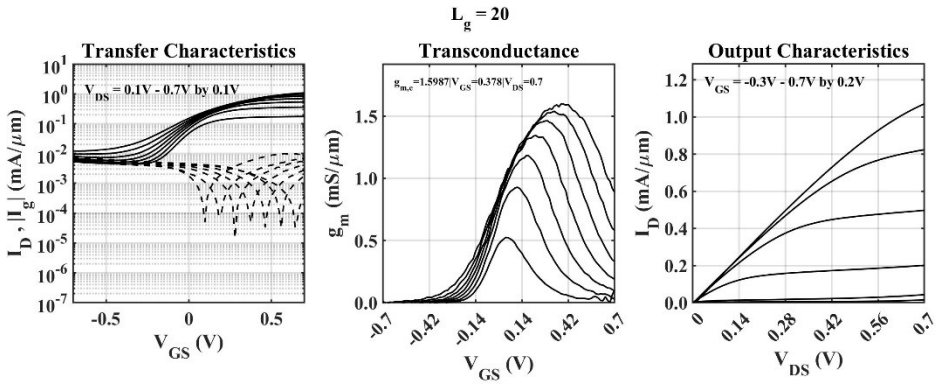


Figure 5.6: DC characteristics for generation 2.1, L_g = 20 nm, W_g = 20 µm, Die = 2

For clarity, the devices with high leakage are removed and the results are regraphed in Figure 5.7 below.

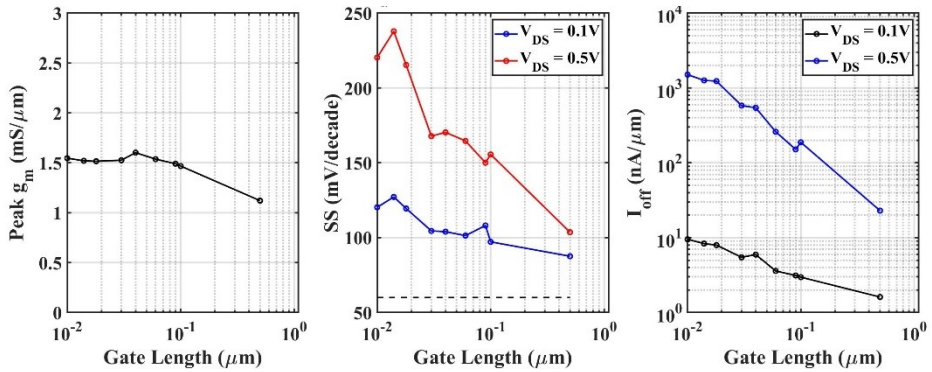


Figure 5.7: Lot DC characteristics for generation 2.1 devices, W_g = 20 µm, Die = 2 (leaky devices removed)

Here, clear trends in subthreshold slope and I_{off} can be seen. The subthreshold slope is below 100 mV/decade at the longest yielded gate length. Assuming all additional subthreshold slope beyond the thermal limit is due to defects, the D_{it} is around 1e13 cm^{-2}. I_{off} increases as gate length decreases due to reduced barrier height from short channel effects.

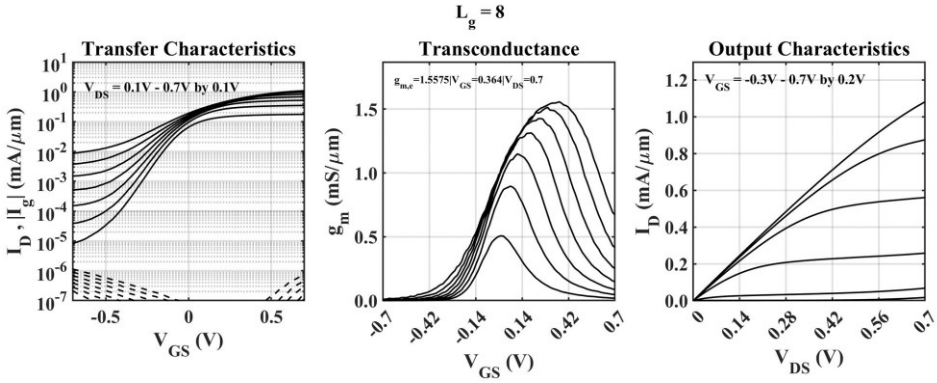


Figure 5.8: DC characteristics for generation 2.1, L_g = 8 nm, W_g = 20 µm, Die = 2

Figure 5.8 shows DC characteristics for an 8 nm device with minimal source to drain or gate leakage, moderate extrinsic transconductance, and reasonable output characteristics.

C. RF Results (Lot)

Testing is performed from DC to 67 GHz using off wafer probe tip calibration followed by on wafer open-short and short open de-embedding. As seen in Figure 5.9, both methods give similar results, so we report the more conservative results. For clarity, data de-embedded using open-short will be presented in this section.

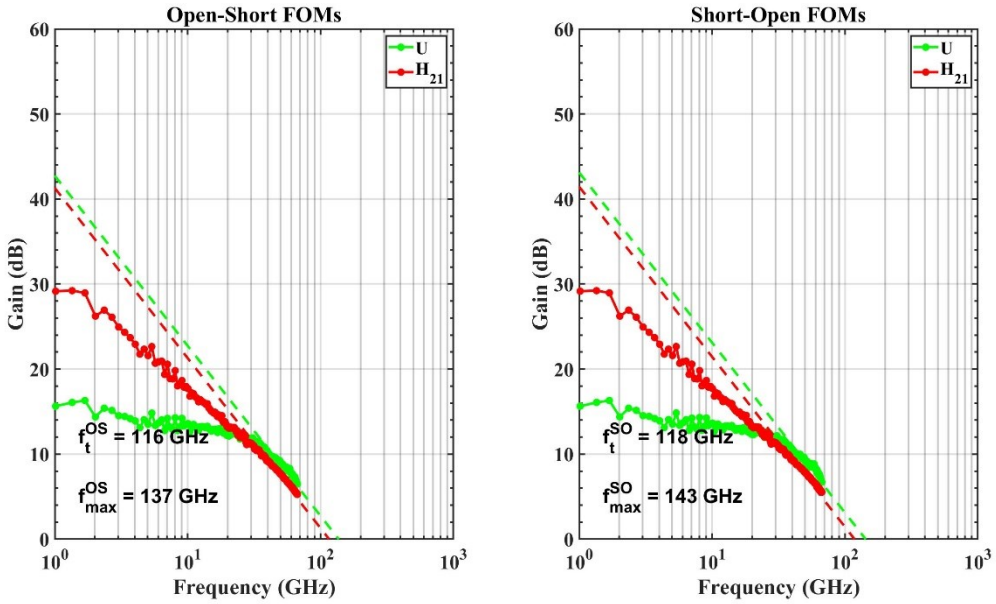


Figure 5.9: RF FOM extraction for RRMH-11-Die-2, W_g=2x20um, Lg = 10 nm, V_{GS} = 0.2 V, V_{DS} = 0.7 V

Initial de-embedding and small signal circuit extraction is performed via automation as outline in the Model Extraction section. Plotting these results vs gate length in Figure 5.10 below show high $C_{GS,e}$ and $C_{GD,e}$ greater than 1.2 and 0.6 fF/μm respectively. Transconductance is roughly cut in half compared to DC characteristics. High capacitance and low transconductance result in extremely limited f_τ ~ 100 GHz and f_{max} ~100 GHz.

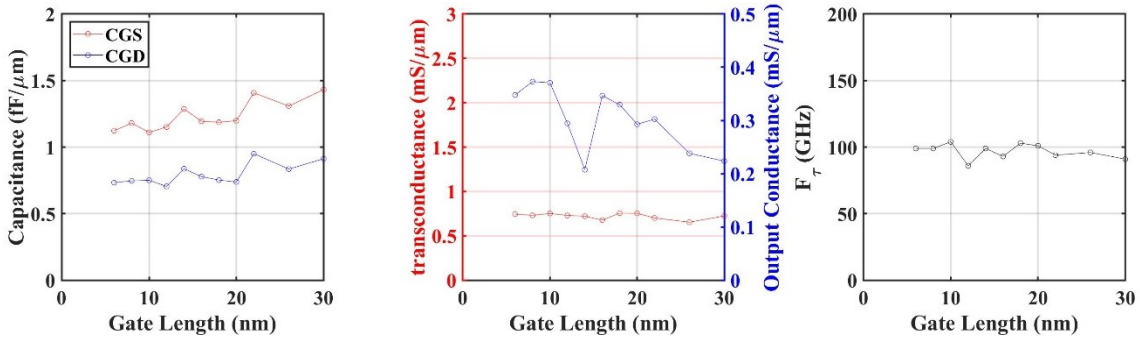


Figure 5.10: Gate length series of extracted common-source SSEC elements for RRMH-11-Die-2, W_g = 2x20 um

D. RF results, Off Wafer Calibration, DC to 67 GHz, Lg = 10 nm

Y parameters for a 10 nm device biased at V_{GS} = 0.2 Volts and V_{DS} = 0.7 Volts, DC to 67 GHz can be seen in Figure 5.11 and Figure 5.12.

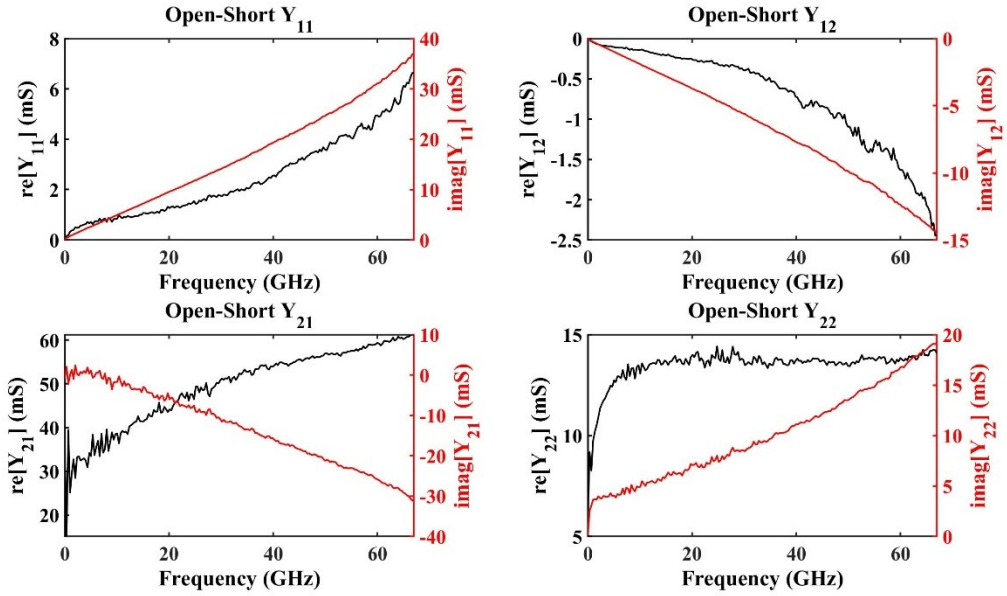


Figure 5.11: DC to 67 GHz Y-parameters with open-short de-embedding for RRMH-11-Die-2, W_g=2x20 um, Lg = 10 nm, V_{GS} = 0.2 V, V_{DS} = 0.7 V

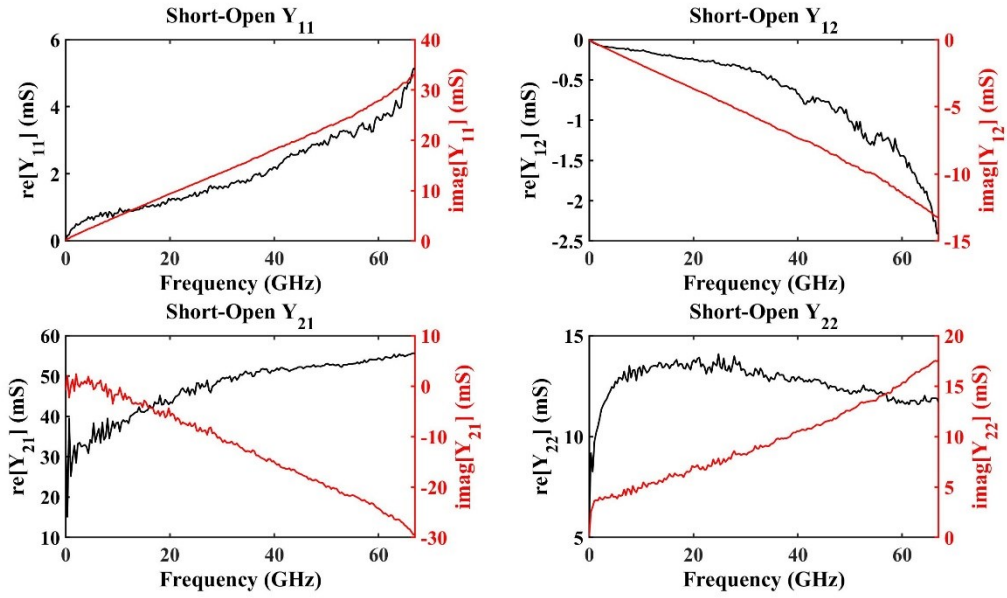


Figure 5.12: DC to 67 GHz Y-parameters with short-open de-embedding for RRMH-11-Die-2, W_g=2x20um, Lg = 10 nm, V_{GS} = 0.2 V, V_{DS} = 0.7 V

In Figure 5.13 below, the final equivalent circuit model and S parameters for the 10 nm gate length device are seen. Extraction utilizes the initial simplified circuit model followed by fine tuning the more extensive circuit model in ADS.

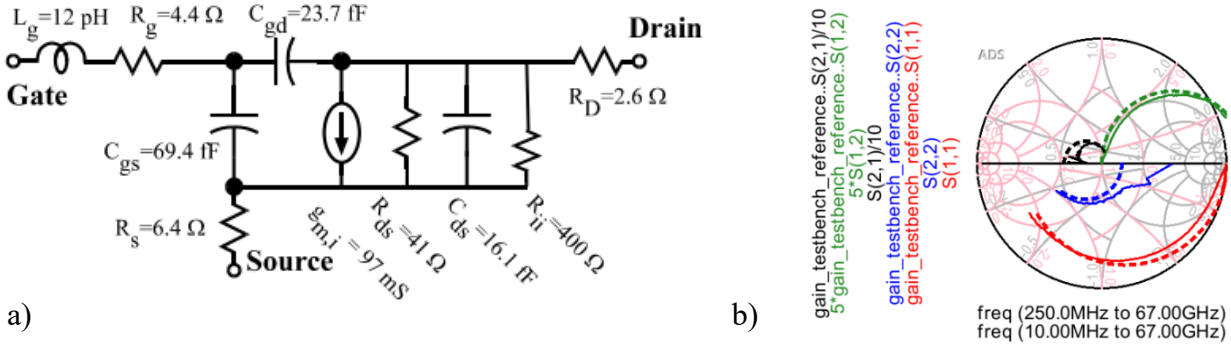


Figure 5.13: RRMH-11-Die-2, W_g=2x20um, Lg = 10 nm, V_{GS} = 0.2 V, V_{DS} = 0.7 V (a) equivalent circuit model (b) S-parameter DC to 67 GHz

E. Conclusions

Generation 2.1 was the first successful attempt at a self-aligned process but had extremely limited high frequency figures of merit. Accurate model extraction was difficult

due to unusual Y-parameters; however, there were two clear issues to address before Generation 2.2. First, high source resistance plagued these early results. High TLM end resistance was resolved going forward by ordering epi with the topside link already grown, as described in the Second Regrowth (Link and Sacrificial layer) section. Additionally, contact resistance was minimized by changing the contact stack as described in the Source Drain Ohmics section. Lastly, the N+ InGaAs contact layer sheet resistance was grown thicker in future designs to minimize sheet resistance as described in the First Regrowth (N+ InGaAs Contacts) section.

Second, various process issues plagued the early generation 2.1 process runs. The most troublesome issues involved inconsistent parasitic etching issues, usually attributed to a "local battery effect". Planning for generation 2.2 involved careful consideration of encapsulating all metals before putting samples in solutions. Additionally, fine tuning of wet etch times to minimize mesa undercut was crucial to maximize intrinsic transconductance. Finally, empirical evidence suggests that minimizing the time between the BHF dip and loading the sample into the ALD for high-k deposition can reduce D_{it}.

At this point of process development, it was believed that increasing the sacrificial etch time would be all that was needed to remove the InP support structure, so this portion of process development was saved for later.

6. Generation 2.2

This chapter will outline fabrication, design, results, and conclusions for the second generation of self-aligned regrowth reversal MOS-HEMTs.

A. Fabrication

3 nm cap	UID	$In_{0.53}Ga_{0.47}As$
3 nm link	N+ (1e19)	$In_{0.52}Al_{0.48}As$
7 nm channel	UID	$In_{0.80}Ga_{0.20}As$
3 nm spacer	UID	$In_{0.52}Al_{0.48}As$
3 nm δ-doping	N+ (1e19)	$In_{0.52}Al_{0.48}As$
100 nm back barier	UID	$In_{0.52}Al_{0.48}As$
500 um substrate	semi-insulating	Fe:InP

Figure 6.1: Illustration of Generation 2.2 MBE epitaxy

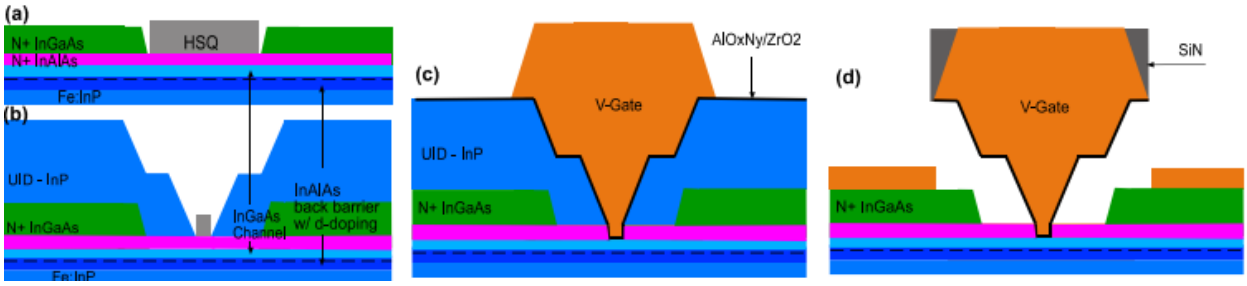


Figure 6.2: process flow (a) Epi, dummy link, contact regrowth (b) dummy gate, sacrificial regrowth (c) etch N+ link, high-k deposition, gate metal deposition (d) high-k etch, SiN sidewall, InP removal, ohmic contact deposition

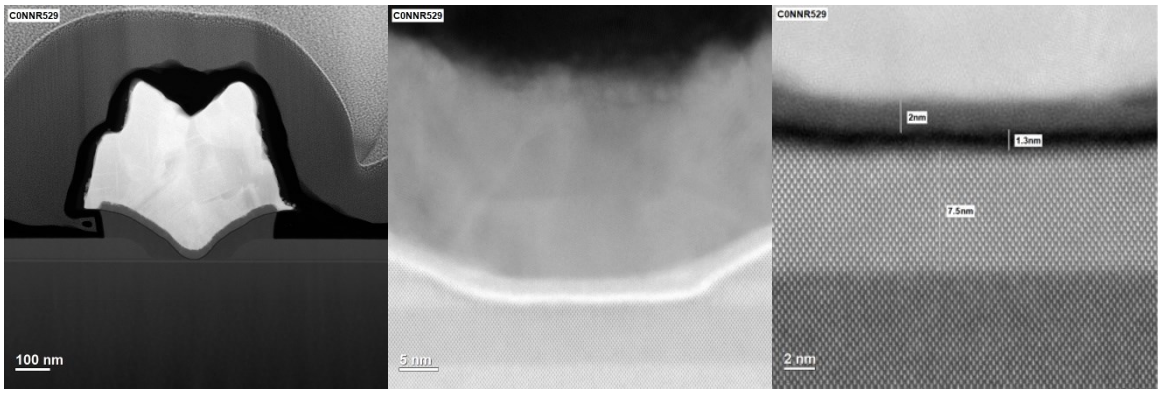


Figure 6.3: 26 nm Lg TEM cross section. (a) full device (b) gate length (c) channel + oxide thickness

The fabrication process started with Epi purchased from Intelligent Epitaxy. The layers were grown by MBE on a (100) Iron doped semi-insulating substrate. Alignment marks were defined using the MLA150 and wet etched as described in the Appendix. Dummy links were defined by EBL in the $0\overline{1}\overline{1}$ and $0\overline{1}1$ directions. 50 nm thick N+ InGaAs Source/Drain contacts were regrown in the MOCVD. After dummy gate definition, 80 nm of UID InP was regrown. Regrowths resulted in good sheet and contact resistance as seen in Figure 6.4 and Table 6.1 below.

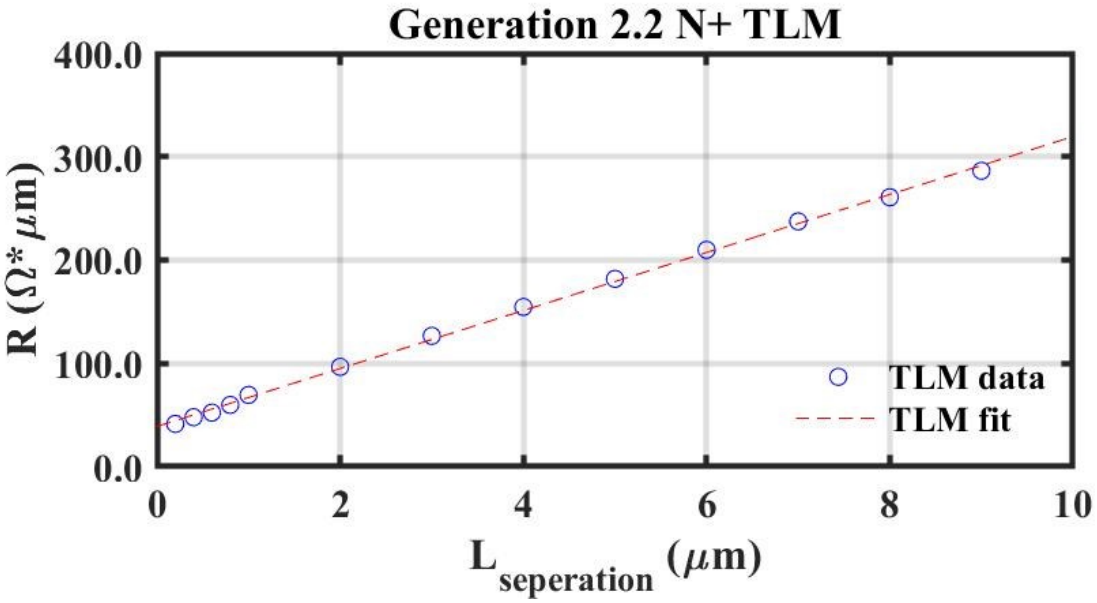


Figure 6.4: RRMH-24 TLMs for 50 nm thick N+ InGaAs

Table 6.1: RRMH-24 TLM results for 50 nm thick N+ InGaAs

RRMH-24 N+ TLM								
R_N	28.07	Ω/□	R_N	8.42	Ω•μm	L_T	0.658	μm
R_C	0.97	Ω	R_C	19.45	Ω•μm	ρ_C	12.16	$\Omega \cdot \mu m^2$

50 cycles of ALD Al_2O_3 were deposited using recipe TMA+H2O-300C as a hard mask. Optical lithography was performed to define the mesa. The sacrificial layer, contact layer, channel, back barrier, and growth initiation layer were wet etched through using BHF for 45 seconds, H_3PO_4:HCl 4:1 for 30 seconds, followed by H_3PO_4:H_2O_2:H_2O 1:1:25 for 110 seconds, and then HCl:H_2O 1:1 for 10 seconds. The H_3PO_4 diluted HCl was used instead of the H_2O diluted HCl to etch through the sacrificial layer in an attempt to minimize the mesa undercut seen during the first etch.

After mesa isolation, the HSQ dummy gate was removed, and the channel was digital etched 6 times to reduce the channel thickness to about 7.5 nm. Next, high-k, gate deposition, and SiN side walling was performed as described in the relevant processing sections. The InP protection lithography was followed by the sacrificial etched in HCL:H_2O 1:1 for 40 seconds to remove the sacrificial layer.

Ohmics were defined by E-beam lithography to minimize contact spacing followed by E-beam evaporation using Pd/Ti/Pt/Au 9/15/15/15 nm. Next, devices were passivated using 42 cycles of SiO_2 (CH3-TDMAS+250W/O*-300C) followed by a 30-minute Hydrogen anneal in the ALD system at 350 degrees Celsius. Vias were defined optically and etched in BHF for only 5 seconds to account for the fast etch rate of SiO_2. Lastly, pad metal was defined optically, and E-beam evaporated using 20 nm of Titanium and 500 nm of Gold.

B. DC Results

Figure 6.5 below shows the lot DC characteristics for Generation 2 devices for 20 µm gate width devices.

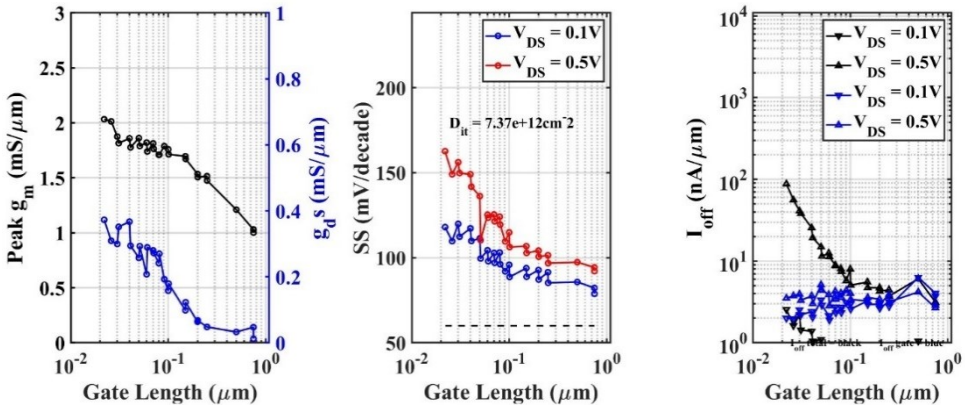


Figure 6.5: Lot DC results for RRMH-24-Die-2-Wg-20um

Peak DC transconductance above 2.0 mS/um is observed with subthreshold slope below 100 mV/decade at 1000 nm gate lengths and V_{DS} = 0.1 Volts. I_{off} < 100 nA is observed at gate lengths measured down to 42 nm at V_{DS} = 0.5 Volts, and gate leakage < 6 nA at gate lengths measured down to 42 nm and at all gate biases.

In Figure 6.6, Ron vs gate length is plotted, and the y intercept is divided by 2 to give a rough estimate of 8 Ω source resistance for these devices. 8 Ω * 20 µm yields 160 Ω*µm which is a large improvement on previous results.

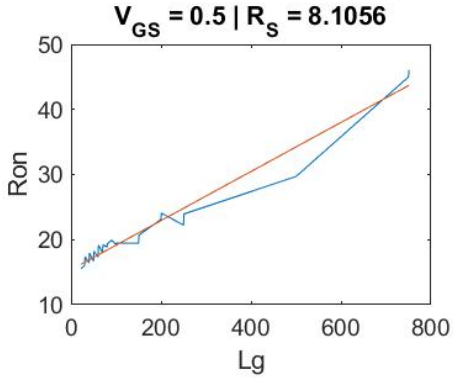


Figure 6.6: R_{on} vs gate length for RRMH-24, Die 2

The best performing device during initial DC testing was the 42 nm gate length device seen in Figure 6.7 below. This device exhibited DC extrinsic transconductance over 2 mS/um and DC extrinsic output conductance below 0.4 mS/um at peak bias conditions.

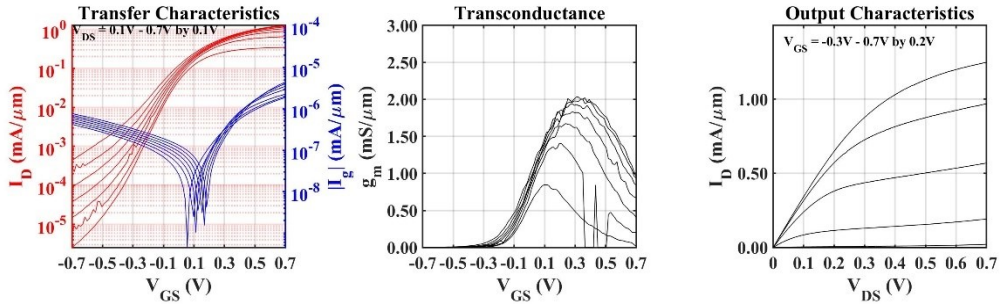


Figure 6.7: DC results for RRMH-24-Die-2, W_g=20um, L_g = 42 nm

C. RF Results (Iot)

Testing is performed from DC to 67 GHz using off wafer probe tip calibration followed by on wafer open-short and short open de-embedding. As seen in Figure 6.8, both methods give similar results, so we report the more conservative results. For clarity, data de-embedded using open-short will be presented in this section.

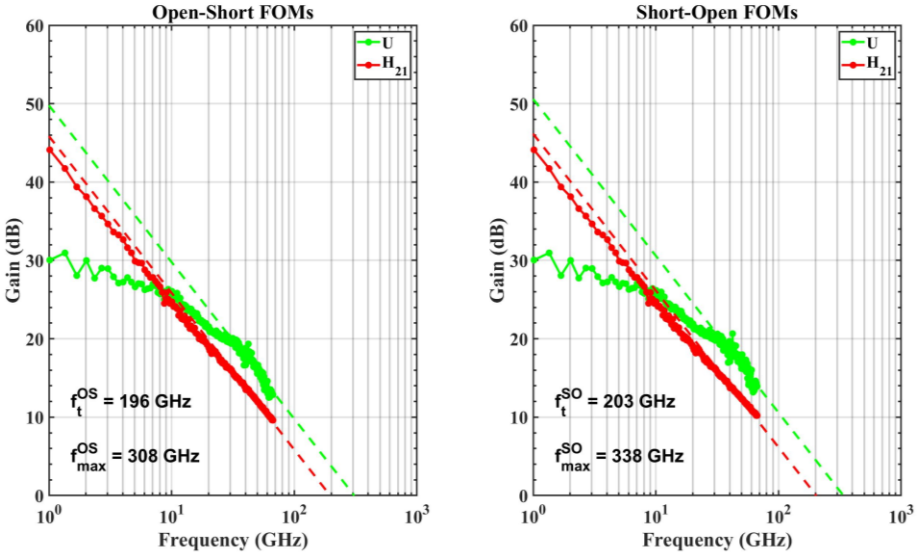


Figure 6.8: RF FOM extraction for RRMH-24-Die-2, W_g=2x10um, Lg = 26 nm, V_{GS} = 0.3 V, V_{DS} = 0.8 V

Initial de-embedding and small signal circuit extraction is performed via automation as outline in the Model Extraction section. Plotting these results vs gate length in Figure 6.9 below show high $C_{GS,e}$ and $C_{GD,e}$ greater than 1.0 and 0.5 fF/μm respectively due to incomplete removal of the sacrificial layer. Both transconductance and output conductance show great improvement from generation 1 with $g_{m,e}$ > 1.5 mS/um and $g_{ds,e}$ < 0.15 mS/um. High frequency figures of merit are increased by the improvement in transconductance and output conductance but are still severely limited by high capacitance. f_τ tops out around 200 GHz and f_{max} 300 GHz.

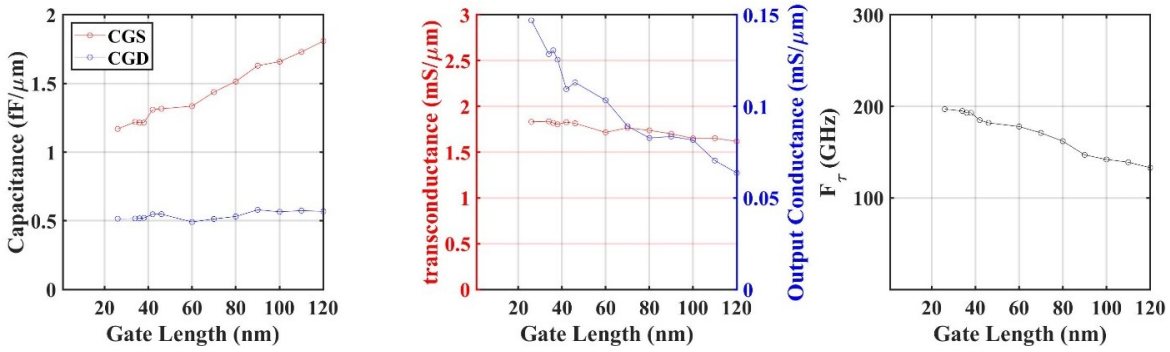


Figure 6.9: Gate length series of extracted common-source SSEC elements for RRMH-24-Die-2, W_g = 2x10 um

D. RF Results, Off Wafer Calibration, DC to 67 GHz, Lg = 26 nm

Y parameters for a 26 nm device biased at V_{GS} = 0.3 Volts and V_{DS} = 0.8 Volts, DC to 67 GHz can be seen in Figure 6.10 and Figure 6.11 below.

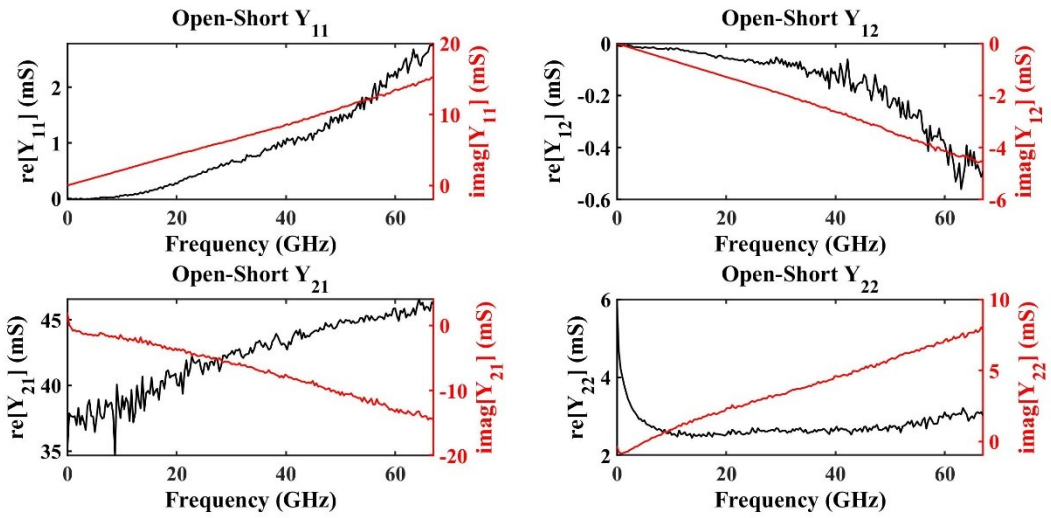


Figure 6.10: DC to 67 GHz Y-parameters with open-short de-embedding for RRMH-24-Die-2, W_g=2x10um, Lg = 26 nm, V_{GS} = 0.3 V, V_{DS} = 0.8 V

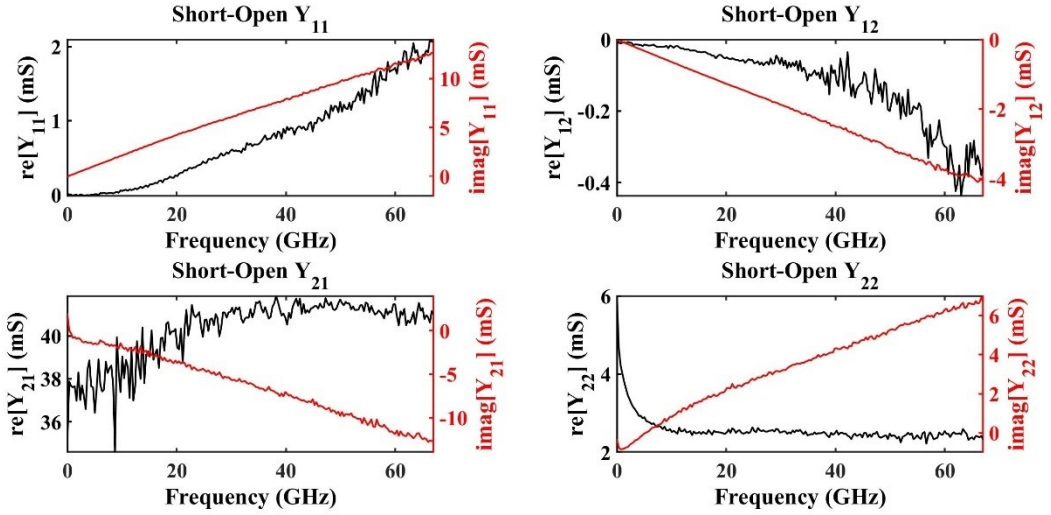


Figure 6.11: DC to 67 GHz Y-parameters with open-short de-embedding for RRMH-24-Die-2, W_g=2x10um, Lg = 26 nm, V_{GS} = 0.3 V, V_{DS} = 0.8 V

In Figure 6.12 below, the final equivalent circuit model and S parameters for the 26 nm gate length device are seen. Extraction utilizes the initial simplified circuit model followed by fine tuning the more extensive circuit model in ADS.

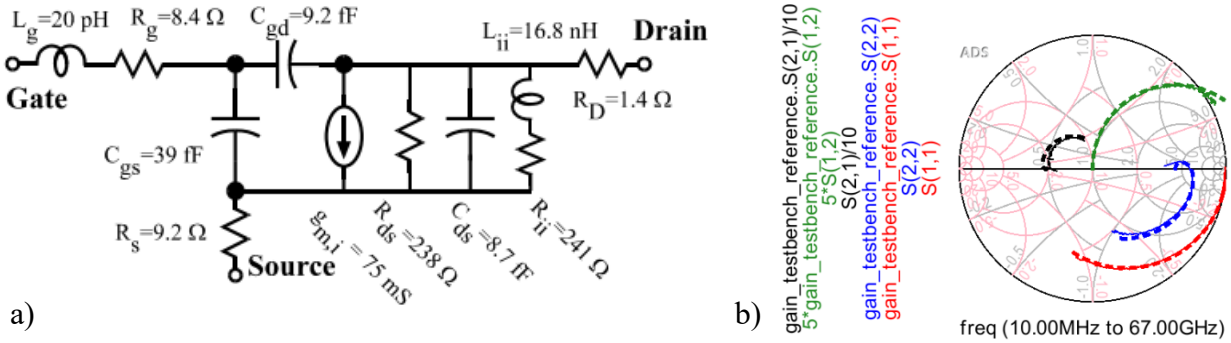


Figure 6.12: RRMH-24-Die-2, W_g=2x10um, Lg = 26 nm, V_{GS} = 0.3 V, V_{DS} = 0.8 V (a) equivalent circuit model (b) S-parameter DC to 67 GHz

E. Conclusions

Improvements in Generation 2's performance were mostly due to the vast improvements in source resistance. The N+ sheet resistance was cut in half by increasing the N+ InGaAs regrowth from 25 to 50 nm. The contact resistance was reduced by changing the methodology of ohmic contacts described in the Source Drain Ohmics section. The link sheet resistance was improved by switching the topside barrier to InAlAs to increase confinement, therefore decreasing scattering while simultaneously improving charge. The link end resistance was improved by growing the topside link doping as part of the initial epi instead of regrowing it. This avoided the issue of voids in the regrowth while also improving mobility by reducing surface roughness.

Further improvements on Generation 2 devices proved to be difficult. Further increases in the sacrificial etch time did little to remove the sacrificial layer until reaching etch times on the order of 10 minutes. In addition, the InAlAs link proved to be an ineffective barrier for the HCl based chemistry for the longer etch times that proved to be necessary. Unfortunately, to make a structure more resilient to the long etch times, the InAlAs topside link doping was replaced by a lattice matched InGaAs layer in proposed Generation 2.3 designs.

7. Generation 2.3

This chapter will outline fabrication, design, results, and conclusions for the self-aligned regrowth reversal MOS-HEMT exhibiting $f_\tau > 500$ GHz and $f_{max} > 1$ THz.

A. Fabrication

3 nm cap	UID	$In_{0.53}Ga_{0.47}As$
3 nm link	N+ (4e19)	$In_{0.53}Ga_{0.47}As$
7 nm channel	UID	$In_{0.80}Ga_{0.20}As$
3 nm spacer	UID	$In_{0.52}Al_{0.48}As$
3 nm δ-doping	N+ (1e19)	$In_{0.52}Al_{0.48}As$
100 nm back barier	UID	$In_{0.52}Al_{0.48}As$
500 um substrate	semi-insulating	Fe:InP

Figure 7.1: Illustration of Generation 2.3 MBE epitaxy

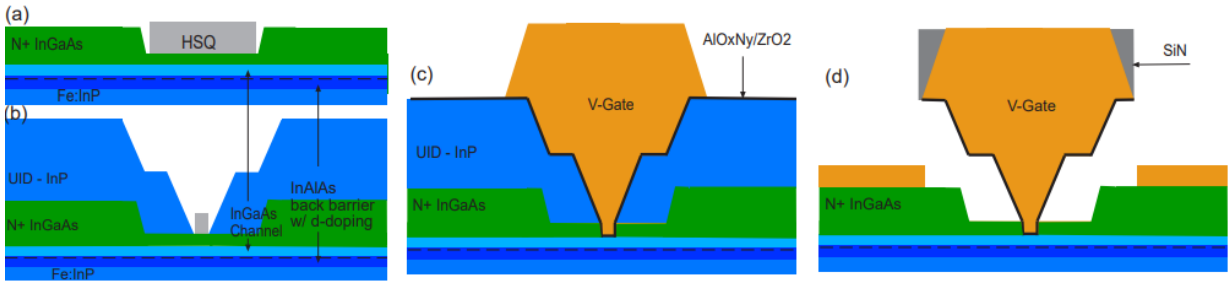


Figure 7.2: process flow (a) Epi, dummy link, contact regrowth (b) dummy gate, sacrificial regrowth (c) etch N+ link, high-k deposition, gate metal deposition (d) high-k etch, SiN sidewall, InP removal, ohmic contact deposition

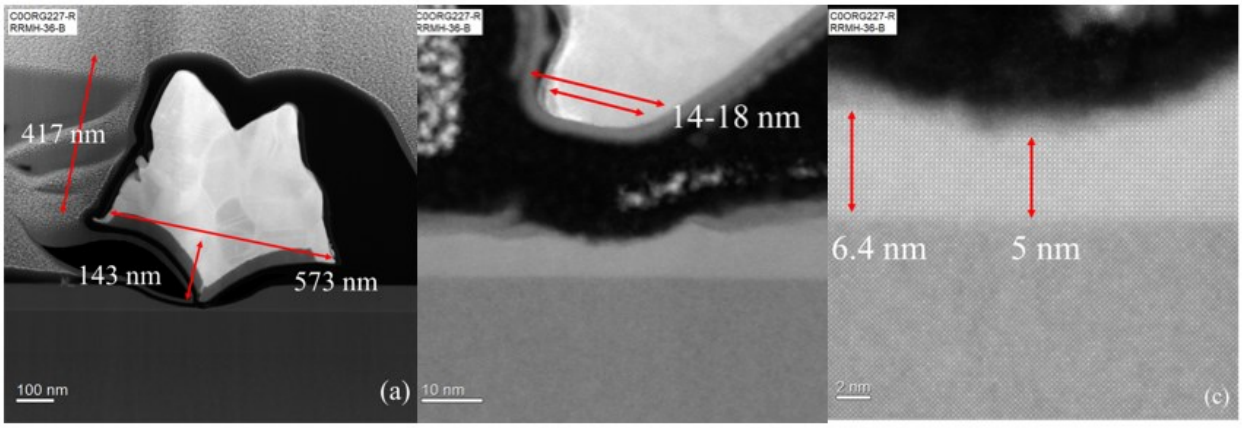


Figure 7.3: 18 nm Lg TEM cross section. Note: the gate was dislodged from channel during FIB. (a) full device (b) gate length (c) channel thickness

The fabrication process started with Epi purchased from Intelligent Epitaxy. The layers were grown by MBE on a (100) Iron doped semi-insulating substrate. Alignment marks were defined using the MLA150 and wet etched as described in the Appendices. Dummy links were defined by EBL in the 010 direction. 50 nm thick N+ InGaAs Source/Drain contacts were regrown in the MOCVD with 100 nm source to gate and gate to drain spacing. After dummy gate definition, 5 nm of UID InGaAs and 80 nm of UID InP were regrown. Regrowths resulted in good sheet and contact resistance as seen in Figure 7.4 and Table 7.1 below.

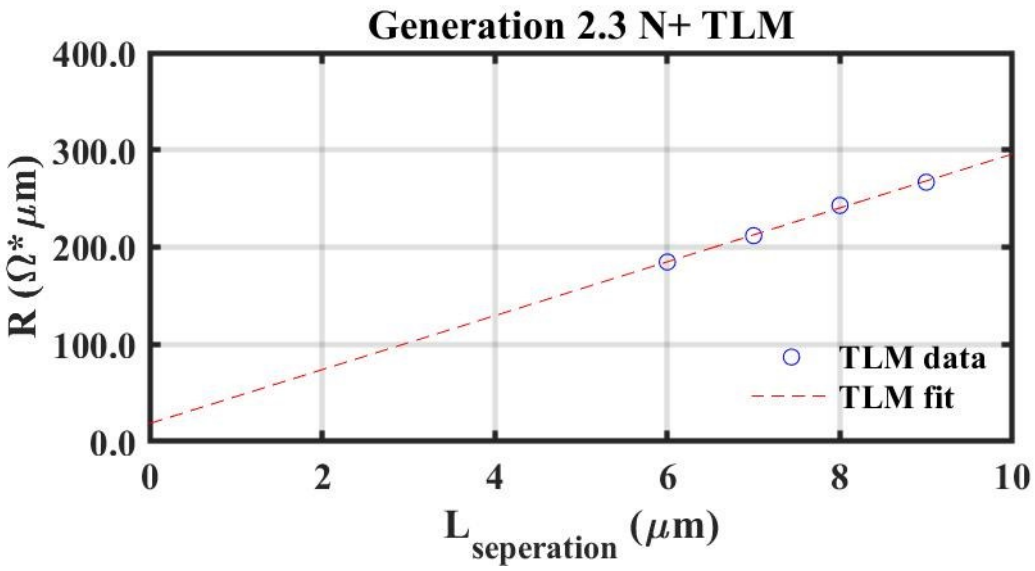


Figure 7.4: RRMH-36 TLMs for 50 nm thick N+ InGaAs

Table 7.1: RRMH-36 TLM results for 50 nm thick N+ InGaAs

RRMH-36 N+ TLM								
R_N	27.73	Ω/□	R_N	8.32	Ω•μm	L_T	0.317	μm
R_C	0.46	Ω	R_C	9.27	Ω•μm	ρ_C	2.79	$\Omega \cdot \mu m^2$

The HSQ dummy gate was removed, and the channel was digital etched 8 times to reduce the channel thickness to about 6 nm. Next, high-k and gate deposition was performed as described in sections “High-k Deposition” and “V-Gate Deposition”. Following the 30 nm SiN deposition by PECVD, the InP protection lithography was exposed. The vertical dry etch was then performed to simultaneously sidewall the gates and create a hard mask at the gate finger ends. Combining these two steps minimized the gate undercut seen at the ends of the fingers and gave smoother pad metal connections. To remove the resulting cross-linked resist, the samples were then placed in a DUV flood exposure for 5 minutes and soaked in NMP for 2 hours.

The devices were then etched in HCL:H2O 1:1 for 2 minutes to remove the sacrificial layer. The devices were then isolated using optical lithography and wet chemistry. Ohmics were defined optically then E-beam evaporated using Pd/Ti/Pt/Au 9/15/15/100 nm. Next, devices were passivated using 30 cycles of ZrO_2 (CH3-TEMAZ+H2O-300C) followed by a 30-minute Hydrogen anneal in the ALD system at 350 degrees Celsius. Vias were defined optically and etched in BHF for 80 seconds to account for the ZrO_2 passivation and the SiN hard mask. Lastly, pad metal was defined optically and E-beam evaporated using 20 nm of Titanium and 500 nm of Gold.

B. DC Results

Figure 7.5 below shows the lot DC characteristics for Generation 3 devices for 20 µm gate width devices on Die 5.

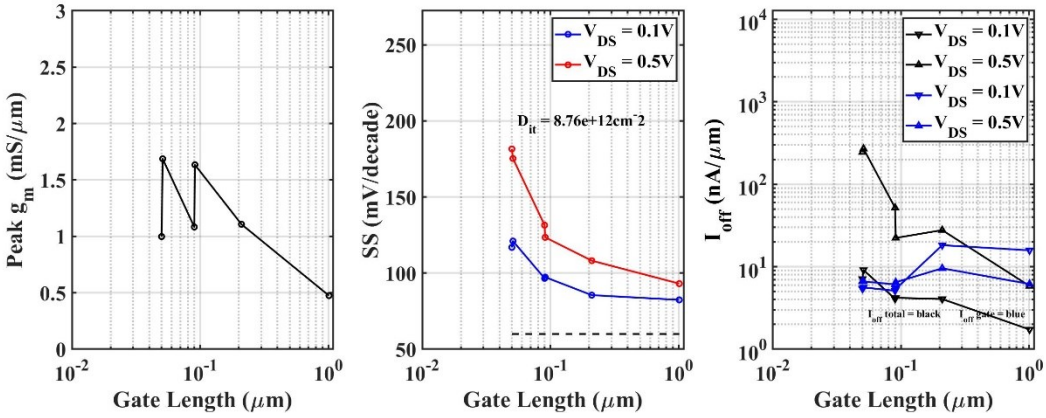


Figure 7.5: Lot DC results for RRMH-36-Die-5-Wg-20um

Peak DC transconductance above 1.5 mS/um is observed with subthreshold slope at 83 mV/decade at 1000 nm gate lengths and V_{DS} = 0.1 Volts. I_{off} < 300 nA is observed at gate lengths measured down to 50 nm at V_{DS} = 0.5 Volts, and gate leakage < 20 nA at all gate lengths at all gate biases.

High variation between the left and right gate fingers for one device is visually seen as vertical lines on the transconductance graph. In Figure 7.6 and Figure 7.7 the left and right gate fingers for a 30 nm device show the differences in more detail. The left gate shows a DC transconductance of about 1 mS/um at about 0.4 Volts V_{GS} while the right gate shows a DC transconductance just over 1.5 mS/um at around 0.2 Volts V_{GS}.

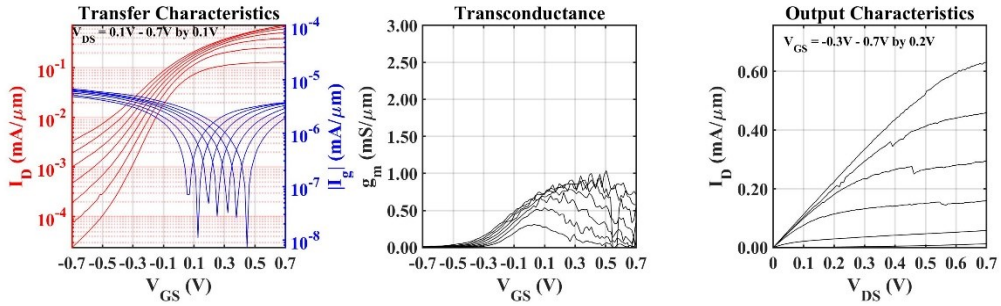


Figure 7.6: DC results for RRMH-36-Die-5, W_g=20um, L_g = 30 nm (left)

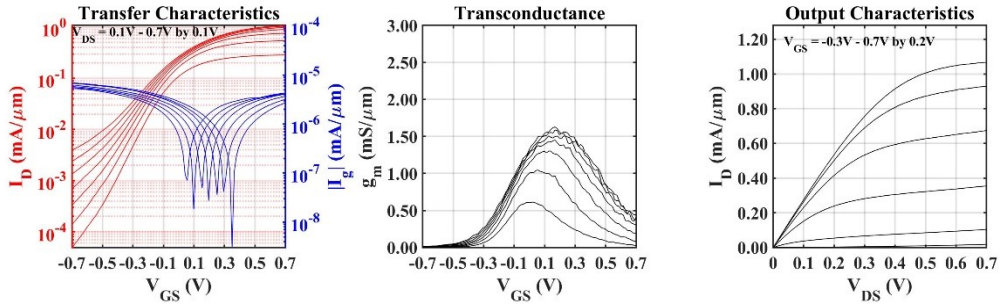


Figure 7.7: DC results for RRMH-36-Die-5, W_g=20um, Lg = 30 nm (right)

This variation is observed across multiple devices on multiple dies, but its exact source is still unknown. Consistent variation in extrinsic transconductance of >30% is not easily explained by source to gate spacing variation because the change in source resistance would have to be on the order of 200-300 Ω*μm. With expected link sheet resistance on the order of 1000 Ω/□ misalignment as high as 50 nm would only result in source resistance variation on the order of 50 Ω*μm. Source to drain spacing variation also is a poor explanation for the drastic threshold shift.

C. RF Results (Lot)

Initial testing is performed from DC to 67 GHz using off wafer probe tip calibration followed by on wafer open-short and short open de-embedding. As seen in Figure 7.8, short-open de-embedding gives better results, but the data is significantly noisier. For clarity, data de-embedded using open-short will be presented in this section.

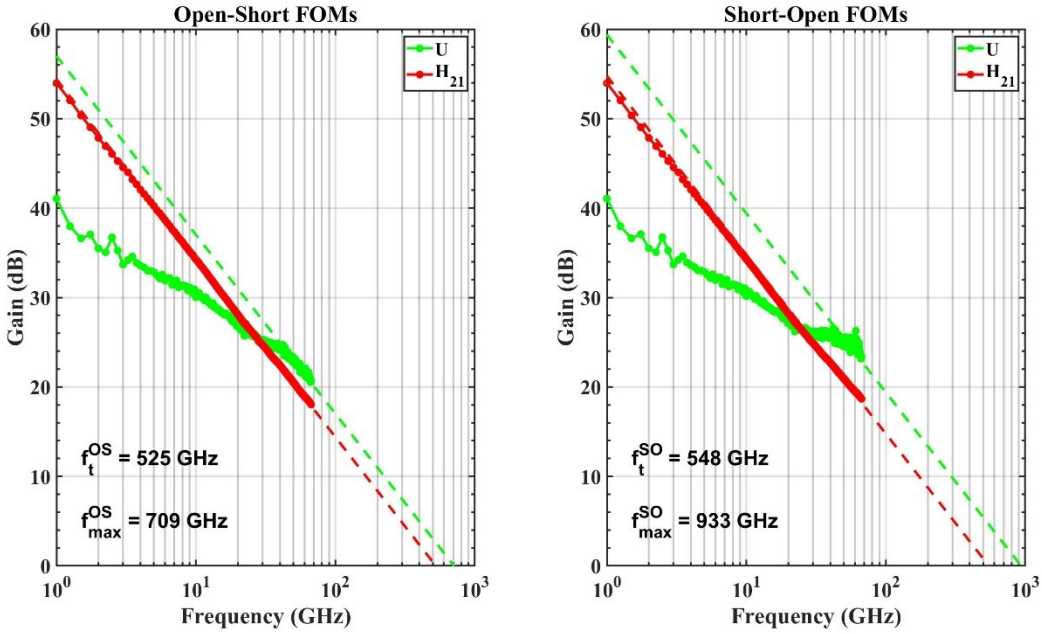


Figure 7.8: RF FOM extraction for RRMH-36-Die-5, W_g=2x20um, Lg = 20 nm, V_{GS} = 0.2 V, V_{DS} = 1.0 V

Initial de-embedding and small signal circuit extraction is performed via automation as outlined in the Model Extraction section. Plotting these results vs gate length in Figure 7.9 below show vast improvements on all previous work on MOS-HEMTs. $C_{GS,e}$ and $C_{GD,e}$ are lowered to below 0.5 fF/μm and 0.1 fF/μm respectively for gate lengths less than 30 nm. Extrinsic RF transconductance peaks around 2 mS/um and extrinsic RF output conductance is below 0.15 mS/um down to minimum achieved gate lengths of 16 nm. F_τ above 500 GHz is achieved for gate lengths less than or equal to 26 nm.

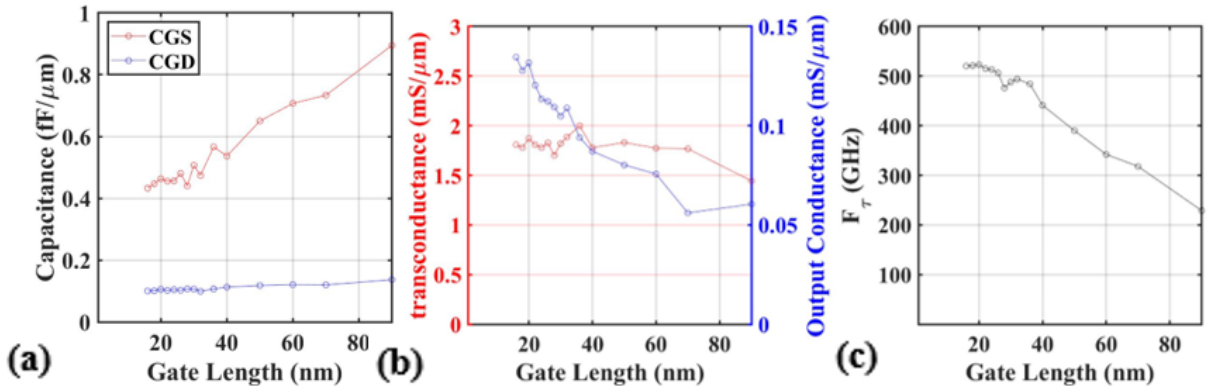


Figure 7.9: Gate length series of extracted common-source SSEC elements for RRMH-36-Die-5, W_g=2x20um

D. RF Results, Off Wafer Calibration, DC to 67 GHz, Lg = 20 nm

Output characteristics for a 20 nm device can be seen in Figure 7.10 below.

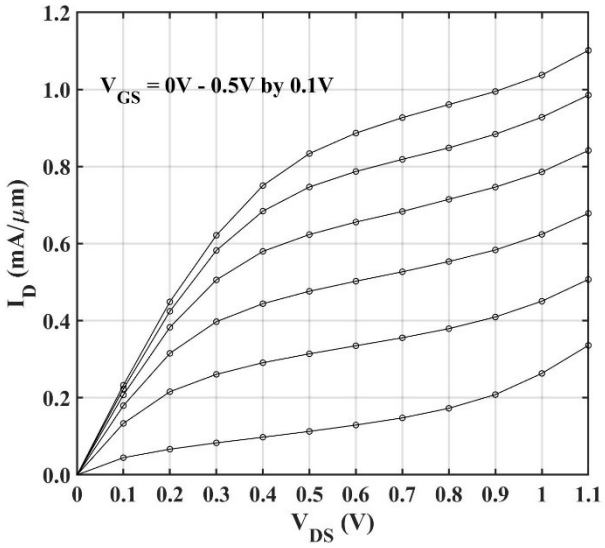


Figure 7.10: Output characteristics for RRMH-36-Die-5, W_g=2x20um, Lg = 20 nm

Y-parameters for a 20 nm device biased at V_{GS} = 0.2 Volts and V_{DS} = 1.0 DC Volts, DC to 67 GHz can be seen in Figure 7.11 and Figure 7.12 below.

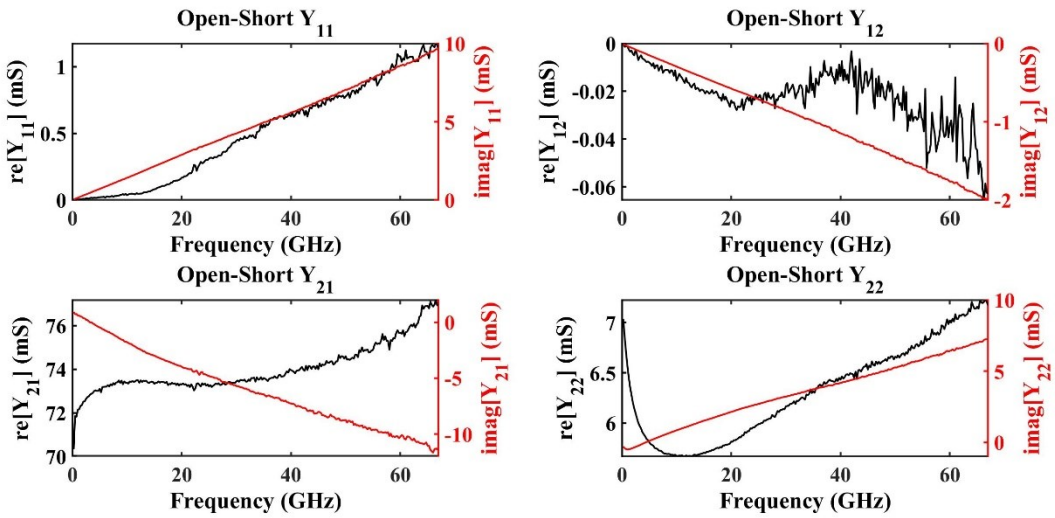


Figure 7.11: DC to 67 GHz Y-parameters with open-short de-embedding for RRMH-36-Die-5, W_g=2x20um, Lg = 20 nm, V_{GS} = 0.2 V, V_{DS} = 1.0 V

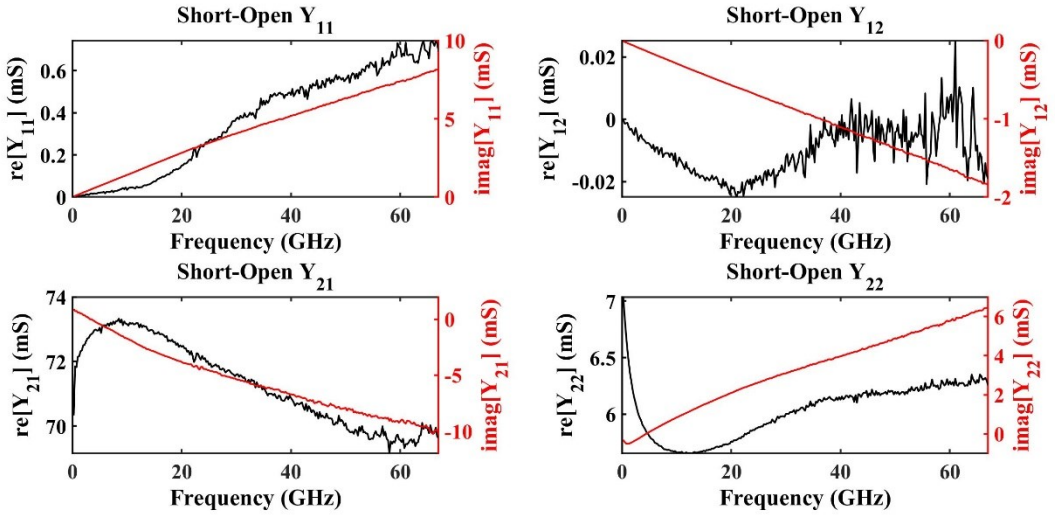


Figure 7.12: DC to 67 GHz Y-parameters with short-open de-embedding for RRMH-36-Die-5, W_g=2x20um, Lg = 20 nm, V_{GS} = 0.2 V, V_{DS} = 1.0 V

U, H_{21}, and MSG are seen plotted in Figure 7.13 below at DC to 67 GHz resulting in an f_τ of 525 GHz and fmax of 708 GHz.

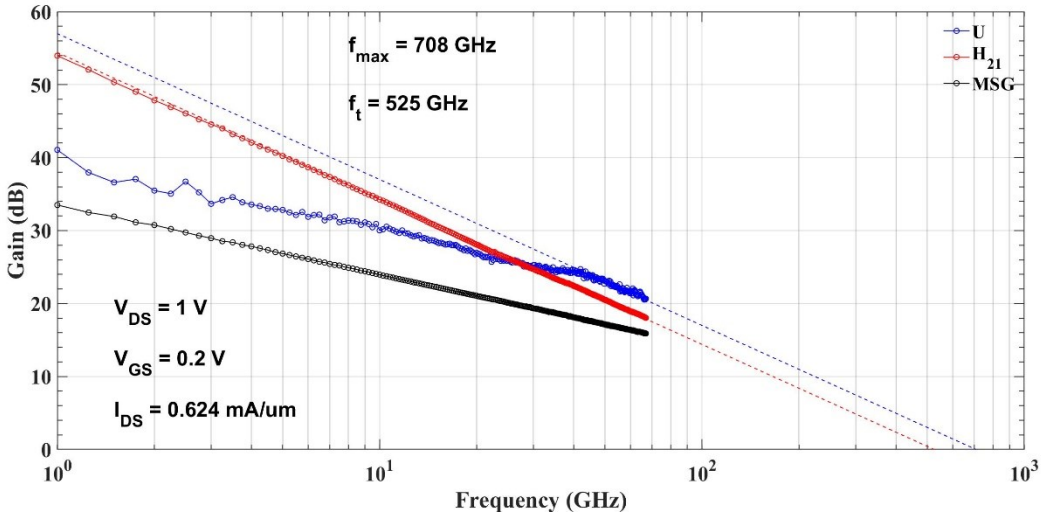


Figure 7.13: U, H_{21}, and MSG at DC to 67 GHz for RRMH-36-Die-5, W_g=20um, Lg = 20 nm, V_{GS} = 0.2 V, V_{DS} = 1.0 V

In Figure 7.14 below, the final equivalent circuit model and S-parameters for the 20 nm gate length device are seen. Extraction utilizes the initial simplified circuit model followed by fine tuning the more extensive circuit model in ADS.

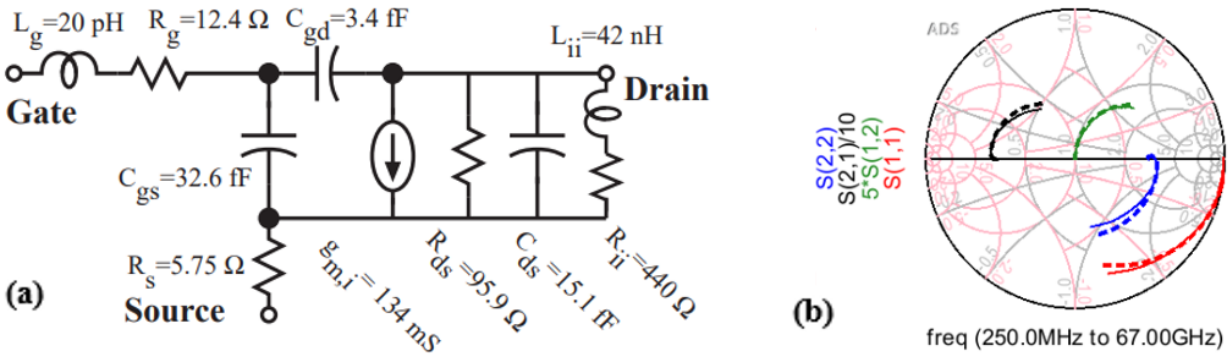


Figure 7.14: RRMH-36-Die-5, W_g=2x20um, Lg = 20 nm, V_{GS} = 0.2 V, V_{DS} = 1.0 V (a) equivalent circuit model (b) S-parameter DC to 67 GHz

E. RF Results, Off Wafer Calibration, DC to 67 GHz, Lg = 36 nm

Output characteristics for a 20 nm device can be seen in Figure 7.15 below.

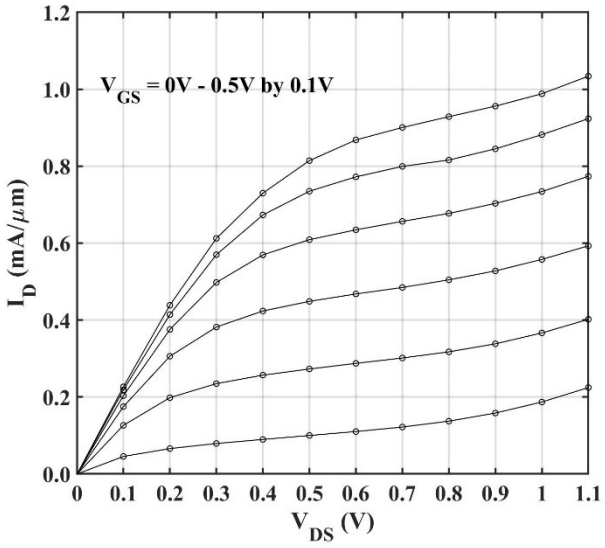


Figure 7.15: Output characteristics for RRMH-36-Die-5, W_g=2x20um, Lg = 36 nm

Y-parameters for a 36 nm device biased at V_{GS} = 0.2 Volts and V_{DS} = 0.9 Volts, DC to 67 GHz can be seen in Figure 7.16 and Figure 7.17 below.

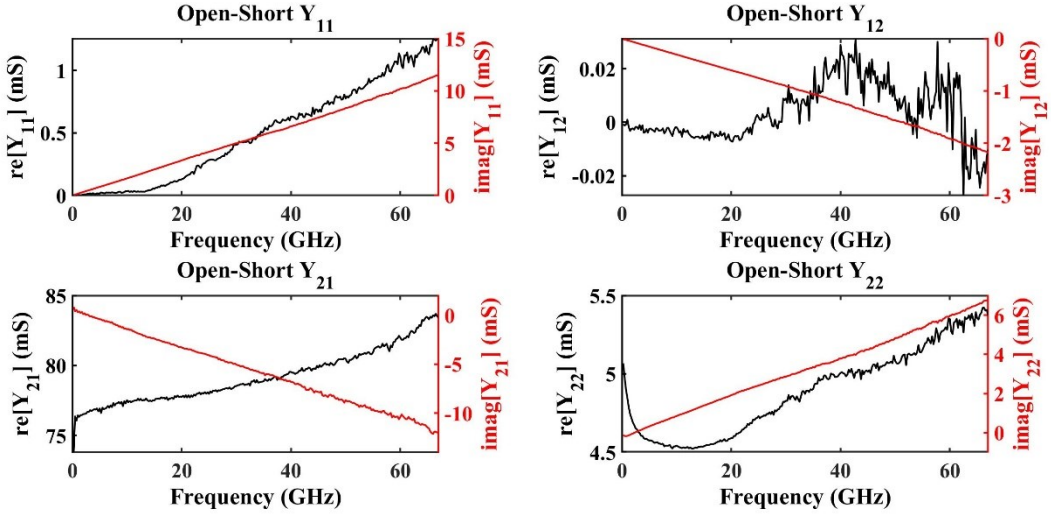


Figure 7.16: DC to 67 GHz Y-parameters with open-short de-embedding for RRMH-36-Die-5, W_g=2x20um, Lg = 36 nm, V_{GS} = 0.2 V, V_{DS} = 0.9 V

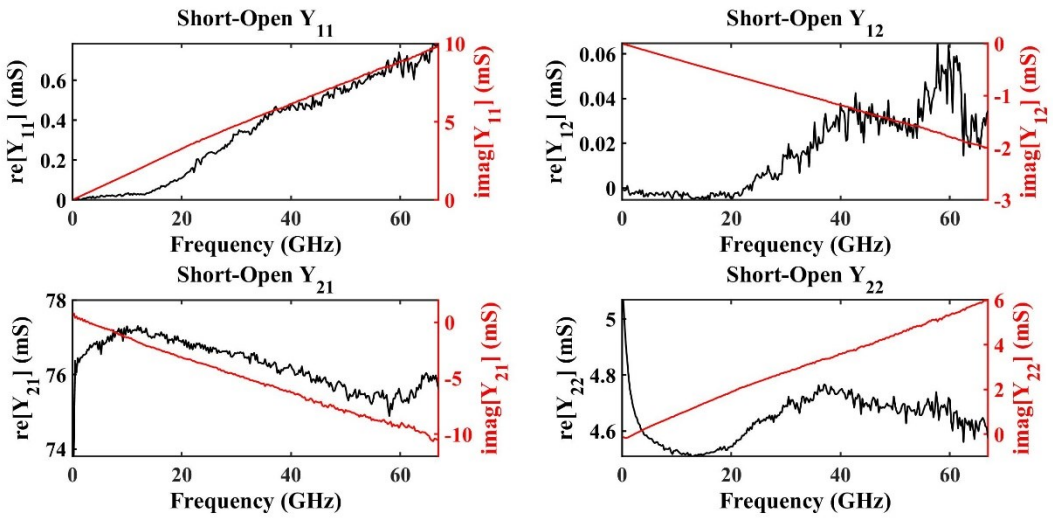


Figure 7.17: DC to 67 GHz Y-parameters with short-open de-embedding for RRMH-36-Die-5, W_g=2x20um, Lg = 36 nm, V_{GS} = 0.2 V, V_{DS} = 0.9 V

U, H_{21}, and MSG are seen plotted in Figure 7.18 below at DC to 67 GHz resulting in an f_τ of 479 GHz and fmax of 1.15 THz.

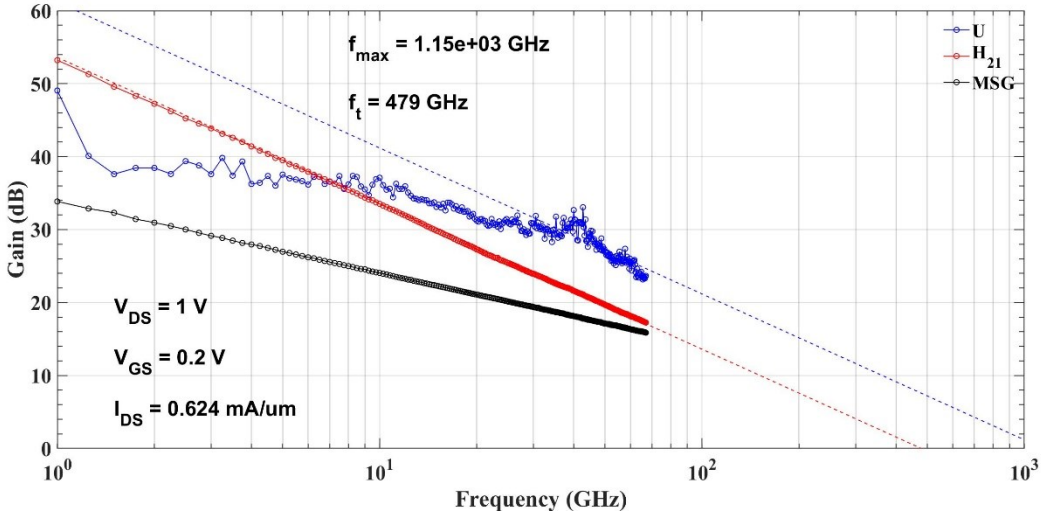


Figure 7.18: U, H_{21}, and MSG at DC to 67 GHz for RRMH-36-Die-5, W_g=2x20um, Lg = 36 nm, V_{GS} = 0.2 V, V_{DS} = 0.9 V

In Figure 7.19 below, the final equivalent circuit model and S-parameters for the 36 nm gate length device are seen. Extraction utilizes the initial simplified circuit model followed by fine tuning the more extensive circuit model in ADS.

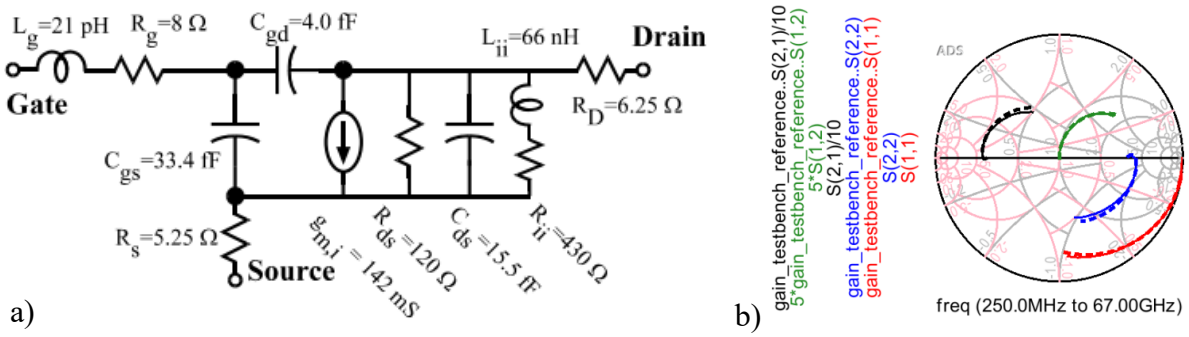


Figure 7.19: RRMH-36-Die-5, W_g=40um, Lg = 36 nm, V_{GS} = 0.2 V, V_{DS} = 0.9 V (a) equivalent circuit model (b) S-parameter DC to 67 GHz

F. RF Results, On Wafer TRL Calibration 15 to 110 GHz

Data up to this point has been collected using off-wafer OSLT (Open, Short, Load, Thru) calibrations and testing up to 67 GHz followed by on wafer open-short de-embedding. While researchers still utilize OSLT for accurate low frequency extractions, on wafer TRL (Thru, Reflect, Line) and LRM (Line, Reflect, Match) are now the preferred industry standard for high frequency calibration.

TRL standards utilize several line lengths to determine the velocity and characteristic impedance of the line to extract pad parasitics. Increasingly long lines can also be utilized to fine tune the velocity further. Unfortunately, longer lines can take significant die area that can be prohibitively expensive for academic researchers. Additionally, reliable processing is necessary for consistent pad shape and thickness.

OSLT standards are purchased from vendors and their characteristics are precisely known. This allows for good measurements at low frequencies. Circuit parameters are generally extracted from lower frequencies, so OSLT is preferred for SSEC. As frequencies increase, higher order modes are excited on the device substrate. OSLT is poor at removing these effects, and TRL is therefore preferred.

To validate the THz results presented in the previous section, these devices were taken to Northrup Grumman for on wafer TRL testing at 15 to 110 GHz. Line lengths of 0, 300 μm, 425 μm, and 650 μm were used. Unfortunately, poor RF results were extracted from these results. Upon further inspection, DC results had also significantly degraded since the OSLT DC-67 GHz testing. Because the TRL testing took place 6 weeks later and after the wafer was broken during TEMs, the devices were said to have degraded. RF and DC results can be seen in Figure 7.20 and Figure 7.21.

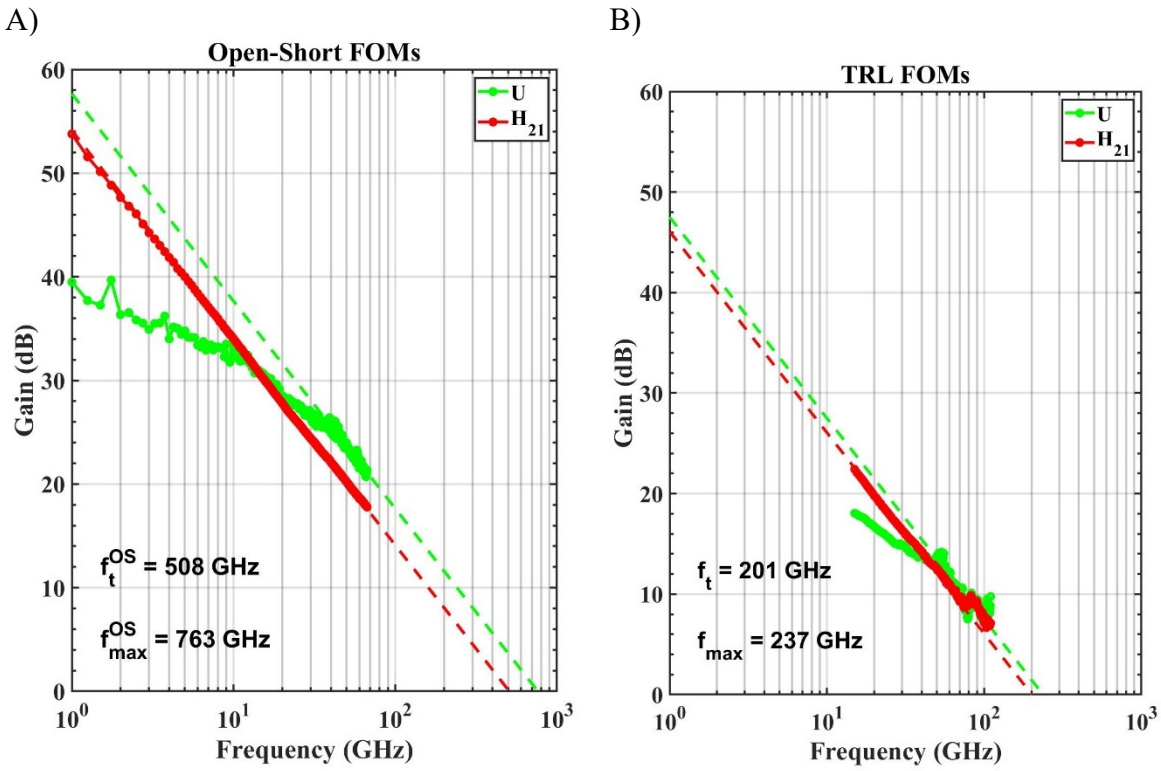


Figure 7.20: High Frequency FOM extractions for a 16 nm device
A) OSLT calibration and open-short de-embedding DC – 67 GHz
B) TRL calibration 15-110 GHz

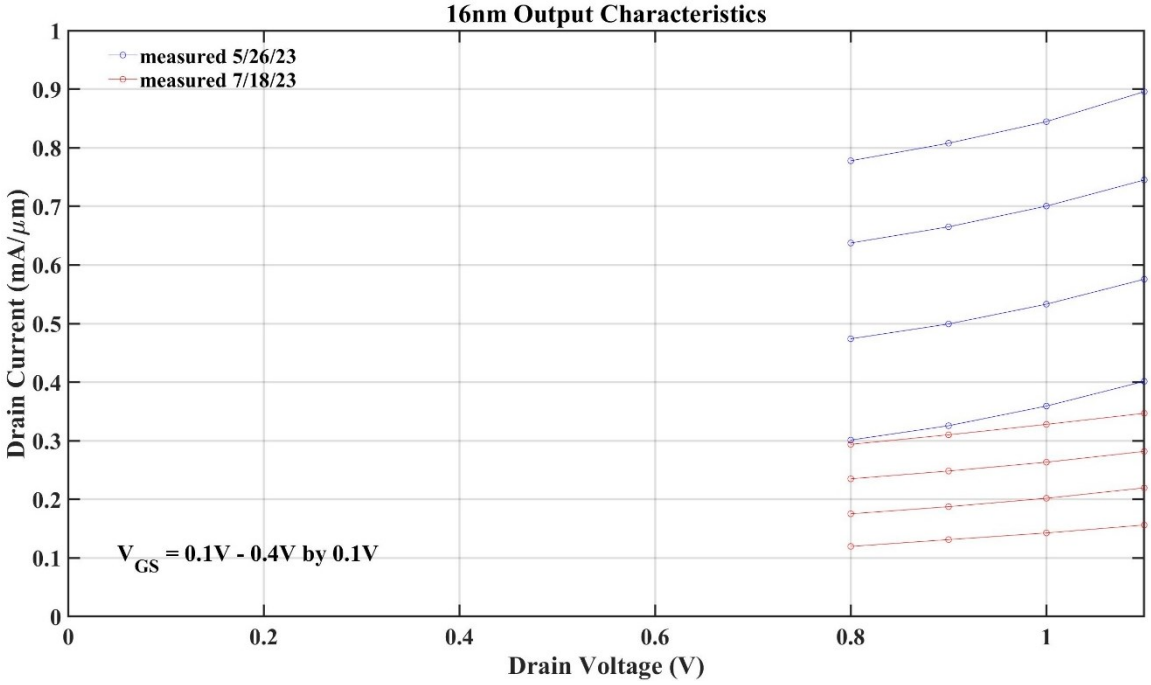


Figure 7.21: DC current for a 16 nm device during initial OSLT and later TRL testing

G. Conclusions

The philosophy for Generation 3 was to remove the sacrificial layer at any cost. First, the process was switched to a gate first process from a mesa first process. This allowed for longer sacrificial etch times without etching into the substrate and making pad connections impossible. This was a change from Generation 2.2 which focused on mesa first processes because side by side experiments repeatedly showed better transconductance for mesa first processes. The exact cause was never confirmed, but possible avenues for transconductance reduction in the gate first process were increased channel undercut or additional high-k damage from processing.

The second conservative choice was in the topside link. To avoid concerns about etching, the topside link doping was changed to 3 nm 4e19 InGaAs capped with 3 nm UID-InGaAs. Predicting the amount of charge for a quantum well with such a small conduction band offset is mathematically ill defined. Predicting the charge using a self-consistent 2D Schrödinger-Poisson solver is difficult for an immature material system such as InP already. The prediction becomes even more volatile in this scenario because the charge is largely dependent on the surface pinning of the InGaAs that is difficult to predict. To account for this and avoid source starvation, the doping levels used in this design were quite high.

High doping levels and low band gap at the drain edge increases DC output conductance for highly scaled devices as detailed by Chen-Ying Huang and Sanghoon Lee of the Rodwell group [37, 10]. The suspected culprit was band to band tunneling (BTBT) because of low band gap and high electric fields. Fields in devices detailed by Huang and Lee were for VLSI applications and therefore had no source to drain spacing. This resulted in higher fields at the gate-drain edge than in the RF devices detailed in this thesis.

Nevertheless, the high output conductance can be seen as a breakdown effect in DC output characteristics in Figure 7.10 and Figure 7.15 or in the DC lot characteristics in Figure 7.5. This high output conductance is noticeably lower in the RF lot characteristics in Figure 7.9 or by looking at the slope of Re[Y22] at frequencies above ~20 GHz in Figure 7.11, Figure 7.12, Figure 7.16, and Figure 7.17. This means that the breakdown phenomenon does not react at high frequencies and is due to impact ionization of trap assisted tunneling.

The third conservative design choice was the inclusion of an additional UID-InGaAs cap layer regrowth right before the InP sacrificial layer regrowth. This was to further protect the topside link doping and the channel. During Generation 2.2 experiments, it was discovered that the strained channel would etch very quickly if exposed to the HCl used during the sacrificial etch. The inclusion of the cap effectively results in a thicker link layer. From simulations and hand calculations details in the Link Design section, this will result in worse end capacitance.

Despite the conservative decisions made in this process, the benefits from complete sacrificial layer removal far outweighed any negatives. Extrinsic gate to source capacitance was reduced by almost half and extrinsic gate to drain capacitance was reduced 5x. This results in a total $C_{GS,e}$ + $C_{GD,e}$ reduction of about 60% for short gate length devices compared to generation 2.2.

8. Conclusion

A. Summary

A self-aligned MOS-HEMT process is demonstrated resulting in world record f_τ = 525 GHz and f_{max} > 1 THz for MOS-HEMT technology. The resulting MOS-HEMTs are rapidly approaching world record HEMT results for f_τ (Park and Jo *et al*, f_τ = 750 GHz, f_{max} = 1.1 THz) and for f_{max} (Deal *et al*, f_τ = 610 GHz, f_{max} = 1.5 THz) [3, 2]. Integrating a sacrificial InP support structure with a double regrowth process flow allowed for self-alignment for MOS-HEMTs. Additionally, the InP regrowth facets resulted in a new V-gate structure for improved gate filling and gate footprint scaling.

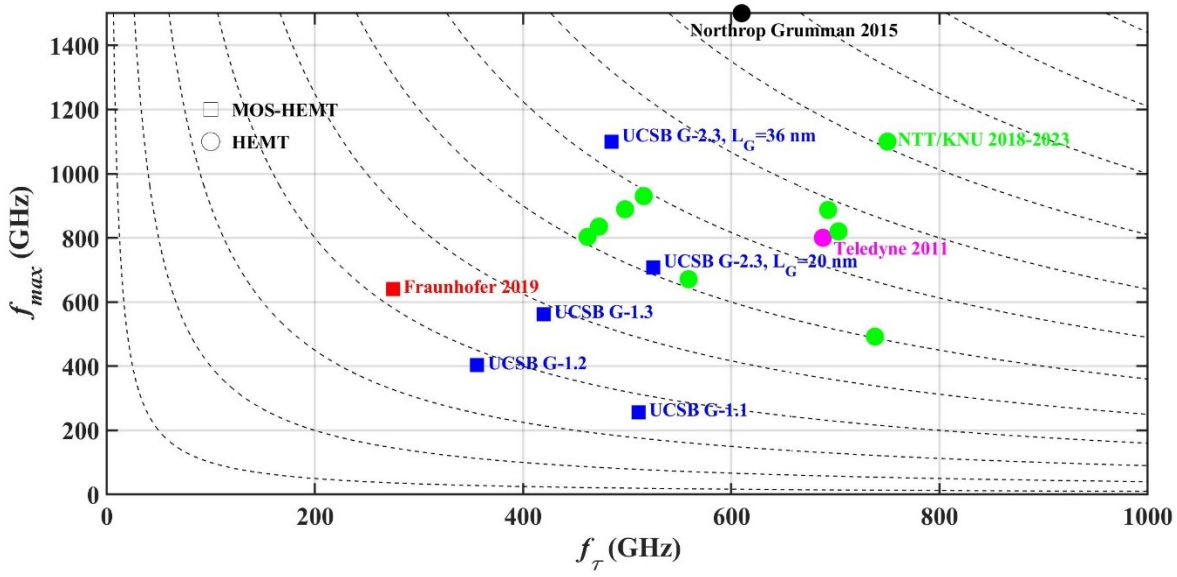


Figure 8.1: High Frequency Figures of Merit for state of the art MOS-HEMTs and HEMTs

Gate resistance theory presented in the Gate Design section indicates that V-gates beat T-gates on vertical resistance. Unfortunately, devices presented in this work do not have scaled gate widths. This results in high lateral resistance that dominates any benefit in vertical resistance.

Link design theory was developed for the new MOS-HEMT structure in the Link Design section. Optimal link design must not only consider the sheet resistance of the link, but it must also consider its effect on fringe capacitance. MOS-HEMTs have increased fringe capacitance due to the high-k dielectric between the gate and the link. Self-alignment helps reduce this capacitance, but thinning the link reduces the gate-link overlap to minimize C_{GS}+C_{GD} further. While thinning the link requires putting topside donor ions closer to the mobile charge in the channel and results in worse mobility, this work shows the benefit in C_{GS}+C_{GD} far outweighs the harm in source resistance. Additionally, the harm to link resistance can be mitigated by aggressive scaling of source to gate spacing. The link design theory allowed for C_{GS}+C_{GD} reduction of roughly 40% compared to generation 1 devices.

B. Future Work

While MOS-HEMT performance still lags behind state-of-the-art HEMTs, moving to a new self-aligned V-gate was just a major step backwards to facilitate even larger steps forward. This work potentially represents the first of those steps. To improve high frequency performance, these devices must be optimized for larger intrinsic transconductance, lower gate resistance, lower source resistance, and lower $C_{GS,fringe}$.

As studied extensively by Markman, intrinsic transconductance is heavily dependent on channel design [11]. A wide and deep quantum well minimizes the first eigen state energy and maximizes E_F-E_1 at peak bias conditions. To accomplish this, one must grow a thick InGaAs channel, to maximize well width, with a large indium content, to maximize well height. Growing thick, high indium content channels requires large amounts of strain. Epitaxy vendors no longer are able to provide such complex epi at low volumes. Access to state-of-

the-art epi should increase intrinsic transconductance from its current level of ~3.35 mS/um to its previous levels of 4.2 mS/um. This roughly 25% increase would increase the ideal f_τ by approximately 25%.

Gate resistance in these devices was limited by large gate widths. Theoretical work presented in this thesis predicts that when gate lengths and widths are scaled, V-gates should win in gate resistance. This would improve f_{max}.

Source resistance in these devices was limited by the link resistance. Link resistance increased in these devices by more than expected for two reasons. First, the original channel design was more strained. This allowed for better confinement in the link region and therefore higher charge and mobility. Second, the source to gate spacing was doubled from the original design. This was to improve the yield of the devices, but the source to gate spacing should be minimized for a future high-performance device.

Fringe capacitance in these devices was limited by the high-k. In these devices, maximizing the insulator capacitance to manage short channel effects was the top priority. This results in a highly scaled oxide in the middle of the gate-link overlap region. Using a thicker high-k would result in lower fringe capacitance but higher output conductance. This would be advantageous for a design more focused on f_τ than f_{max}. Additionally, these devices are passivated in the high-k. This puts additional high dielectric constant material between the corner of the gate and the link, further driving up the fringe capacitance. Replacing this with a SiN passivation layer would decrease fringe capacitance.

References

[1] M. Rodwell, B. Markman, Y. Fang, L. Whitaker, H.-Y. Tseng and A. S. H. Ahmed, "Transistors for 100-300GHz Wireless," *DRC,* 2021.

[2] W. Deal, K. Leong, W. Yoshida, A. Zamora and X. Mei, "InP HEMT Integrated Circuits operating above 1,000 GHz," *IEDM,* 2016.

[3] W.-S. Park, H.-B. Ji, H.-J. Kim, S.-M. Choi, J.-H. Yoo, J.-H. Kim, H.-S. Jeon, S. George, I.-G. L. Ji-Min Beak, T.-W. Kim, S.-k. Kim, J. Yun, T. Kim, T. Tsutsumi, H. Sugiyama, H. Matzuzaki, J. K. Lee and D.-H. Kim, "Terahertz In0.8Ga0.2As quantum-well HEMTs toward 6G applications," *IEDM,* 2022.

[4] T.-W. Kim and J. A. d. Alamo, "Injection Velocity in Thin-Channel InAs HEMTs," *IEEE,* 2011.

[5] M. Rodwell, W. Frensley, S. Steiger, E. Chagarov, S. Lee, H. Ryu, Y. Tan, G. Hegde, L. Wang, J. Law, T. Boykin, G. Klimek, P. Asbeck, A. Kummel and J. N. Schulman, "III-V FET Channel Designs for High Current Densities and Thin Inversion Layers," *DRC,* 2010.

[6] K. Shinohara, Y. Yamashita, A. Endoh, I. Watanabe, T. M. K. Hikosaka, T. Mimura and S. Hiyamizu, "547-GHz ft In0:7Ga0:3As–In0:52Al0:48As HEMTs With Reduced Source and Drain Resistance," *IEEE Electron Device Letters,* vol. 25, no. 5, pp. 241-243, 2004.

[7] A. D. Carter, "Gate Last Indium-Gallium-Arsenide MOSFETs with Regrown Source-Drain Regions and ALD Dielectrics," *University of California, Santa Barbara,* 2013.

[8] U. Singisetti, "In0.53Ga0.47As MOSFETs with 5 nm channel and self-aligned source/drain by MBE regrowth," *University of California, Santa Barbara,* 2009.

[9] S. Lee, "Design, Fabrication, and Characterization of High Performance III-V nMOSFETs for VLSI Beyond Si-CMOS Scaling Limit," *University of California, Santa Barbara,* 2014.

[10] C. Y. Huang, "III-V Ultra-Thin-Body InGaAs / InAs MOSFETs for Low Standby Power Logic Applications," *University of California, Santa Barbara,* 2015.

[11] B. Markman, "III-V InxGa1-xAs / InP MOS-HEMTs for 100-340GHz Communication Systems," *University of California, Santa Barbara,* 2020.

[12] B. Markman, S. T. Š. Brunelli, M. Guidry, L. Whitaker and M. J. Rodwell, "Lg = 40nm Composite Channel MOS-HEMT Exhibiting fτ = 420 GHz, fmax = 562 GHz," *DRC,* 2021.

[13] S. M. Sze, Physics of Semiconductor Devices, New York: John Wiley & Sons, Inc., 1981.

[14] I. Jo and T. Matsuoka, "Accurate Extraction of Effective Gate Resistance in RF MOSFET," *Circuits and Systems,* vol. 6, pp. 143-151, 2015.

[15] T. Gilani and D. Rabchuk, "Electrical resistivity of gold thin film as a function of film thickness," *Canadian Journal of Physics,* 2017.

[16] H.-B. Jo, "Lg = 25 nm InGaAs/InAlAs high-electron mobility transistors with both ft and fmax in excess of 700 GHz," *Applied Physics Express,* vol. 12, no. 054006, 2019.

[17] B. L. Ooi, Z. Zhong and M.-S. Leong, "Analytical Extraction of Extrinsic and Intrinsic FET Parameters," *IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES,* vol. 57, no. 2, pp. 254-261, 2009.

[18] M. Egard et al, "High transconductance self-aligned gate-last surface channel In0.53Ga0.47As MOSFET," *2011 International Electron Devices Meeting,* pp. 13.2.1-13.2.4, 2011.

[19] M. Zhao, T. Xu, B. Chen and J. Niu, "Technology of alignment mark in electron beam lithography," *Proceedings of SPIE,* 2014.

[20] G. J. Burek, Y. Hwang, A. D. Carter, V. Chobpattana, J. J. M. Law, W. J. Mitchell, B. Thibeault, S. Stemmer and M. J. W. Rodwell, "Influence of gate metallization processes on the electrical characteristics of high-k/In0.53Ga0.47As interfaces," *Journal of Vacuum Science & Technology,* vol. 29, no. 4, 2011.

[21] H.-Y. Tseng, "Triple-heterojunction (3-HJ) TFETs Design and Fabrication for Low Power Logic," *University of California, Santa Barbara,* 2021.

[22] S. A. Campbell, Fabrication Engineering at the Micro and Nanoscale, New York: Oxford University Press, 2013.

[23] M. J. Loboda, C. M. Grove and R. F. Schneider, "Properties of a - SiOx:H Thin Films Deposited from Hydrogen Silsesquioxane Resins," *J. Electrochem. Soc,* vol. 145, no. 8, pp. 2861-2866, 1998.

[24] Y. Huang, J.-H. Ryou, R. D. Dupuis, C. Pflugl, F. Capasso, K. Sun, A. M. Fischer and F. A. Ponce, "deposition, Optimization of growth conditions for InGaAs/InAlAs/InP quantum cascade lasers by metalorganic chemical vapor," *Journal of Crystal Growth,* vol. 316, no. 1, pp. 75-80, 2011.

[25] H. Heinecke, M. Wachter and U. Schoffel, "Facet formation and characterization of III-V structures grown on patterned surfaces," *Microelectronics Journal,* vol. 28, pp. 803-815, 1997.

[26] D.-H. Kim and J. A. d. Alamo, "30-nm InAs Pseudomorphic HEMTs on an InP Substrate With a Current-Gain Cutoff Frequency of 628 GHz," *IEEE ELECTRON DEVICE LETTERS,* vol. 29, no. 8, pp. 830-833, 2008.

[27] V. Chobpattana, J. Son, J. J. M. Law, R. Engel-Herbert, C. Y. Huang and a. S. Stemmer, "“Nitrogen-passivated dielectric/InGaAs interfaces with sub-nm equivalent oxide thickness and low interface trap densities," *Appl. Phys. Lett.,* vol. 102, no. 2, pp. 100-103, 2013.

[28] T. Takahagi, I. Nagai, A. Ishitani, H. Kuroda and Y. Nagasawa, "The formation of hydrogen passivated silicon single-crystal surfaces using ultraviolet

cleaning and HF etching," *Journal of Applied Physics,* vol. 64, pp. 3516-3521, 1988.

[29] Y. Fang, "Regrown Extrinsic Base InP HBT with Sub-100nm Emitter Contact," *University of California, Santa Barbara,* 2021.

[30] P. Walker and W. H. Tarn, Handbook of Metal Etchants, Boca Raton: CRC Press, 1991.

[31] A. Hugger, A. Dlugolecka, H. Stieglauer, R. Ehrbrecht and M. Hosch, "Impact of Water Content in NMP on Ohmic Contacts in GaN HEMT Technologies," *IEEE TRANSACTIONS ON SEMICONDUCTOR MANUFACTURING,* vol. 33, no. 4, pp. 552-556, 2020.

[32] M. Egard, L. Ohlsson, M. Ärlelid, K.-M. Persson, B. M. Borg, F. Lenrick, R. Wallenberg, E. Lind and a. L.-E. Wernersson, "High-Frequency Performance of Self-Aligned Gate-Last Surface Channel In0.53Ga0.47As MOSFET," *IEEE ELECTRON DEVICE LETTERS,* vol. 33, no. 3, pp. 369-371, 2012.

[33] P. H. L. Noten, "The Etching of InP in HCI Solutions: A Chemical Mechanism," *Journal of The Electrochemical Society,* vol. 131, no. 11, pp. 2641-2644, 1984.

[34] M. Rodwell, "Picosecond Electrical Wafront Generation and Picosecond optoelectronic instrumentation," *Standford University,* 1987.

[35] J. Skriniarova, J. Kovac, J. Breza and D. Gregusova, "Wet Etching of InGaP and GaAs in HCl: H3P04: H202," *Sensors and Materials,* pp. 213-218, 1998.

[36] J. C. Lin, S. Y. Yu and a. S. E. Mohney, "Characterization of low-resistance ohmic contacts to n- and p-type InGaAs," *J. Appl. Phys.,* vol. 114, 2013.

[37] S. Lee, "Design , Fabrication , and Characterization of High Performance III-V nMOSFETs for VLSI Beyond Si-CMOS Scaling Limit," *University of California, Santa Barbara,* 2014.

[38] K. Natori, "Ballistic metal-oxide-semiconductor field effect transistor," *J. Appl. Phys.,* pp. 4879-4890, 1998.

[39] A. Tessmann, A. Leuther, F. Heinz, F. Bernhardt, L. John, H. Massler, L. Czornomaz and T. Merkle, "20-nm In0.8Ga0.2As MOSHEMT MMIC Technology on Silicon," *IEEE JOURNAL OF SOLID-STATE CIRCUITS,* vol. 54, no. 9, pp. 2411-2418, 2019.

[40] D.-H. Kim, B. Brar and J. A. d. Alamo, "fT = 688 GHz and fmax = 800 GHz in Lg = 40 nm In0.7Ga0.3As MHEMTs with gm_max > 2.7 mS/μm," *IEDM,* 2011.

[41] G. DAMBRINE, A. CAPPY, F. HELIODORE and E. PLAYEZ, "A New Method for Determining the FET Small-Signal Equivalent Circuit," *IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES,* vol. 36, no. 7, pp. 1151-1159, 1988.

Appendix 1 – Generation 2.1 Process flow

#.#		Name	Substep name	tool	Process
1	1	Alignment Marks	Hard Mask Deposition	Oxford-FlexAL ALD	**USE SILICON WITNESS** TMA+H2O-300C for 50 cycles
1	2		Measure Alumina Thicknesses	J.A. Woolam	Measure Al2O3 Thickness
1	3		Spin SPR 955-0.9	PR Bench	1) Dispense SPR 955-0.9, wait 30s 2) Spin 4000 RPMs for 30s
1	4		Pre-Bake	PR Bench	Bake 90°C for 90s
1	5		Expose Alignment Marks	GCA200	Mask = 0-FET-ALIGN, Job = RFMARK\MARK Focus-offset = 0, Exposure-time = 0.50 s
1	6		Post-Bake	PR Bench	Bake 110°C for 90s
1	7		Develop	Develop Bench	1) AZ300-MIF for 60s 2) DI Rinse 60s
1	7		Optical Check	Optical Microscope	Check how the Lithography looks
1	8		Hard-Bake	PR Bench	Bake 120°C for 15mins
1	9		Etch Alignment Marks	Acid Bench	1. HF for 8s to remove 5nm Al2O3 (2 minute rinse) 2. 250 mL H2O | 10 mL H3PO4 | 10 mL H2O2 (fresh squirt bottles) stir at 600 rpm for 10 minutes 13 nm channel + 106 nm BB = 119 nm etch (2nm/s) 150%*(119/2) = **90 second etch** (2 minute rinse) **STIR WHILE ETCHING** 3. 100 mL H2O | 100 mL HCl (directly from bottles) stir at 600 rpm for 10 minutes 1 um etch (8nm/s) 100%*(1000/8) = **2 minute etch** (2 minute rinse)
1	10		Strip Resist	Isothermal Bath	1. NMP at 80°C for 1 hours 2. IPA/DI rinse
1	11		Solvent Clean	Solvent Bench	Acetone/IPA/DI rinse 60s
1	12		Optical Check	Optical Microscope	Check how the marks look
1	13		Yes Plasma clean	Yes plasma clean	180-C-0.7 kV-5 minutes
1	13		Remove Hard Mask	HF Bench	1. BHF for 2mins 2. DI rinse for 2mins
2	1	S/D regrowth (Dummy Gate 2)	Solvent Clean	Solvent Bench	Acetone/IPA/DI rinse 5 minutes
2	2		Dehydration	PR Bench	Bake 110°C for 5mins
2	3		Adhesion Layer Deposition	Oxford-FlexAL ALD	**USE SILICON WITNESS** TMA+H2O-300C for 10 cycles
2	4		Spin 2% HSQ	PR Bench	1) Dispense 2% HSQ, wait 30s 2) Spin 5000 RPMs for 30s

2	5		Pre-Bake	PR Bench	Bake 200°C for 120s
2	6		EBL Exposure	JEOL 6300	500 pA, Aperture 5, Dose 5000 uC/cm^2
2	7		Develop	Develop Bench	1. NaOH:NaCl:H2O = 2g:8g:200mL for 60s (DO NOT STIR) 2. DI rinse for 5-10mins (DO NOT STIR)
2	8		Write Check	Optical Microscope	Check to see if dummy gates are visible, straight, and well adhered
2	9		Dummy Gate Bake	PR Bench	Bake 150°C for 30mins to avoid HSQ outgas in MOCVD
2	10		Digital Etch (x1)	UV Ozone Acid Bench	10 minute UV ozone HCl:H2O 1:10 for 60s (DO NOT STIR)
2	11		S/D Regrowth	Thomas Swan MOCVD	25nm 4x10^19 cm^-3 Si:InGaAs
2	12		growth check	Optical Microscope	check regrowth
3	1	Link regrowth (Dummy Gate 2)	Remove HSQ Dummy Gate	HF Bench	1. BHF for 2mins 2. DI rinse for 2mins
3	2		Adhesion Layer Deposition	Oxford-FlexAL ALD	TMA+H2O-300C for 10 cycles
3	3		Spin 2% HSQ	PR Bench	1) Dispense 2% HSQ, wait 30s 2) Spin 5000 RPMs for 30s
3	4		Pre-Bake	PR Bench	Bake 200°C for 120s
3	5		EBL Exposure	JEOL 6300	500 pA, Aperture 5, Dose 5000 uC/cm^2
3	6		Develop	Develop Bench	1. NaOH:NaCl:H2O = 2g:8g:200mL for 60s (DO NOT STIR) 2. DI rinse for 5-10mins (DO NOT STIR)
3	7		Write Check	Optical Microscope	Check to see if dummy gates are visible, straight, and well adhered
3	8		Dummy Gate Bake	PR Bench	Bake 150°C for 30mins to avoid HSQ outgas in MOCVD
3	9		Digital Etch (x1)	UV Ozone Acid Bench	10 minute UV ozone HCl:H2O 1:10 for 60s (DO NOT STIR)
3	10		S/D Regrowth	Thomas Swan MOCVD	1. 5nm 4x10^19 cm^-3 Si:InGaAs 1. 80nm UID InP
3	11		growth check	Optical Microscope	check regrowth
4	1	high - k	Solvent Clean	Solvent Bench	Acetone/IPA/DI rinse 60s
4	2		Remove HSQ Dummy Gate	HF Bench	1. BHF for 2mins 2. DI rinse for 2mins
4	3		Digital Etch (x4)	UV Ozone Acid Bench	10min UV Ozone HCl:H2O 1:10 for 60s **(SKIP LAST DIP)**
4	4		Remove Native Oxide	HF Bench	BHF for 2mins, DI rinse 60s
4	5		High-k Deposition	Oxford-FlexAL ALD	**USE SILICON WITNESS** 1. Season/shake plasma shutter CH3-TMA+100W/N*-300C for 15 cycles 2. CH3-TMA+100W/N*-300C for 9 cycles 3. CH3-TEMAZ+H2O-300C for 30 cycles
4	6		Post high-k Anneal	Oxford-FlexAL ALD	4. Bake in H2 at 350°C for 30mins

4	7		Measure High-k Thicknesses	J.A. Woolam	Measure High-k thickness
5	1		Spin Surpass/UV6	PR Bench	1) Surpass 4000 soak for 60 sec 2) DI rinse 30 sec 3) Dry with Nitrogen gun 4) UV-6.8 5) spin 3000 RPM for 30 sec
5	2		Pre-Bake	PR Bench	6) Bake 115C for 90 sec
5	3		EBL Exposure	JEOL 6300	500 pA, Aperture 5, Dose 5000 uC/cm^2
5	4		Post-Bake	Solvent Bench	Bake 135°C for 2mins
5	5		Develop	Develop Bench	1) AZ-300MIF for 60 seconds (slow stir) 2) DI rinse for 60 seconds (water flush)
5	6		litho check	Optical Microscope	Check to make sure features resolved and are aligned
5	7		Gate Metal Deposition	Thermal Evaporator	Ni/Au 20nm/200nm (x5 = 1.0kA/10kA) Rates: 1.0/3.0 Å/s
5	8		PR Strip	Isothermal Bath	1. NMP at 80°C for 2+ hours 2. IPA/DI rinse
5	9		deposition check	Optical Microscope	Check to make sure features resolved and are aligned
6	1	sacrificial removal	Solvent Clean	Solvent Bench	Acetone/IPA/DI rinse 5 minutes
6	2		remove high-k	HF Bench	1. BHF for 45s (DO NOT STIR) 2. DI rinse for 2mins (DO NOT STIR)
6	3		Solvent Clean	Solvent Bench	Acetone/IPA/DI rinse 60s
6	4		Dehydration	PR Bench	Bake 110°C for 5mins
6	5		SiNx deposition	PECVD #1	1. wet + 10 minute O2 clean 2. 2 minute chamber season 3. load sample and **witness** 4. 30 nm SiNx deposition (t=T/R = 300 A/ 2A/s = 50 sec = **2.5 min**) 5. unload samples 6. 10 minute O2 clean
6	6		Measure SiNx thickness	J.A. Woolam	Measure High-k thickness (T1)
6	7		SiNx etch (witness)	ICP #2	CF4 (20 sccm) / O2 (2 sccm) / Pressure (0.2 Pa) / Power (25 W) / Bias (19 W) / rate (12 nm/min) 1. O2 Clean ICP for 15 minutes (RECIPE 103) 2. Season chamber for 2 minutes (RECIPE 165) 3. etch witness for 1 minute (RECIPE 165)
6	8		Measure SiNx thickness	J.A. Woolam	1. Measure High-k thickness (T2) 2. R=T1-T2/60seconds = (___ - ___)/60 = _____nm/minute 3. t2=110%*(T1/R) = 1.1*(___/___)=____minute
6	9		SiNx etch (sample)	ICP #1	1. etch sample for t2 (____) minutes
6	10		Solvent Clean	Solvent Bench	Acetone/IPA/DI rinse 60s
6	11		Digital Etch (x2)	UV Ozone Acid Bench	10min UV Ozone HCl:H2O 1:10 for 60s
6	12		Solvent Clean	Solvent Bench	Acetone/IPA/DI rinse 60s
6	13		Dehydration	PR Bench	Bake 110°C for 5mins

6	14		Spin SPR 955-0.9	PR Bench	1) Dispense SPR 955-0.9, wait 30s 2) Spin 3000 RPMs for 30s
6	15		Pre-Bake	PR Bench	Bake 95°C for 90s
6	16		Expose Sacrificial Protection	MLA 150	substrate: Automatic rectangular_OptAF ***INVERT!*** Laser: 405 Dose: 240 Defocus: -6
6	17		Post-Bake	PR Bench	Bake 110°C for 90s
6	18		Develop	Develop Bench	1) AZ300-MIF for 60s 2) DI Rinse 60s
6	19		lithography check	Optical Microscope	Check to make sure features resolved and are aligned
6	20		Hard-Bake	PR Bench	Bake 120°C for 15mins
6	21		Remove Sacrificial Layer	Acid Bench	1. 100 mL HCl | 100 mL H2O (directly from bottles)stir at 600 rpm for 10 minutes ~ 250 nm undercut etch (10 nm/s)150%*(250/10) = **<u>30 second etch</u>** (2 minute rinse)
6	22		Strip Resist	Isothermal Bath	1. NMP at 80°C for 1 hours 2. IPA/DI rinse
7	1	Mesa Isolation	solvent clean	Solvent Bench	Acetone/IPA/DI rinse 60s
7	2		Dehydration	PR Bench	Bake 110°C for 5mins
7	3		optical check	Optical Microscope	Check etch
7	4		Spin SPR 955-0.9	PR Bench	1) Dispense SPR 955-0.9, wait 30s 2) Spin 3000 RPMs for 30s
7	5		Pre-Bake	PR Bench	Bake 95°C for 90s
7	6		Expose Mesa Iso	MLA 150	substrate: Automatic rectangular_OptAF ***INVERT!*** Laser: 405 Dose: 240 Defocus: -6
7	7		Post-Bake	PR Bench	Bake 110°C for 90s
7	8		Develop	Develop Bench	1) AZ300-MIF for 60s 2) DI Rinse 60s
7	9		lithography check	Optical Microscope	Check to make sure features resolved and are aligned
7	10		Hard-Bake	PR Bench	Bake 120°C for 15mins

7	11		Etch Mesa	Acid Bench	1. 250 mL H2O | 10 mL H3PO4 | 10 mL H2O2 (fresh squirt bottles) stir at 600 rpm for 10 minutes 25nm N+ 13 nm channel + 106 nm BB = 144 nm etch (2nm/s) undercut shouldn't be an issue because the channel etches faster 150%*(144/2) = **110 second etch** (2 minute rinse) **STIR WHILE ETCHING** 2. 100 mL H2O | 100 mL HCl (directly from bottles) stir at 600 rpm for 10 minutes 100 nm etch through initiation layer (8nm/s) 100%*(100/8) = **10 second etch** (2 minute rinse)
7	12		Strip Resist	Isothermal Bath	1. NMP at 80°C for 1 hours 2. IPA/DI rinse
7	13		Etch Check	dektak	Check to make sure etched into substrate
8	1	Source / Drain Vias	Solvent Clean	Solvent Bench	Acetone/IPA/DI rinse 60s
8	2		Dehydration	PR Bench	Bake 110°C for 5mins
8	3		Spin nLoff-2020	PR Bench	1) Dispense HMDS, wait 20s 2) Spin HMDS 4000 RPMs for 30 seconds (Recipe 7) 3) Dispense nLoff-2020, wait 30s 4) Spin 4000 RPMs for 30s
8	4		Pre-Bake	PR Bench	Bake 110°C for 60s
8	5		Expose S/D ohmics	MLA 150	substrate: Automatic rectangular_OptAF**INVERT!**Laser: 375Dose: 340Defocus: -3
8	6		Post-Bake	PR Bench	Bake 110°C for 60s
8	7		Develop	Develop Bench	1) AZ300-MIF for 90s 2) DI Rinse 60s
8	8		litho check	Optical Microscope	Check lithography
8	9		Surface Clean	Acid Bench	1. HCl:H2O 1:10 for 60s 2. DI rinse 60s
8	10		S/D Metal Deposition	E-Beam #4	Ti/Pd/Au 10/10/10 (Recipe 30) Rates: 0.7/1.0/1.0 Å/s
8	11		PR Strip	Isothermal Bath	1. NMP at 80°C for 2+ hours 2. IPA/DI rinse
8	12		deposition check	Optical Microscope	Check S/D Metal quality and alignment
8	13		Solvent Clean	Solvent Bench	Acetone/IPA/DI rinse 60s
8	14		Passivation deposition	Oxford-FlexAL ALD	**USE SILICON WITNESS** 1. CH3-TEMAZ+H2O-300C for 50 cycles
8	15		Post Metal Anneal	Oxford-FlexAL ALD	2. Bake in H2 at 350°C for 30mins

8	16		Spin nLoff-2020	PR Bench	1) Dispense HMDS, wait 20s 2) Spin HMDS 4000 RPMs for 30 seconds (Recipe 7) 3) Dispense nLoff-2020, wait 30s 4) Spin 4000 RPMs for 30s
8	17		Pre-Bake	PR Bench	Bake 110°C for 60s
8	18		Expose S/D vias	MLA 150	substrate: Automatic rectangular_OptAF **INVERT!** Laser: 375 Dose: 340 Defocus: -3
8	19		Post-Bake	PR Bench	Bake 110°C for 60s
8	20		Develop	Develop Bench	1) AZ300-MIF for 90s 2) DI Rinse 60s
8	21		lithography check	Optical Microscope	Check to make sure features resolved and are aligned
8	22		Hard-Bake	PR Bench	Bake 120°C for 15mins
8	23		Etch vias	Acid Bench	1. HF for 60s to remove 4nm ZrO2 (2 minute rinse)
8	24		Strip Resist	Isothermal Bath	1. NMP at 80°C for 1 hours 2. IPA/DI rinse
9	1	pad metal	Solvent Clean	Solvent Bench	Acetone/IPA/DI rinse 60s
9	2		Dehydration	PR Bench	Bake 110°C for 5mins
9	3		Spin nLoff-2020	PR Bench	1) Dispense HMDS, wait 20s 2) Spin HMDS 4000 RPMs for 30 seconds (Recipe 7) 3) Dispense nLoff-2020, wait 30s 4) Spin 4000 RPMs for 30s
9	4		Pre-Bake	PR Bench	Bake 110°C for 60s
9	5		Expose Pad metal	MLA 150	substrate: Automatic rectangular_OptAF**INVERT!**Laser: 375Dose: 340Defocus: -3
9	6		Post-Bake	PR Bench	Bake 110°C for 60s
9	7		Develop	Develop Bench	1) AZ300-MIF for 90s 2) DI Rinse 60s
9	8		litho check	Optical Microscope	Check lithography
9	9		Hard-Bake	Solvent Bench	Bake 120°C for 15mins
9	10		Pad Metal Deposition	E-Beam #4	Ti/Au 20/500nm (Recipe 9) Rates: 1/3.0 Å/s
9	11		PR Strip	Isothermal Bath	1. NMP at 80°C for 2 hours 2. IPA/DI rinse
9	12		deposition check	Optical Microscope	Check Pad Metal quality and alignment

Appendix 2 – Generation 2.2 Process flow

1	1	Alignment Marks	Hard Mask Deposition	Oxford-FlexAL ALD	**USE SILICON WITNESS** TMA+H2O-300C for 50 cycles
1	2		Measure Alumina Thicknesses	J.A. Woolam	Measure Al2O3 Thickness
1	3		Spin SPR 955-0.9	PR Bench	1) Dispense SPR 955-0.9, wait 30s 2) Spin 4000 RPMs for 30s
1	4		Pre-Bake	PR Bench	Bake 90°C for 90s
1	5		Expose Alignment Marks	MLA 150	substrate: Automatic rectangular_OptAF Laser: 405 Dose: 105 Defocus: -3
1	6		Post-Bake	PR Bench	Bake 110°C for 90s
1	7		Develop	Develop Bench	1) AZ300-MIF for 60s 2) DI Rinse 60s
1	8		Optical Check	Optical Microscope	Check how the Lithography looks
1	9		Hard-Bake	PR Bench	Bake 120°C for 10 mins
1	10		ash	Technics O2 ash	Technics O2 ash (300mT, 100W), 10 sec
1	11		Etch Alignment Marks	Acid Bench	1. HF for 8s to remove 5nm Al2O3 (2 minute rinse) 2. 250 mL H2O | 10 mL H3PO4 | 10 mL H2O2 (fresh squirt bottles) stir at 600 rpm for 10 minutes 13 nm channel + 106 nm BB = 119 nm etch (2nm/s) 150%*(119/2) = **90 second etch** (2 minute rinse) **STIR WHILE ETCHING** 3. 100 mL H2O | 100 mL HCl (directly from bottles) stir at 600 rpm for 10 minutes 1 um etch (8nm/s) 100%*(1000/8) = **90 second etch** (2 minute rinse)
1	12		Strip Resist	Isothermal Bath	1. NMP at 80°C for 2 hours 2. directly to 5 minutes IPA + 2 minutes DI
1	13		Solvent Clean	Solvent Bench	Acetone/IPA/DI rinse 60s
1	14		Optical Check	Optical Microscope	Check how the marks look
1	15		Yes Plasma clean	Yes plasma clean	180-C-0.7 kV-5 minutes
1	16		Remove Hard Mask	HF Bench	1. BHF for 2mins 2. DI rinse for 2mins
2	1	MOCVD	MOCVD bake	Thomas Swan MOCVD	bake MOCVD to remove any contaminants
2	2		MOCVD coat	Thomas Swan MOCVD	coat MOCVD in InP

2	3		MOCVD calibration	Thomas Swan MOCVD	1. 50 nm UID InP 2. 100 nm 4x10^19 cm^-3 Si:InGaAs
2	4		Doping calibration (4 point probe)	4 point probe	Rs=_____ ohms/square
3	1	S/D regrowth (Dummy Link)	Solvent Clean	Solvent Bench	Acetone/IPA/DI rinse 60s
3	2		Dehydration	PR Bench	Bake 110°C for 5mins
3	3		Adhesion Layer Deposition	Oxford-FlexAL ALD	**USE SILICON WITNESS** TMA+H2O-300C for 10 cycles
3	4		Spin 2% HSQ	PR Bench	1) Dispense 2% HSQ, wait 30s 2) Spin 5000 RPMs for 30s
3	5		Pre-Bake	PR Bench	Bake 200°C for 120s
3	6		EBL Exposure	JEOL 6300	500 pA, Aperture 5, Dose 5000 uC/cm^2
3	7		Develop	Develop Bench	1. NaOH:NaCl:H2O = 2g:8g:200mL for 60s (DO NOT STIR) 2. DI rinse for 5-10mins (DO NOT STIR)
3	8		Write Check	Optical Microscope	Check to see if dummy gates are visible, straight, and well adhered
3	9		Dummy Gate Bake	PR Bench	Bake 150°C for 30mins to avoid HSQ outgas in MOCVD
3	10		Digital Etch (x1)	UV Ozone Acid Bench	10 minute UV ozone HCl:H2O 1:10 for 60s (DO NOT STIR)
3	11		S/D Regrowth	Thomas Swan MOCVD	50nm 4x10^19 cm^-3 Si:InGaAs
4	1	Link regrowth (Dummy Gate)	Remove HSQ Dummy Gate	HF Bench	1. BHF for 2mins 2. DI rinse for 2mins
4	2		Adhesion Layer Deposition	Oxford-FlexAL ALD	TMA+H2O-300C for 10 cycles
4	3		Spin 2% HSQ	PR Bench	1) Dispense 2% HSQ, wait 30s 2) Spin 5000 RPMs for 30s
4	4		Pre-Bake	PR Bench	Bake 200°C for 120s
4	5		EBL Exposure	JEOL 6300	500 pA, Aperture 5, Dose 5000 uC/cm^2
4	6		Develop	Develop Bench	1. NaOH:NaCl:H2O = 2g:8g:200mL for 60s (DO NOT STIR) 2. DI rinse for 5-10mins (DO NOT STIR)
4	7		Write Check	Optical Microscope	Check to see if dummy gates are visible, straight, and well adhered
4	8		Dummy Gate Bake	PR Bench	Bake 150°C for 30mins to avoid HSQ outgas in MOCVD
4	9		Digital Etch (x1)	UV Ozone Acid Bench	10 minute UV ozone HCl:H2O 1:10 for 60s (DO NOT STIR)
4	10		sacrificial Regrowth	Thomas Swan MOCVD	1. 80nm UID InP
5	1	Mesa Isolation	solvent clean	Solvent Bench	Acetone/IPA/DI rinse 60s
5	2		Dehydration	PR Bench	Bake 110°C for 5mins
5	3		Hard Mask Deposition	Oxford-FlexAL ALD	**USE SILICON WITNESS** TMA+H2O-300C for 50 cycles
5	4		Measure Alumina Thicknesses	J.A. Woolam	Measure Al2O3 Thickness

5	5		Spin SPR 955-0.9	PR Bench	1) Dispense SPR 955-0.9, wait 30s 2) Spin 3000 RPMs for 30s
5	6		Pre-Bake	PR Bench	Bake 95°C for 90s
5	7		Expose Mesa Iso	MLA 150	substrate: Automatic rectangular_OptAF ***INVERT!*** Laser: 405 Dose: 240 Defocus: -6
5	8		Post-Bake	PR Bench	Bake 110°C for 90s
5	9		Develop	Develop Bench	1) AZ300-MIF for 60s 2) DI Rinse 60s
5	10		lithography check	Optical Microscope	Check to make sure features resolved and are aligned
5	11		Hard-Bake	PR Bench	Bake 120°C for 15mins
5	12		Etch Mesa	Acid Bench	1. HF for 8s to remove 5nm Al2O3 (2 minute rinse)2. **200 mL HCPO4 | 50 mL HCl** (directly from bottles)stir at 600 rpm for 15 minutes 100 nm etch through sacrificial layer (15nm/s)400%*(100/15) = 30 second etch (2 minute rinse)3. 250 mL H2O | 10 mL H3PO4 | 10 mL H2O2 (fresh squirt bottles)stir at 600 rpm for 10 minutes 25nm N+ 13 nm channel + 106 nm BB = 144 nm etch (2nm/s)150%*(144/2) = **110 second etch** (2 minute rinse)**STIR WHILE ETCHING**4. 100 mL HCl | 100 mL H2O (directly from bottles)stir at 600 rpm for 10 minutes 10 second etch (2 minute rinse)
5	13		Strip Resist	Isothermal Bath	1. NMP at 80°C for 2 hours 2. IPA/DI rinse
5	14		Etch Check	dektak	Check to make sure etched into substrate
6	1	high - k	Solvent Clean	Solvent Bench	Acetone/IPA/DI rinse 60s
6	2		Remove HSQ Dummy Gate / Adhesion layer	HF Bench	1. BHF for 2mins 2. DI rinse for 2mins
6	3		Digital Etch (x6)	UV Ozone Acid Bench	10min UV Ozone HCl:H2O 1:10 for 60s + H2O for 60s **(DO NOT STIR) (SKIP LAST DIP)**
6	4		Remove Native Oxide	HF Bench	BHF for 2mins, DI rinse 60s
6	5		High-k Deposition	Oxford-FlexAL ALD	**USE SILICON WITNESS** 1. Season CH3-TMA+100W/N*-300C for 15 cycles 2. CH3-TMA+100W/N*-300C for 9 cycles 3. CH3-TEMAZ+H2O-300C for 30 cycles
6	6		Post high-k Anneal	Oxford-FlexAL ALD	4. Bake in H2 at 350°C for 30mins

6	7		Measure High-k Thicknesses	J.A. Woolam	Measure High-k thickness
7	1		Spin Surpass/UV6	PR Bench	1) Surpass 4000 soak for 60 sec 2) DI rinse 30 sec 3) Dry with Nitrogen gun 4) UV-6.8 5) spin 3000 RPM for 30 sec
7	2		Pre-Bake	PR Bench	6) Bake 115C for 90 sec
7	3		EBL Exposure	JEOL 6300	500 pA, Aperture 5, Dose 5000 uC/cm^2
7	4		Post-Bake	Solvent Bench	Bake 135°C for 2mins
7	5		Develop	Develop Bench	1) AZ-300MIF for 60 seconds (slow stir) 2) DI rinse for 60 seconds (water flush)
7	6		litho check	Optical Microscope	Check to make sure features resolved and are aligned
7	7		Gate Metal Deposition	Thermal Evaporator	Ni/Au 20nm/300nm (x5 = 1.0kA/15kA) Rates: 1.0/3.0 Å/s
7	8		PR Strip	Isothermal Bath	1. NMP at 80°C for 2+ hours2. IPA/DI rinse
8	1	Sidewall & InP removal	Solvent Clean	Solvent Bench	Acetone/IPA/DI rinse 60s
8	2		remove high-k	HF Bench	1. BHF for 45s (DO NOT STIR) 2. DI rinse for 2mins (DO NOT STIR)
8	3		SiNx deposition	PECVD #1	1. 10 minute O2 clean 2. 2 minute chamber season 3. load sample and **witness** 4. 30 nm SiNx deposition (t=T/R = 300 A/ 2A/s = 50 sec = **2.5 min**) 5. unload samples 6. 10 minute O2 clean
8	4		Ellipsometry	J.A. Woolam	Oxide thickness (on silicon): T1=_____ nm
8	5		SiNx etch (witness)	ICP #1	CF4 (20 sccm) / O2 (2 sccm) / Pressure (0.2 Pa) / Power (25 W) / Bias (19 W) / rate (12 nm/min) 1. O2 Clean ICP for 15 minutes (RECIPE 103) 2. Season chamber for 2 minutes (RECIPE 165) 3. etch witness for 1 minute (RECIPE 165)
8	6		Measure SiNx thickness	J.A. Woolam	1. Measure High-k thickness (T2) 2. R=T1-T2/60seconds = (___ - ___)/60 =____nm/s=____nm/min 3. t2=110%*(T1/R) = 1.1*(___/___)=_____minutes
8	7		SiNx etch (sample)	ICP #2	PLACE WITNESS UNDER LASER MONITOR 1. etch sample for t2 (____) minutes (RECIPE 165) 2. CF4/O2 Clean ICP for 10 minutes (RECIPE 106) (CF4/O2)
8	8		Digital Etch (x2)	UV Ozone Acid Bench	10min UV Ozone HCl:H2O 1:10 for 60s
8	9		Solvent Clean	Solvent Bench	Acetone/IPA/DI rinse 60s
8	10		Dehydration	PR Bench	Bake 110°C for 5mins

8	11		Spin SPR 955-0.9	PR Bench	1) Dispense SPR 955-0.9, wait 30s 2) Spin 3000 RPMs for 30s
8	12		Pre-Bake	PR Bench	Bake 95°C for 90s
8	13		Expose InP protection	MLA 150	substrate: Automatic rectangular_OptAF ***INVERT!*** Laser: 405 Dose: 240 Defocus: -6
8	14		Post-Bake	PR Bench	Bake 110°C for 90s
8	15		Develop	Develop Bench	1) AZ300-MIF for 60s 2) DI Rinse 60s
8	16		lithography check	Optical Microscope	Check to make sure features resolved and are aligned
8	17		Hard-Bake	PR Bench	Bake 120°C for 15mins
8	18		Remove Sacrificial Layer	Acid Bench	1. 100 mL HCl | 100 mL H2O (directly from bottles) stir at 600 rpm for 10 minutes ~ 250 nm undercut etch (10 nm/s) 150%*(250/10) = 4**0 second etch** (2 minute rinse)
8	19		PR Strip	Isothermal Bath	1. NMP at 80°C for 2+ hours 2. IPA/DI rinse
9	1	Ohmics	Solvent Clean	Solvent Bench	Acetone/IPA/DI rinse 60s
9	2		Dehydration	PR Bench	Bake 110°C for 5mins
9	3		Spin Surpass/CSAR	PR Bench	1) Surpass 4000 soak for 60 sec 2) DI rinse 30 sec 3) blow dry 4) Spin 100% CSAR 3000 RPMs for 30 seconds
9	4		CSAR prebake	PR Bench	5) Bake 180°C for 5 mins
9	5		EBL Exposure	JEOL 6300	2 nA, Aperture 6, Dose 230 uC/cm^2
9	6		Develop	Solvent Bench	1) Amyl Acetate for 75 seconds 2) IPA rinse for 20 seconds
9	7		litho check	Optical Microscope	Check to make sure features resolved and are aligned
9	8		Digital Etch (x1)	UV Ozone Acid Bench	10min UV Ozone HCl:H2O 1:10 for 60s
9	9		S/D Metal Deposition	E-Beam #4	let pump for 2 full hours run Ti dep with shutter closed for 2 minutes to get oxygen Pd/Ti/Pt/Au 9/15/15/10 Rates: 0.7/1.0/1.0/1.0 Å/s
9	10		PR Strip	Isothermal Bath	1. NMP at 80°C for 2+ hours 2. IPA/DI rinse
9	11		deposition check	Optical Microscope	Check S/D Metal quality and alignment
10	1	Passivate	Solvent Clean	Solvent Bench	Acetone/IPA/DI rinse 60s
10	2		Passivation deposition	Oxford-FlexAL ALD	**USE SILICON WITNESS** 1. CH3-TDMAS+250W/O*-300C for 42 cycles
10	3		Post Metal Anneal	Oxford-FlexAL ALD	2. Bake in H2 at 350°C for 30mins

11	1	vias	Spin nLoff-2020	PR Bench	1) Dispense HMDS, wait 20s 2) Spin HMDS 4000 RPMs for 30 seconds (Recipe 7) 3) Dispense nLoff-2020, wait 30s 4) Spin 4000 RPMs for 30s
11	2		Pre-Bake	PR Bench	Bake 110°C for 60s
11	3		Expose S/D vias	MLA 150	substrate: Automatic rectangular_OptAF INVERT! Laser: 375 Dose: 340 Defocus: -3
11	4		Post-Bake	PR Bench	Bake 110°C for 60s
11	5		Develop	Develop Bench	1) AZ300-MIF for 90s 2) DI Rinse 60s
11	6		lithography check	Optical Microscope	Check to make sure features resolved and are aligned
11	7		Etch vias	Acid Bench	1. BHF etch vias in 3 nm SiO2 for 5 seconds (2 minute rinse)
11	8		Strip Resist	Isothermal Bath	1. NMP at 80°C for 2 hours 2. IPA/DI rinse
12	1	pad metal	Solvent Clean	Solvent Bench	Acetone/IPA/DI rinse 60s
12	2		Dehydration	PR Bench	Bake 110°C for 5mins
12	3		Spin nLoff-2020	PR Bench	1) Dispense HMDS, wait 20s2) Spin HMDS 4000 RPMs for 30 seconds (Recipe 7)3) Dispense nLoff-2020, wait 30s4) Spin 4000 RPMs for 30s
12	4		Pre-Bake	PR Bench	Bake 110°C for 60s
12	5		Expose Pad metal	MLA 150	substrate: Automatic rectangular_OptAF INVERT! Laser: 375 Dose: 340 Defocus: -3
12	6		Post-Bake	PR Bench	Bake 110°C for 60s
12	7		Develop	Develop Bench	1) AZ300-MIF for 90s 2) DI Rinse 60s
12	8		litho check	Optical Microscope	Check lithography
12	9		Pad Metal Deposition	E-Beam #4	Ti/Au 20/500nm (Recipe 9) Rates: 1/3.0 Å/s
12	10		PR Strip	Isothermal Bath	1. NMP at 80°C for 2 hours 2. IPA/DI rinse
12	11		deposition check	Optical Microscope	Check Pad Metal quality and alignment

Appendix 3 – Generation 2.3 Process flow

#.#		Name	Substep name	tool	Process
1	1	Alignment Marks	Hard Mask Deposition	Oxford-FlexAL ALD	**USE SILICON WITNESS** TMA+H2O-300C for 50 cycles
1	2		Measure Alumina Thicknesses	J.A. Woolam	Measure Al2O3 Thickness = t0 = ____ nm ; t1 = _____nm
1	3		Spin SPR 955-0.9	PR Bench	1) Dispense SPR 955-0.9, wait 30s 2) Spin 4000 RPMs for 30s
1	4		Pre-Bake	PR Bench	Bake 90°C for 90s
1	5		Expose Alignment Marks	MLA 150	substrate: Automatic rectangular_OptAF Laser: 405 Dose: 105 Defocus: -3
1	6		Post-Bake	PR Bench	Bake 110°C for 90s
1	7		Develop	Develop Bench	1) AZ300-MIF for 60s 2) DI Rinse 60s
1	8		Optical Check	Optical Microscope	Check how the Lithography looks
1	9		Hard-Bake	PR Bench	Bake 120°C for 10 mins
1	10		ash	Technics O2 ash	Technics O2 ash (300mT, 100W), 10 sec
1	11		Etch Alignment Marks	Acid Bench	1. HF for 8s to remove 5nm Al2O3 (2 minute rinse) 2. 250 mL H2O | 10 mL H3PO4 | 10 mL H2O2 (fresh squirt bottles) stir at 600 rpm for 10 minutes 13 nm channel + 106 nm BB = 119 nm etch (2nm/s) 150%*(119/2) = **90 second etch** (2 minute rinse) **STIR WHILE ETCHING** 3. 100 mL H2O | 100 mL HCl (directly from bottles) stir at 600 rpm for 10 minutes 1 um etch (8nm/s) 100%*(1000/8) = **90 second etch** (2 minute rinse)
1	12		Strip Resist	Isothermal Bath	1. NMP at 80°C for 2 hours 2. directly to 5 minutes IPA + 2 minutes DI
1	13		Solvent Clean	Solvent Bench	Acetone/IPA/DI rinse 60s
1	14		Optical Check	Optical Microscope	Check how the marks look
1	15		Yes Plasma clean	Yes plasma clean	180-C-0.7 kV-5 minutes
2	1	MOCVD setup	MOCVD bake	Thomas Swan MOCVD	bake MOCVD to remove any contaminants
2	2		MOCVD coat	Thomas Swan MOCVD	coat MOCVD in InP
2	3		MOCVD calibration	Thomas Swan MOCVD	1. 50 nm UID InP 2. 100 nm 4x10^19 cm^-3 Si:InGaAs
2	4		Doping calibration (4 point probe)	4 point probe	Rs=_____ ohms/square
3	1	Dummy Link + S/D Regrowths	Remove Hard Mask	HF Bench	1. BHF for 2mins 2. DI rinse for 2mins
3	2		Adhesion Layer Deposition	Oxford-FlexAL ALD	TMA+H2O-300C for 10 cycles
3	3		Spin 2% HSQ	PR Bench	1) Dispense 2% HSQ, wait 30s 2) Spin 5000 RPMs for 30s

3	4		Pre-Bake	PR Bench	Bake 200°C for 120s
3	5		Dummy link exposure	JEOL 6300	500 pA, Aperture 5, Dose 5000 uC/cm^2
3	6		Develop	Develop Bench	1. NaOH:NaCl:H2O = 3g:12g:300mL for 60s (DO NOT STIR) 2. DI rinse for 1 mins (DO NOT STIR) 3. switch out water 4. DI rinse for 5 mins (DO NOT STIR)
3	7		Write Check	Optical Microscope	Check to see if dummy gates are visible, straight, and well adhered
3	8		Dummy Gate Bake	PR Bench	Bake 150°C for 30mins to avoid HSQ outgas in MOCVD
3	9		Digital Etch (x1)	UV Ozone Acid Bench	10 minute UV ozone HCl:H2O 1:10 for 60s (DO NOT STIR)
3	10		S/D Regrowth	Thomas Swan MOCVD	1. 50 nm 4x10^19 cm^-3 Si:InGaAs
3	11		Growth Check	Optical Microscope	Check to make sure growth is smooth no major impurities on wafer
4	1	Dummy gate + sacrificial regrowth	Remove Hard Mask	HF Bench	1. BHF for 2mins 2. DI rinse for 2mins
4	2		Adhesion Layer Deposition	Oxford-FlexAL ALD	TMA+H2O-300C for 10 cycles
4	3		Spin 2% HSQ	PR Bench	1) Dispense 2% HSQ, wait 30s 2) Spin 5000 RPMs for 30s
4	4		Pre-Bake	PR Bench	Bake 200°C for 120s
4	5		Dummy gate Exposure	JEOL 6300	500 pA, Aperture 5, Dose 5000 uC/cm^2
4	6		Develop	Develop Bench	1. NaOH:NaCl:H2O = 3g:12g:300mL for 60s (DO NOT STIR) 2. DI rinse for 1 mins (DO NOT STIR) 3. switch out water 4. DI rinse for 5 mins (DO NOT STIR)
4	7		Write Check	Optical Microscope	Check to see if dummy gates are visible, straight, and well adhered
4	8		Dummy Gate Bake	PR Bench	Bake 150°C for 30mins to avoid HSQ outgas in MOCVD
4	9		Digital Etch (x1)	UV Ozone Acid Bench	10 minute UV ozone HCl:H2O 1:10 for 60s (DO NOT STIR)
4	10		sacrificial Regrowth	Thomas Swan MOCVD	1. 5 nm UID InGaAs 2. 80 nm UID InP
5	1	high - k	Solvent Clean	Solvent Bench	Acetone/IPA/DI rinse 60s
5	2		Remove HSQ Dummy Gate / Adhesion layer	HF Bench	1. BHF for 2mins 2. DI rinse for 2mins
5	3		Digital Etch (x8)	UV Ozone Acid Bench	10min UV Ozone HCl:H2O 1:10 for 60s + H2O for 60s **(SKIP LAST DIP)**
5	4		Remove Native Oxide	HF Bench	BHF for 2mins, DI rinse 60s
5	5		High-k Deposition	Oxford-FlexAL ALD	**USE SILICON WITNESS** 1. Season/shake plasma shutter CH3-TMA+100W/N*-300C for 15 cycles 2. move carrier wafer into load lock and place "DO NOT USE" sign 3. BHF 2 min + H2O 1 min 4. load wafer IMMEDIATELY after dip 5. CH3-TMA+100W/N*-300C for 9 cycles 6. CH3-TEMAZ+H2O-300C for 30 cycles
5	6		Post high-k Anneal	Oxford-FlexAL ALD	7. Bake in H2 at 350°C for 30mins

5	7		Measure High-k Thicknesses	J.A. Woolam	Measure High-k thickness. T0 = ____ nm ; T1 = ____ nm
6	1	V-gate dep	Spin Surpass/UV6	PR Bench	1) Surpass 4000 soak for 60 sec 2) DI rinse 30 sec 3) Dry with Nitrogen gun 4) UV-6.8 5) spin 3000 RPM for 30 sec
6	2		Pre-Bake	PR Bench	6) Bake 115C for 90 sec
6	3		EBL Exposure	JEOL 6300	500 pA, Aperture 5, Dose 80 uC/cm^2
6	4		Post-Bake	Solvent Bench	Bake 135°C for 2mins
6	5		Develop	Develop Bench	1) AZ-300MIF for 60 seconds (slow stir)2) DI rinse for 60 seconds
6	6		litho check	Optical Microscope	Check to make sure features resolved and are aligned
6	7		Gate Metal Deposition	Thermal Evaporator	Raise height of stage using aluminum pieces (cuts rate to 20%) Ni/Au 30nm/300nm (x5 = 1.5kA/15kA)
6	8		PR Strip	Isothermal Bath	1. NMP at 80°C for 2 hours 2. directly to 5 minutes IPA + 2 minutes DI
7	1	Sacrificial removal	remove high-k	HF Bench	1. BHF for 45s (DO NOT STIR) 2. DI rinse for 2mins (DO NOT STIR)
7	2		SiNx deposition	PECVD #1	1. wet + 10 minute O2 clean 2. 2 minute chamber season 3. load sample and **witness** 4. 30 nm SiNx deposition (t=T/R = 300 A/ 2A/s = 50 sec = **2.5 min**) 5. unload samples 6. 10 minute O2 clean
7	3		Ellipsometry	J.A. Woolam	Oxide thickness (on silicon): T1=_____ nm
7	4		Spin SPR 955-0.9	PR Bench	1) Dispense SPR 955-0.9, wait 30s 2) Spin 3000 RPMs for 30s
7	5		Pre-Bake	PR Bench	Bake 95°C for 90s
7	6		Expose InP protection	MLA 150	substrate: Automatic rectangular_OptAF always use field alignment ***INVERT!*** Laser: 405 Dose: 240 Defocus: -6
7	7		Post-Bake	PR Bench	Bake 110°C for 90s
7	8		Develop	Develop Bench	1) AZ300-MIF for 60s 2) DI Rinse 60s
7	9		lithography check	Optical Microscope	Check to make sure features resolved and are aligned
7	10		SiNx etch (witness)	ICP #2	CF4 (20 sccm) / O2 (2 sccm) / Pressure (0.2 Pa) / Power (25 W) / Bias (19 W) / rate (12 nm/min) 1. O2 Clean ICP for 15 minutes (RECIPE 103) 2. Season chamber for 2 minutes (RECIPE 165) 3. etch witness for 1 minute (RECIPE 165)
7	11		Measure SiNx thickness	J.A. Woolam	1. Measure oxide thickness (T2 _____ nm) 2. R=T1-T2 =_____nm/min 3. t2=120%*(T1/R) = 1.2*(_____/_____)=_____minutes
7	12		SiNx etch (sample)	ICP #2	1. etch sample for t2 (____) minutes (RECIPE 165)

7	13		Measure SiNx thickness	J.A. Woolam	1. Measure High-k thickness (T3 _____ nm) *--> if T3 > 3 nm etch again* *2. R=(T2-T3)/t2 =_____nm/min* *3. t3=120%*(T3/R) =* *1.2*(_____/_____)=_____minutes*
7	14		SiNx etch (sample)	ICP #2	*1. etch sample for t3 (____) minutes (RECIPE 165)* 2. O2 Clean ICP for 10 minutes (RECIPE 103) (O2)
7	15		Measure SiNx thickness	J.A. Woolam	1. Measure High-k thickness (T4 _____ nm)
7	16		UV Ozone	UV Ozone	5 min UV flood exposure
7	17		PR Strip	Isothermal Bath	1. NMP at 80°C for 2 hours 2. directly to 5 minutes IPA + 2 minutes DI
7	18		PR strip	Asher	2 minute Oxygen ash (300/100)
7	19		UV Ozone	UV Ozone	10min UV Ozone
7	20		Remove Sacrificial Layer	Acid Bench	1. 100 mL HCl | 100 mL H2O (directly from bottles)stir at 600 rpm for 10 minutes **<u>2 minute etch</u>** (2 minute rinse)
7	21		Dehydration	PR Bench	Bake 110°C for 5mins
8	1	mesa isolation	Spin SPR 955-0.9	PR Bench	1) Dispense SPR 955-0.9, wait 30s 2) Spin 3000 RPMs for 30s
8	2		Pre-Bake	PR Bench	Bake 95°C for 90s
8	3		Expose Mesa Iso	MLA 150	substrate: Automatic rectangular_OptAF ***INVERT!*** Laser: 405 Dose: 240 Defocus: -6
8	4		Post-Bake	PR Bench	Bake 110°C for 90s
8	5		Develop	Develop Bench	1) AZ300-MIF for 60s 2) DI Rinse 60s
8	6		lithography check	Optical Microscope	Check to make sure features resolved and are aligned
8	7		hard bake	hot plate	Hard bake 120°C for 15 min
8	8		Etch Mesa	Acid Bench	1. 250 mL H2O | 10 mL H3PO4 | 10 mL H2O2 (fresh squirt bottles) stir at 600 rpm for 10 minutes 25nm N+ 13 nm channel + 106 nm BB = 144 nm etch (2nm/s) 150%*(144/2) = **<u>2 minute etch</u>** (2 minute rinse) **<u>STIR WHILE ETCHING</u>** 2. 100 mL HCl | 100 mL H2O (directly from bottles) stir at 600 rpm for 10 minutes 100 nm etch through sacrificial layer (15nm/s) 400%*(100/15) = 10 second etch (2 minute rinse)
8	9		UV Ozone	UV Ozone	5 min UV flood exposure
8	10		Strip Resist	Isothermal Bath	1. NMP at 80°C for 2 hours 2. directly to 5 minutes IPA + 2 minutes DI
9	1	SD ohmics	Spin nLoff-2020	PR Bench	1) Dispense HMDS, wait 20s 2) Spin HMDS 4000 RPMs for 30 seconds (Recipe 7) 3) Dispense nLoff-2020, wait 30s 4) Spin 4000 RPMs for 30s
9	2		Pre-Bake	PR Bench	Bake 110°C for 60s
9	3		Expose S/D Ohmics	MLA 150	substrate: Automatic rectangular_OptAF INVERT! Laser: 375 Dose: 340 Defocus: -3 GLOBAL MARK: -500, 0

9	4		Post-Bake	PR Bench	Bake 110°C for 60s
9	5		Develop	Develop Bench	1) AZ300-MIF for 90s 2) DI Rinse 60s
9	6		litho check	Optical Microscope	Check to make sure features resolved and are aligned
9	7		Digital Etch (x1)	UV Ozone Acid Bench	10min UV Ozone HCL:H2O 1:10 dip for 60 s H2O rinse for 60 s
9	8		S/D Metal Deposition	E-Beam #4	let pump for 2 full hours (try to get in the e-7 range if possible) Pd/Ti/Pt/Au 9/15/15/100 Rates: 0.7/1.0/1.0/1.0 Å/s
9	9		PR Strip	Isothermal Bath	1. NMP at 80°C for 2 hours 2. directly to 5 minutes IPA + 2 minutes DI
9	10		deposition check	Optical Microscope	Check S/D Metal quality and alignment
10	1	Passivate/ vias	Solvent Clean	Solvent Bench	Acetone/IPA/DI rinse 60s
10	2		Passivation deposition	Oxford-FlexAL ALD	**USE SILICON WITNESS**1. CH3-TEMAZ+H2O-300C for 30 cycles
10	3		Post Metal Anneal	Oxford-FlexAL ALD	2. Bake in H2 at 350°C for 30mins
10	4		Measure High-k Thicknesses	J.A. Woolam	Measure High-k thickness. T0 = ____ nm ; T1 = ____ nm
10	5		Spin nLoff-2020	PR Bench	1) Dispense HMDS, wait 20s 2) Spin HMDS 4000 RPMs for 30 seconds (Recipe 7) 3) Dispense nLoff-2020, wait 30s 4) Spin 4000 RPMs for 30s
10	6		Pre-Bake	PR Bench	Bake 110°C for 60s
10	7		Expose S/D vias	MLA 150	substrate: Automatic rectangular_OptAF INVERT! Laser: 375 Dose: 340 Defocus: -3 GLOBAL MARK: -500, 0
10	8		Post-Bake	PR Bench	Bake 110°C for 60s
10	9		Develop	Develop Bench	1) AZ300-MIF for 90s 2) DI Rinse 60s
10	10		lithography check	Optical Microscope	Check to make sure features resolved and are aligned
10	11		Etch vias	Acid Bench	1. BHF etch vias in 3 nm ZrO2 + 30 nm SiN 45s etch for 3 nm ZrO2 + 30 nm SiN / 84 nm/min = 22 seconds for 80 seconds (2 minute rinse)
10	12		Strip Resist	Isothermal Bath	1. NMP at 80°C for 2 hours 2. directly to 5 minutes IPA + 2 minutes DI
10	13		litho check	Optical Microscope	Check lithography
11	1	Pad metal	Dehydration	PR Bench	Bake 110°C for 5mins
11	2		Spin nLoff-2020	PR Bench	1) Dispense HMDS, wait 20s 2) Spin HMDS 4000 RPMs for 30 seconds (Recipe 7) 3) Dispense nLoff-2020, wait 30s 4) Spin 4000 RPMs for 30s
11	3		Pre-Bake	PR Bench	Bake 110°C for 60s

11	4		Expose S/D Ohmics	MLA 150	substrate: Automatic rectangular_OptAF INVERT! Laser: 375 Dose: 340 Defocus: -3 GLOBAL MARK: -500, 0
11	5		Post-Bake	PR Bench	Bake 110°C for 60s
11	6		Develop	Develop Bench	1) AZ300-MIF for 90s 2) DI Rinse 60s
11	7		litho check	Optical Microscope	Check lithography
11	8		Pad Metal Deposition	E-Beam #4	Ti/Au 20/500nm
11	9		PR Strip	Isothermal Bath	1. NMP at 80°C for 2 hours 2. directly to 5 minutes IPA + 2 minutes DI
11	10		deposition check	Optical Microscope	Check Pad Metal quality and alignment