University of California, Santa Barbara
Department of Electrical and Computer Engineering

ECE 189A/B – Senior Computer Systems Project

Course Fact Sheet

Catalog Description
Prerequisite: ECE 153B; senior standing in Computer Engineering, Computer Science or EE. Enrollment Comments: Not open for credit to students who have completed Computer Science 189A-B.

Student groups design a significant computer-based project. Groups work independently with interaction among groups via interface specifications and informal meetings.

Instructor
Dr. John M. Johnson (johnson@ece.ucsb.edu) Harold Frank Hall 3165
Office hours: Monday and Wednesday, 2:00 – 3:00 PM

Lecture
Monday and Wednesday, 12:30 – 1:45 PM, GIRV 2123

Teaching Assistant
William Miller (wmiller@umail.ucsb.edu)

ECE 189A Web Sites
Global Access http://www.ece.ucsb.edu/Faculty/Johnson/ECE189
GauchoSpace https://gauchospace.ucsb.edu

Text
(Required) none

(Reference) Mentor PCB Tools Tutorials —
http://www.ece.ucsb.edu/Faculty/Johnson/ECE189/Mentor2007

Grading
The intention of this class is to provide every student with a complete capstone project design experience. The grading will be based on the overall project results and not on level of effort expended. Grades will be assigned individually and the role played by each student team member and his/her specific contribution must be made apparent. If the final project (or your portion of it) is not finished by end of quarter then the assigned grade will reflect that fact.
Unfinished projects are obviously problematic for your spring quarter ECE 189B course as well.

In both ECE 189A and 189B we will utilize an industrial style, weighted review process in which evaluations by the instructor (50%), the Teaching Assistant (25%) and your teammates/classmates (25%) will determine your grade.

Exam Dates
No exams

Homework
Minimal and not graded. Generally, homework tasks are designed to familiarize you with the Mentor Graphics CAD tools as well as NXP microcontrollers, reference designs and Integrated Development Environment (IDE), etc.

Primary turn-ins are project milestone reports, design reviews and individual weekly reports. Individual weekly reports are mandatory and are critical to a successful project.

Laboratory Use
We will have access to the Computer Engineering Instructional Lab (HFH 4118). We will not formally reserve blocks of time there for this class (outside of our scheduled class time) and we may be sharing space with the groups from the EE capstone class (ECE 188).

Equipment/Parts Checkout

1) Go to the ECE Shop (HFH 1160) to get access cards to the CE Lab and for equipment checkout. Some of the major equipment items (e.g. logic analyzer pods, oscilloscope probes) may require instructor or TA approval so feel free to ask if/when you actually need them.

2) Each group will be assigned a project locker in the CE Lab. Do not try to check out a locker until your group has been officially formed (i.e. after milestone #1). The lockers are located inside the CE Lab. Each is large enough to house all of the parts of your project.

Teams
Project teams should consist of at least 3 and at most 5 members, depending on overall project size and complexity. Optimum group size is probably 3 or 4. Every group must have a defined lead person and very clear subdivisions of responsibility. Make sure that you group with people who complement your skills rather than duplicate them! You will have the same project teams during spring quarter, so you are going to see a lot of each other. Please choose your team members wisely.
Project Selection
Each project must involve the creation of both hardware and software components. The instructor must approve the chosen project before milestone #3 (System Level Design) begins.

You may start with a kit if you like but the kit cannot be the entire project. There are a number of pre-designed kits on the market that could serve as a basis for various projects, particularly in the area of robotics. Use of kits is allowed but your project must go substantially farther than what the kit provides.

Project Cost and Ownership
The cost of making the projects will be borne primarily by the ECE department. In order to maintain control over expenses we will use a "purchasing agent model". All material and fabrication expense items will go through a purchasing agent (the instructor) and wherever possible we will make use of the UCSB Procurement Gateway (more on this later).

The design must be created by each project team. As such, any patentable technology (or other intellectual property) resulting from the project will be owned by the individual student team members. It is strongly suggested that you keep a project notebook which can serve as "proof of discovery" documentation in the event that something patentable emerges from the project.

Project Fabrication
Printed circuit boards will be fabricated by a commercial board house (Sunstone Circuits) and assembled by a commercial assembler (Rapid Prototypes). The number of copies of your project (nominally one per team member) that are made, as well as the disposition of any "extra" copies, will depend on project cost. All fabrication parameters (including the number of copies) must be approved by the instructor. ECE reserves the right to make and keep one or more copies of your design for use in demonstrations, future student recruiting, etc.

ECE 189A — Project Milestones (Fall Quarter 2015)
In order to complete the project in the time available it is necessary to pay careful attention to scheduling.

Below are the course milestones showing the time allotted and the due date for each.

1) **Project Idea and Team Formation** —
   one week (due Monday, October 5) List of team members, conceptual drawing and brief overview "datasheet" of the project with preliminary block diagram.
2) **Refined Project** — one week (due Monday, October 12)
Annotated block diagram, external behavioral specification (prose description of what the project does, not so much about how) with as much detail as possible; identification of the role to be played by each team member.

3) **System Level Design** — two weeks (due Monday, October 26)
Subsystem requirements & specifications, and interface specs.

4) **Detailed Design** — approx four weeks (due Monday, November 23)
Schematic drawings, and (if programmable logic is being used) Verilog or VHDL sources with both functional and timing simulations.

5) **Implementation of the Hardware Design** —
two+ weeks (due Friday, December 11) Artwork for fabricating the printed circuit board (PCB), including Gerber plots, final schematics, engineering drawing, assembly drawing.

**ECE 189A – Design Reviews**
In addition to the milestones and deliverables defined in the previous section, each group will be expected to conduct three design reviews. Each design review represents a significant decision point in the product development cycle and includes a checklist which must be completed before continuing.

**Initial Design Review**
The purpose of the Initial Design Review (IDR) is to define the product development effort and to coordinate the activities and responsibilities of all team members. All team members commit to the goals, tasks and schedules of the product development:

“We will do this product and this is how we will do it”

IDR’s will be conducted after Milestone #2, during the week of October 19.

**Preliminary Design Review**
The Preliminary Design Review (PDR) is all about details and its purpose is to provide proof that the job can be done (or can’t be done). Beyond PDR, there is only execution and the review should instill a sense of confidence that:

“This job can be done...and done by us...”

PDR’s are informal design reviews and will be conducted in my office, actual dates to be determined.
Critical Design Review
At the Critical Design Review (CDR) you demonstrate that the design is complete, correct and ready for fabrication. On completion of CDR, significant financial resources are committed. At CDR you declare and defend that:

“We are done with this design...it will work and this is why...”

CDR’s will be conducted during our scheduled final exam period, Tuesday, December 8 from 12:00 to 3:00 PM.

Winter Quarter 2016

6) **PCB Fabrication & Assembly** — Final review of printed circuit board artwork; generation and submittal of Gerber files to Sunstone Circuits. Final procurement of components for PCB’s, creation of complete assembly kits and submittal to Rapid Prototypes.

All dates are approximations with Friday, March 25 the "drop dead" date for delivery of assembled PCB’s to begin ECE 189B in spring quarter.

- Final review and submittal of Printed Circuit Board artwork - three weeks (due Friday, January 22)
- Printed Circuit Board fabrication - two weeks (bare PCB received Friday, February 5)
- Final Assembly Kit: bagged parts, assembly drawing and Bill of Materials (due Monday, February 8)
- PCB assembly - four weeks (assembled PCB received Friday, March 11)
- PCB worst case completion date to begin Spring quarter - Friday, March 25

ECE 189B Project Milestones (Spring Quarter 2016)

7) **Initial Power-Up** – one week (due Friday, April 1)
   Apply power to board with no shorts, correct regulated voltages, currents within spec, etc.

8) **Processor / Memory / Boot-up** – one week (due Friday, April 8)
   Demonstrate execution of user code via the “Hello World” program, flashing LED’s, etc.
9) **BIOS-Level Monitor** – one week (due Friday, April 15)
   main() with infinite loop; polling / interrupt structure of peripheral control demonstrated

10) **Individual Subsystem Tests** – two weeks (due Friday, April 29)
    Independent software control of all sensors, motors, wireless, displays, etc.

11) **Integration of Subsystems** – two weeks (due Friday, May 13)
    All systems exercised and communicating through common main()

12) **Full Application and Poster Submittal** –
    two weeks (due Friday, May 27) Final integration of “Controls Indicators & Interconnect” and full system operation including any mechanical assembly.

13) **Final Presentation** – Capstone Project Presentation Day
    (tentatively scheduled for Thursday, June 2, 2016)