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Cite as: Appl. Phys. Lett. 114, 172102 (2019); doi: 10.1063/1.5090437
Submitted: 28 January 2019 · Accepted: 18 April 2019 · Published Online: 30 April 2019

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ABSTRACT

We report the development of gallium arsenide (GaAs) films grown on V-groove patterned (001) silicon (Si) by metalorganic chemical vapor deposition. This technique can provide an advanced virtual substrate platform for photonic integrated circuits on Si. A low defect density of 9.1×10^6 cm^-2 was achieved with the aspect ratio trapping capability of the V-grooved Si and dislocation filtering approaches including thermal cycle annealing and dislocation filter layers. The efficiencies of these dislocation reduction methods are quantified by statistical electron channeling contrast imaging characterization. Meanwhile, different sets of dislocation filtering layers are evaluated and optimized. To further demonstrate the suitability of GaAs on the V-grooved Si technique for Si-based photonic devices, especially for the appealing 1.3 μm quantum dot (QD) lasers, a 7-layer indium arsenide QD structure was grown on both GaAs-on-V-grooved Si and native GaAs substrates. The same photoluminescence intensity and full-width at half-maximum values were observed for both structures. The optimization methodology in this work therefore offers a feasible approach to realize high quality III–V materials on Si for large-scale integration.

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There has been significant interest in the monolithic integration of III–V semiconductors on Si due to the potential to combine the complementary metal-oxide-semiconductor (CMOS)-compatible Si photonics platform with III–V light sources.1 Such a capability would offer the design flexibility and scalability required for large-scale photonic integrated circuits (PICs).2 Epitaxial growth of III–V materials on (001) Si is regarded as one of the most promising technologies to fulfill the monolithic integration strategy.3 However, fundamental challenges including threading dislocations (TDs), stacking faults (SFs), and antiphase boundaries (APBs) have hindered the development of high quality III–V on Si.4–6 To address these issues, considerable efforts have been devoted to minimizing the defects. Notable progress has been achieved by growing gallium arsenide (GaAs) on offcut Si with a thin Ge intermediate buffer (200–300 nm).7–9 The thickness of the GaAs layer can be even lowered down to ~1 μm while possessing a smooth surface as well as a low dislocation density due to the small lattice mismatch (0.07%) between GaAs and Ge. Generally, a 2°–6° miscut Si (001) substrate is used to provide biatomic terraces, to avoid the emergence of APBs.10 Other promising techniques to eliminate APBs are based on careful treatments to (001) Si substrates. These include high temperature (HT) annealing in a hydrogen ambient,12 using an optimized thin GaP buffer,13 and nanopatterning of a Si substrate.14–16 Compared with GaAs directly grown on planar Si, the adoption of GaAs on V-grooved Si (GoVS) not only restricts the generation of APBs but also introduces less defects owing to “aspect ratio trapping” and III–V nucleation on Si (111) planes.17

Pioneering work has been conducted to grow GoVS from highly ordered nanowires to coalesced thin films.18 Yet the surface defect density is still on the order of 9×10^7 cm^-2.19 The remarkable extension of the quantum dot (QD) device lifetime on a lower dislocation density GaAs/GaP/Si platform has urgently necessitated a further defect reduction of GaAs buffers.20 Historically, to lower the dislocation density, graded buffer layers, thermal cycle annealing (TCA), and dislocation filter layers (DFLs) have been investigated.21–23 However, progress is still lacking for further lowering the defect density and quantifying the efficiencies of various dislocation filtering approaches on the GoVS virtual substrate.

In this work, we report the systematic development of low defect density GoVS by metalorganic chemical vapor deposition (MOCVD),
Unlike the conventional defect characterization using transmission electron microscopy (TEM),
here the large-area (1813–4538 μm²) electron channeling contrast imaging (ECCI) is adopted as a
reliable technique to quantify the surface dislocation density without any specific sample preparation. We use a channeling condition consisting of both [0 1 0] and [2 2 0] excitations to maximize the detection of 6θ misfit dislocations threading onto the surface.\(^\text{22}\) Benefiting from the optimized dislocation filtering methods including TCA and DFLs, the defect density was lowered to 9.1 × 10^6 cm\(^{-2}\). A multilayer indium arsenide (InAs)-based QD structure was simultaneously grown on GoVS and GaAs substrates, yielding the identical room-temperature photoluminescence (RT-PL) intensities and full-width at half-maximum (FWHM) values.

To start with, the on-axis Si (001) substrate was patterned and dry-etched into [110] aligned nanotrenches with 70 nm opening. The wafer was then immersed in 1% dilute hydrofluoric acid (HF) for 15 s to remove the native oxide. Afterward, the v-grooves were formed by 45% dilute potassium hydroxide (KOH) etching for 30 s, followed by dipping in 16% hydrochloric (HCl) solution for 60 s to clean up the KOH residuals. The oxide stripes were removed, and the as-fabricated V-grooved Si was then subjected to scanning electron microscopy (SEM) characterization, as shown in Fig. 1(a). In addition to the highly ordered V-groove arrays, a further zoomed-in SEM image in Fig. 1(b) reveals some dents formed along the v-grooves, possibly due to the KOH wet etching. This may become an issue by generating extra planar defects. In our growth methodology, we refer to a simple one-step growth approach, indicating that the GaAs layers at various temperatures are completed within a single growth run on the V-grooved Si. By adopting this approach, the negative intrusion of planar defects from the SiO\(_2\)/GaAs interfaces can be effectively avoided.

Specifically, material growth was performed using the Thomas Swan MOCVD at 50 Torr. The V-grooved Si was first annealed at 815 °C for 15 min in an H\(_2\) ambient to desorb the native oxide. The reactor was then cooled down under arsenic overpressure for Si surface passivation. After a thin (12 nm) low-temperature (LT) GaAs wetting layer at 400 °C and a middle-temperature (MT) GaAs layer at 550 °C, the thick high-temperature (HT) GaAs main buffer was grown between 600 and 630 °C. Figure 1(c) presents the cross-sectional SEM image of the 1.6-μm-thick one-step GoVS, suggesting a good coalescence of GaAs. The surface morphology was examined by a 10 × 10 μm² atomic force microscopy (AFM) scan in Fig. 1(d). By adopting the one-step method, most pinholes and pits are eliminated, along with a significant reduction in the surface roughness. The root-mean-square (RMS) value is as low as 1.46 nm, ensuring the subsequent application of dislocation filtering approaches.

Once the smooth GaAs surface has been achieved, TCA and strained layer superlattices (SLSs) were applied. The schematic diagram is shown in Fig. 2(a). To compare the efficiency of different dislocation filtering approaches, we terminated the GaAs buffer growth at various stages (labeled A, B, C, and D) and subjected the samples to the ECCI measurement. The representative images are presented in Fig. 2(b). The basic mechanism for the functioning of TCA was attributed to the dislocation movement and coalescence under thermal stress.\(^\text{40}\) For five cycles of TCA, the sample was annealed at 750 °C for 5 min under arsenic protection. Immediately after that, the substrate was cooled down to 350 °C and held for 5 min. The surface roughness remained the same after the optimum five cycles of TCA (not shown here). It is noteworthy that a higher annealing temperature of 800 °C results in severe surface decomposition. The FWHM of the x-ray diffraction (XRD) rocking curve was reduced by more than 2 times after TCA, as shown in Fig. 3(b). Based on Ayers’ model, the dislocation density determined primarily by the angular rotation of dislocations is given by \(D \approx \beta_d^2/(4.36b^2)\), where \(\beta_d\) is the rocking curve broadening in radians and \(b\) is the length of Burgers vector.\(^\text{35}\) This means that the dislocation density should be decreased by 4.47 times after TCA (from 4.2 × 10^8 to 9.3 × 10^6 cm\(^{-2}\)). Yet, according to the quantitative ECCI scans, the surface defect density is \(\sim 2.4 \times 10^8\) cm\(^{-2}\) after TCA. The large discrepancy between results measured by ECCI and XRD can be explained by the unconsidered strain broadening in the XRD rocking scans, which affects the FWHM during TCA and DFL insertion.

Compared with TCA, a more efficient filtering technique is to insert DFLs. In this work, we studied two categories of DFLs: InGaAs/ GaAs SLSs and InGaAs strained interlayers (SILs). As shown in Figs. 2(c) and 2(d), a remarkable reduction of dislocations is observed after the insertion of the two sets of ten-period 12 nm In\(_{0.16}\)Ga\(_{0.84}\)As/12 nm GaAs SLSs, grown at 495 °C. In-situ annealing at 680 °C for 5 min was
applied after each set of SLSs. The evolution of dislocation density with different GaAs thicknesses and those undergoing various filtering approaches are summarized in Fig. 3(a). Several conclusions can be drawn: First, the dependence of the dislocation density \((\rho_{TD})\) on the GaAs thickness \(d\) (no dislocation filtering method was applied) can be experimentally fitted by a power law: \(\rho_{TD} = 10^{8.93} \cdot d^{-0.963}\). This observation agrees well with the findings via counting \(\rho_{TD}\) by cross-sectional TEM.\(^2\) Second, the introduction of TCA filters out 56% of the defects. Further regrowth of GaAs without any influence of SLSs follows a power law by \(\rho_{TD} = 10^{8.62} \cdot d^{-0.82}\). Moreover, the first set of SLSs is found to be the most efficient in filtering dislocations. This is because \(\rho_{TD}\) becomes lower, the strain field provided by the SLS is not enough to drive the adjacent TDs into coalescence. Here, the efficiencies of two sets of SLSs are 84% and 76%, respectively. Therefore, to achieve the same level of \(\rho_{TD}\) within a thinner buffer, our next step is to apply the TCA and SLSs in an earlier stage. Figure 3(c) shows the optimization of the Indium composition in the In\(_{0.13}\)Ga\(_{0.87}\)As layer. A lower Indium composition (13.5%) is limited in generating enough strain field to interact with the TDs, while a higher one (19.3%) will result in a partial relaxation in the SLSs.

In addition to quantifying the evolution of \(\rho_{TD}\), it is also instructive to directly examine the interaction of dislocations with the filters. Therefore, scanning TEM (STEM) was carried out to analyze dislocation propagation. Figure 4(a) presents the bright-field (BF) STEM image of the complete GoVS template with 7-layer InAs/InGaAs/GaAs QDs grown atop. The STEM lamella was prepared by a focused ion beam (FIB) with a width and a thickness of \(-12 \text{ nm}\) and \(-300 \text{ nm}\), respectively. Images were recorded tilting into a diffraction condition \((g = [002])\) from the [110] zone axis. It is clearly observed that the GaAs buffer above the second set of SLSs is clean without any TDs (the separation of TDs is on the order of 10\(\mu\)m), indicating a defect density less than \(10^7 \text{ cm}^{-2}\). A close-up view of the QD region reveals some misfit dislocations trapped within the QDs [Fig. 4(b)], which may degrade the optical efficiencies. A sharp regrowth interface of GaAs buffer and QDs is noticed in Fig. 4(b). Different from the GaAs on planar Si utilizing thin GaP or MT-Al(Ga)As nucleation,\(^3\)\(^4\)\(^2\)\(^7\) the advantage of the V-grooved (111) Si planes acquired here is that the 4% lattice mismatch between GaAs/Si can be accommodated into a thin layer of SFs (\(-12 \text{ nm}\)).\(^1\)\(^7\) Most of the SFs are absorbed by the LT-GaAs nucleation and coalesced into self-annihilation, as shown in Fig. 4(c). However, some dislocations are noted to thread out of the top GaAs/Si (001) interfaces formed by Si undercut. The effect of SLSs is demonstrated in the zoomed-in STEM image in Fig. 4(d). In addition to the sharp interfaces of the SLSs, apparent TD bending and termination at the InGaAs/GaAs hetero-interfaces are observed, implied by the yellow arrows. An array of in-plane misfit dislocations is generated at both sides of the SLSs and strongly confined by the strain field of SLSs. Meanwhile, localized fluctuation of stacked InGaAs/GaAs is also identified, probably due to the interface distortion by the accumulated strain fields.

For the InGaAs SILs, two sets of 200 nm In\(_{0.08}\)Ga\(_{0.92}\)As layers are embedded in the GoVS buffer in Fig. 5(a). No obvious relaxation of the InGaAs layer was detected in Fig. 5(c). Sharp lines are noticed on top of each InGaAs interlayer, due to the \textit{in-situ} annealing at an elevated temperature of 680 °C. One interesting observation presented in Fig. 5(b) is that some SFs, they are stopped at an interface where TCA was applied. This may indicate that by creating an extra interface (TCA and regrowth), the SFs can be stopped. The surface defect density is characterized at \((1.56 \pm 0.4) \times 10^7 \text{ cm}^{-2}\). One representative ECCI image is shown in Fig. 5(d), with some TDs indicated by yellow arrows. Considering the comparable overall strain offered by SLSs and SILs, the filtering results are not prevailing for InGaAs SILs, possibly due to the lack of multiple InGaAs/GaAs interfaces for dislocations to bend laterally.

To assess the suitability of the well-developed GoVS template for 1.3 \(\mu\)m QD lasers, a 7-layer InAs/InGaAs/GaAs dot-in-well (DWELL) structure was grown on GoVS and GaAs substrates simultaneously. A layer of uncapped InAs QDs was grown on top of the 7-stack QDs for the AFM measurement. The growth scheme is illustrated in Fig. 6(a).

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**FIG. 2.** (a) Schematic diagram of the complete GoVS structure. (b) Representative ECCI images at different growth stages, labeled as “A, B, C, and D.”
The growth details can be found elsewhere. The surface morphology of the 8th QDs is shown in Fig. 6(b), without any obvious formation of large defective clusters. The elimination of clusters clearly demonstrates an effective stacking of QDs to achieve an enhanced material gain. The QD density is extracted to be \( \frac{5 \times 10^{10} \text{ cm}^{-2}}{2} \). Figure 6(c) displays the zoomed-in BF STEM image of the stacked QDs grown on GoVS. The buried QDs can be distinguished, with some dislocation loops surrounding these dots. These surrounding defects are also observed for the QDs on the GaAs substrate with a lower density. A higher resolution STEM image of a representative single QD is shown in Fig. 6(d). The typical dot size is \( \sim 22 \text{ nm} \) in diameter and \( \sim 7 \text{ nm} \) in height.

Power-dependent RT-PL was performed to evaluate the optical properties of QDs grown on GaAs and GoVS. The pumping laser is a 780 nm continuous-wave semiconductor laser, and the excitation power densities reaching onto the sample surface are calibrated at 8.6 W/cm\(^2\) and 60 W/cm\(^2\), respectively. In the low excitation regime,
the RT-PL spectra in Fig. 6(c) reveal the same peak intensity and the same FWHM value (44 meV) of the ground state (GS). These results are attributed to the low defect density of the GoVS buffer, as well as the less sensitivity of QDs to defects.\textsuperscript{11,12} Furthermore, a slight overlap between GS and the first excited state (ES) is observed, due to the QD inhomogeneous broadening, and different carrier fill-levels induced by the InGaAs cap layer. It has also been observed in some molecular beam epitaxy (MBE) and MOCVD grown QDs.\textsuperscript{30,31} The intensity ratio and energy separation between GS and ES can be tailored by varying the QD growth temperature and Indium composition of the InGaAs cap layer. It has also been observed in some molecular beam epitaxy (MBE) and MOCVD grown QDs.\textsuperscript{30,31}

The efficiencies of different dislocation filtering approaches are evaluated while the ES becomes more distinct under higher excitation powers, the ES becomes more distinct.\textsuperscript{21} The high PL efficiencies of QDs grown on GaAs reveal the same peak intensity and the same PL intensities of the QDs grown on GoVS and well-developed GoVS in two pump power regimes, demonstrating the same optical performance with the QDs grown on GaAs. These results offer a pathway to monolithically integrate large-scale III–V semiconductors on the CMOS-standard Si substrate for integrated photonics.

The authors acknowledge financial support from the Defense Advanced Research Projects Agency (DARPA) through the Young Faculty Award (YFA). The authors acknowledge SUNY Polytechnic Institute for providing patterned silicon substrates. The research reported here made use of shared facilities of the UCSB MRSEC (No. NSF DMR 1720256).

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