Defect engineering for InP epitaxially grown on (001) Si by MOCVD

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Abstract: We demonstrated a defect reduction from 5.6×10^8 to 7.9×10^7 cm^{-2} for InP monolithically grown on a V-groove patterned (001) Si substrates, by optimizing the $In_xGa_{1-x}As$/InP strained layer superlattices (SLSs). The effects of SLSs are further evaluated by large-area statistical electron channeling contrast imaging (ECCI), scanning transmission electron microscopy (STEM) and room-temperature photoluminescence (RT-PL).

1. Introduction

Monolithic integration of indium phosphide (InP) and its related lattice matched alloys on Si substrates have been extensively investigated in the past decades [1,2]. Recently, defect engineering for InP grown on Si has regained considerable interests, motivated by the demonstrations of efficient InAs quantum dot lasers in both datacom and telecom wavelengths [3,4]. However, compared to the device-applicable GaAs/Si system with a dislocation density below 10^6 cm^{-2}, the development of InP on microelectronic-standard (001) Si substrates is lagging and demanding more efforts. The challenges in this heteroepitaxy mainly exist in a high threading dislocation density (TDD) due to a larger lattice mismatch (8%) than the GaAs/Si, as well as anti-phase boundaries (APBs) formation during the polar/non-polar growth.

To address the APB issue, one robust methodology applied in this work is to grow III-V materials on the V-groove patterned Si substrates [5,6]. A single step on the formed Si (111) surface possesses the height of a bi-atomic layer (0.31 nm). On the other hand, except the graded buffer approach [7], here we grew a GaAs intermediate buffer to well accommodate the lattice mismatch between InP and Si. The high density of TDs generated at the InP/GaAs heterointerface can be partially filtered by the $In_xGa_{1-x}As$/InP SLS during TD propagation [8]. In this work, we focused on the improvement of dislocation filtering efficiency by optimizing the growth conditions of the SLSs. It is uncovered that high density of hillocks emerge for SLSs grown at low temperatures due to Indium clustering. By increasing the SLS growth temperature, a cluster-free InP surface can be obtained, with a smooth morphology. Furthermore, a 7-fold reduction in defect density was achieved by introducing $In_{0.82}Ga_{0.18}As$/InP SLSs, as characterized by large-area ECCI. The interaction of dislocations with SLSs were analyzed based on the cross-sectional STEM images.

2. Experiments and results

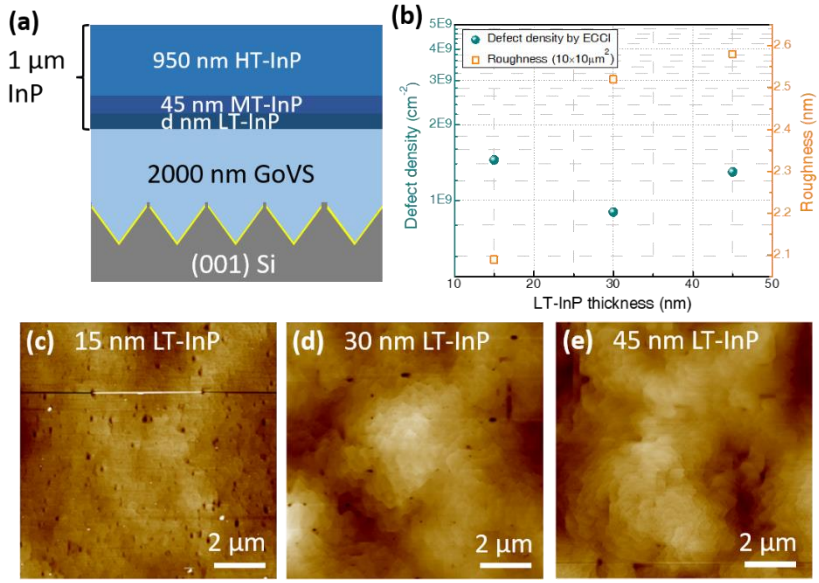

Fig. 1. (a) Schematic of 1 μm InP grown on the GoVS substrate. (b) Defect density and surface roughness as a function of LT-InP thickness. (c)-(e) AFM images of 1 μm InP with various LT-InP thicknesses.

The material growth was performed using the Thomas Swan MOCVD system at 350 Torr. Prior to growth, a 12-inch 2-μm-thick GaAs-on-V-grooved Si (GoVS) wafer was diced into small pieces for the sequential InP growth development. Details about the GoVS template adopted in the growth can be found in Ref. [9]. The InP was grown using a "three-step" method, as indicated in Fig. 1(a). It comprises of a thin low-temperature (LT) InP at 430-450°C, a middle-temperature (MT) InP at 540°C, and a thick high-temperature (HT) InP buffer at 600-630°C. The critical parameter in the "three-step" growth is the thickness of the LT-InP nucleation, which significantly affect the surface morphology and defect density of the overall InP buffer. Figures 1(c)-(e) compare the surface morphology of 1 μm InP buffer with varied LT-InP thicknesses. It is noted that a thicker LT-InP helps eliminate the pinholes on the surface, owing to a better InP coverage on the GaAs intermediate buffer. However, as shown in Fig. 1(b), the defect density is higher in this situation, possibly due to more TDs and stacking faults (SFs) generation within the LT-InP layer. In our optimized structure, a LT-InP thickness of 30 nm is chosen to minimize the defects below SLSs.

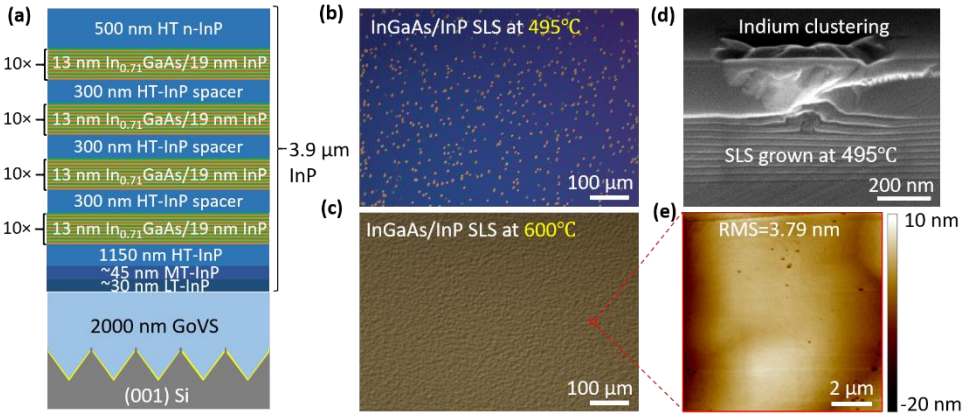

Fig. 2. (a) Schematic of 3.9 μm InP grown on GoVS, inserted with four sets of InGaAs/InP SLSs. (b) Optical microscope images of the InP surface with SLSs grown at 495°C and (c) 600°C, respectively. (d) Cross-sectional SEM image of the LT-SLS, showing the Indium clustering. (e) 10×10 μm^2 AFM scan of the InP surface with HT-SLS.

Figure 2(a) illustrates the 3.9 μm InP buffer inserted with four sets of 10-period $In_{0.71}Ga_{0.29}As$/InP SLS. For the SLS grown at 495°C, dense hillocks appear on the final InP surface, as shown in the optical microscope image (Fig. 2(b)). The cross-sectional scanning electron microscope (SEM) image in Fig. 2(d) reveals an Indium clustering phenomenon during the LT-SLS growth. Yet, for the SLS grown at higher temperatures (600°C or even above), the surface is free of hillocks, exhibiting a smooth surface. The root-mean-square (RMS) value is 3.79 nm for a 10×10 μm^2 atomic force microscopy (AFM) scan. Therefore, the formation of Indium clusters during LT-SLS growth can be ascribed to the InGaAs phase separation in the LT growth. Strain accumulation occurs severely in the Indium-rich region, resulting in an Indium out-diffusion and clustering during the stacked SLS growth.

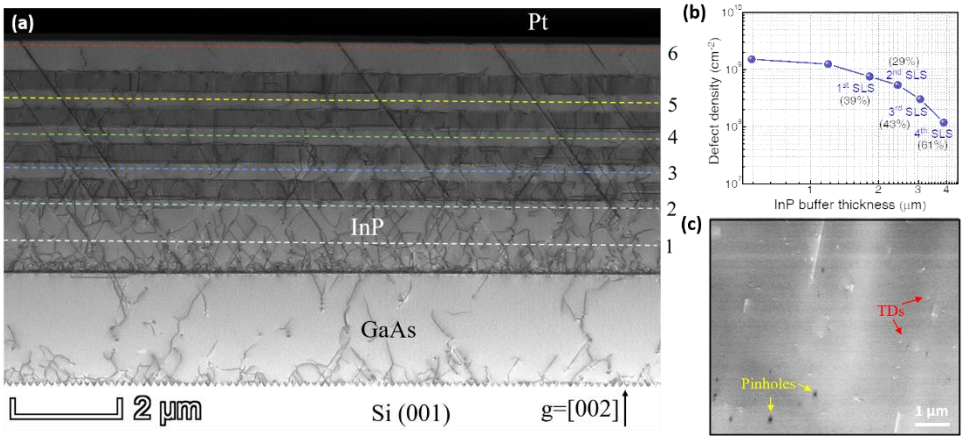

Fig. 3. (a) Cross-sectional STEM image of the 3.9 μm InP on GoVS. (b) Dependence of extracted dislocation density on the InP buffer thickness. (c) Typical ECCI image of the InP buffer with a defect density of 1.15×10^8 cm^{-2}.

To justify the effectiveness of the embedded SLSs, both STEM and ECCI were carried out for qualitative and quantitative analysis. The TEM lamella was prepared by focused ion beam (FIB), with a width of 12 μm and a thickness of 500 nm. The zone axis is [110] and the diffraction vectors are chosen at on-axis and g=[002], respectively. Figure 3(a) presents a global view across the lamella, suggesting a much cleaner top InP layer above the final set of SLS. Some SFs generated from the InP/GaAs interface are noted to penetrate through the SLSs and terminate at the InP surface. The evolution of defects after each set of SLS is summarized in Fig. 3(b). Generally, the filtering efficiency becomes higher as the SLS set number increases (shown inside the brackets in Fig. 3(b)). After the four sets of SLS, the calculated defect density reached 1.17×10^{8} cm^{-2}, based on the STEM characterization. Interestingly, the large-area ECCI measurement reveals a surface defect density of 1.15×10^{8} cm^{-2}, correlating well with the STEM results. One typical ECCI image is shown in Fig. 3(c), where SFs, TDs and pinholes can be easily distinguished.

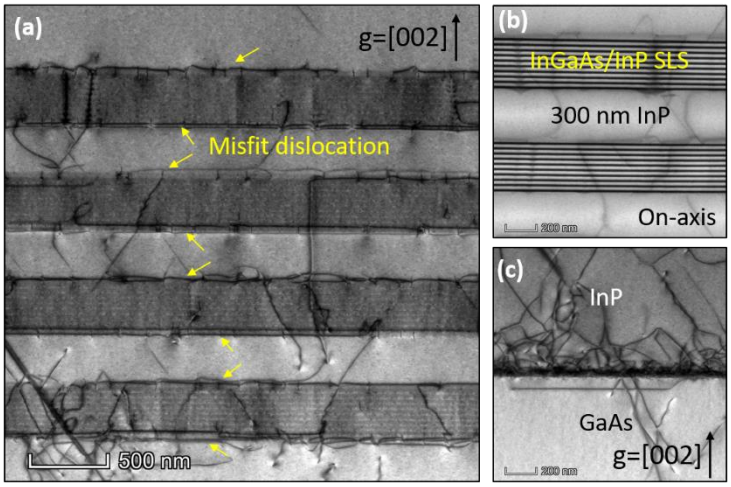

Fig. 4. (a) Zoomed-in STEM image of the four sets of $In_{0.71}Ga_{0.29}As$/InP SLSs. (b) Higher resolution STEM image showing the sharp InGaAs/InP interfaces. (c) Close-up STEM of the InP/GaAs interface.

A zoomed-in STEM image helps with understanding the dislocation filtering mechanisms. Besides the lateral motion of dislocations driven by the strain field of SLSs, it is noted in Fig. 4(a) that an array of misfit dislocations is pinned at both top and bottom interfaces of the SLSs. The emergence of these misfit dislocations indicates the sufficient strain field to terminate the TDs [10]. Similar phenomenon is also observed at the InP/GaAs interface (Fig. 4(c)). The moire fringe is formed due to the network of misfit dislocations. However, these misfit dislocations will thread out to form movable TDs when far exceeding the critical thickness. Figure 4(b) shows the sharp and atomically smooth interfaces between InGaAs/InP.

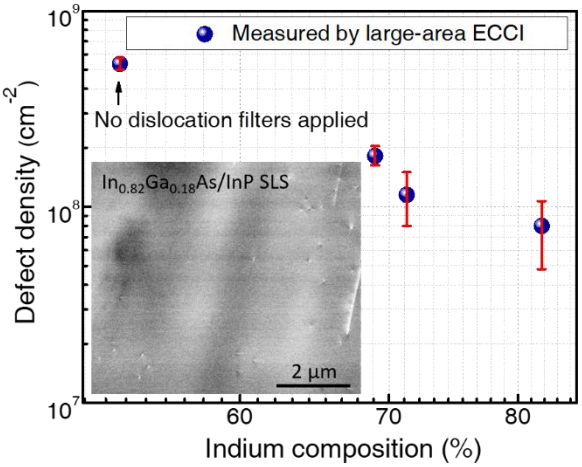

Fig. 5. Dependence of defect density on the Indium composition of the $In_xGa_{1-x}As$ layer. The inset shows a representative ECCI image of InP buffer inserted with $In_{0.82}Ga_{0.18}As$/InP SLSs.

In order to investigate the influence of strain field on the dislocation filtering efficiency, the Indium composition of the InGaAs layer is varied to offer with different strain fields. Meanwhile, the same thickness of InP buffer without the insertion of SLS is grown as a reference, showing a defect density of 5.36×10^{8} cm^{-2}. As demonstrated in Fig. 5, a higher Indium composition (82%, misfit=1.9%) leads to a significant defect reduction to ~7.9×10^{7} cm^{-2}. It is anticipated that further increasing the Indium composition will inversely introduce more TDs with partial relaxation of the SLS. A representative ECCI image of the InP buffer inserted with $In_{0.82}Ga_{0.18}As$/InP SLS is shown in the inset of Fig. 5.

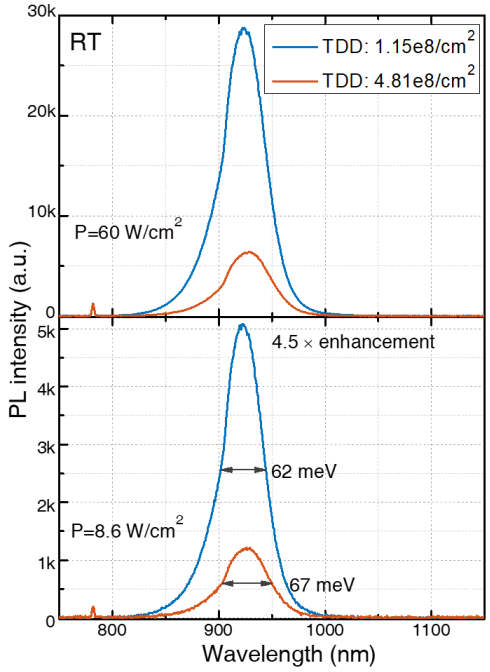

Fig. 6. Power-dependent RT-PL spectra of two InP-on-GoVS samples equipped with different defect densities.

Power-dependent RT-PL is performed on two InP-on-Si samples with different surface defect densities to assess their optical properties. The surface defect densities are 1.15×10^{8} cm^{-2} and 4.81×10^{8} cm^{-2}, respectively. At both excitation regimes, the peak PL intensity is ~4.5 times stronger and the full-width at half-maximum (FWHM) value is slightly lower for the less defective InP buffer (shown in blue curves). This result suggests using a room-temperature photoluminescence as an effective tool to distinguish the crystalline quality of InP grown on Si substrates. Our future work is to grow 1.55 μm quantum well or quantum dot structures on top of these templates to figure out the influence of dislocations on the optical performance of the active layers.

3. Conclusions

In summary, a detailed study on the role of strained-layer superlattice on dislocation filtering is presented. By optimizing the thickness of LT-InP, the growth temperature and Indium composition of the InGaAs SLS, the InP surface defect density has been as low as 7.9×10^{7} cm^{-2}, together with a smooth surface front. To further lower down the defect density, our next step is to replace the InGaAs/InP SLS with the strain-compensated $In_xGa_{1-x}As/In_yGa_{1-y}As$ superlattices to intensify the lateral movement of the TDs.

4. Acknowledgements

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5. References

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