Toward All MOCVD Grown InAs/GaAs Quantum Dot Laser on CMOS-compatible (001) Silicon

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Abstract: Indium arsenide quantum dots (QDs) are demonstrated on gallium arsenide on silicon templates by metalorganic chemical vapor deposition. The template threading dislocation density is only 9.5×10^{6} cm^{-2} and the QDs are of high quality. © 2019 The Author(s)
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1. Introduction

Direct heteroepitaxy of III-V quantum dots (QDs) is promising for achieving a monolithic laser source for silicon photonics [1,2]. QDs are believed to be less sensitive to defects than quantum wells, and also offer desirable characteristics for high-temperature operation and reduced sensitivity to reflection. Recently reported indium arsenide (InAs) QD lasers on silicon have been based primarily on molecular beam epitaxy (MBE), but many of those demonstrations utilized off-axis silicon substrates or templates firstly grown by metalorganic chemical vapor deposition (MOCVD). It is desirable to grow entire QD lasers, including the underlying template, with a single growth technique, and MOCVD is preferable since it is the industry standard for large-volume production; MOCVD offers high throughput enabled by larger multi-wafer reactors and higher growth rates. MOCVD also allows for selective area growth, nonplanar growth, and regrowth over gratings (for single-frequency lasers).

Critical to the realization of a QD laser on silicon are template material demonstrating low threading dislocation density (TDD) and low roughness, and QDs with optimal size, density and uniformity. Templates have been demonstrated on (001) silicon utilizing gallium arsenide (GaAs) grown on v-groove-patterned silicon (so called GoVS) [3], and indium phosphide (InP) on patterned silicon or silicon on insulator [4-6]. In this work, state-of-the-art GoVS templates were demonstrated along with high quality InAs/GaAs QDs, all by MOCVD. The GoVS template yielded a TDD of 9.5×10^{6} cm^{-2} and surface roughness of 1.75 nm. The QDs grown on these templates yielded optimal size (average diameter of 22 nm), optimal density (approximately 5×10^{10} cm^{-2}), high uniformity, and a photoluminescence (PL) intensity nearly identical to that for the same QD structure grown on a native GaAs substrate. These results are extremely promising for the eventual realization of an all MOCVD grown monolithic InAs/GaAs QD laser on (001) silicon.

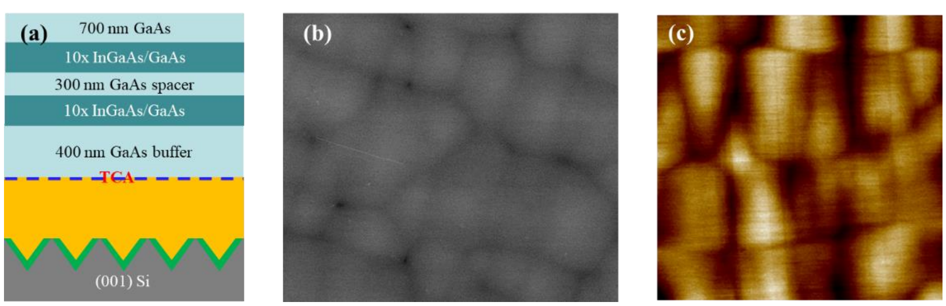

Fig. 1. (a) Layer structure for GaAs template on silicon. (b) Representative ECCI image for TDD characterization. (b) AFM image demonstrating 1.75 nm roughness (area = 10×10 μm^2).

2. GaAs on Silicon Template Development

Standard (001) silicon substrates were patterned with a uniform array of 65 nm trenches on a 130 nm pitch. The nanopatterned silicon was subsequently etched with potassium hydroxide (KOH) to form the silicon v-grooves, which effectively avoids the generation of anti-phase domains (APDs) during subsequent III-V growth. For the MOCVD growth of the GaAs buffer, a 10-nm-thick low temperature GaAs nucleation layer was first grown at 400°C, followed by a 40 nm GaAs layer at a temperature of 550°C, and finally a 1.3-μm-thick high temperature (600°C) GaAs layer to achieve a coalesced flat surface. The template was then subjected to thermal cycle annealing (TCA). Two periods of a 10-layer indium gallium arsenide (InGaAs)/GaAs strained layer superlattice (SLS) were then grown to further reduce the TDD. The entire layer stack is shown in Fig. 1(a). A large area (over 3000 μm^2) electron channeling contrast imaging (ECCI) measurement was performed and the image is shown in Fig. 1(b). The TDD was measured to be 9.5×10^6 cm^{-2}, which is considerable low. Meanwhile, as shown in Fig. 1(c), the surface roughness was as low as 1.75 nm based on the 10×10 μm^2 atomic force microscopy (AFM) scan.

3. InAs/GaAs QD Development and Results

A QD calibration growth on a GaAs template (or native GaAs substrate) begins with a GaAs buffer layer grown at 630°C. The temperature is then reduced to 495°C to grow a 2-nm-thick InGaAs pre-layer and 3-monolayer (ML) thick InAs layer. After InAs deposition, a growth interruption of 60 s is introduced to facilitate QD formation. Then the QDs are covered by a 5-nm-thick InGaAs layer followed by 2-nm-thick GaAs layer. After that, the temperature is increased to 580°C and held for 60 s for annealing. Afterwards, a 50-nm-thick GaAs spacer layer is grown at the same temperature. The temperature is then reduced again to 495°C to grow another period of QDs. After all periods of QDs with capping layers, a 2-nm-thcik InGaAs pre-layer and an uncapped QD layer are grown, which is used for AFM characterization. The underlying (capped) QD layers are used for PL characterization. The full layer structure with seven periods of capped QDs is shown in Fig. 2(a). These structures were grown both on native GaAs and on the GoVS template described in Section 2. AFM measurements with a scan area of 1×1 μm^2 were performed to characterize the surface morphology of the QDs on both substrates. As shown in Fig. 2(b) and (c), the QDs on native GaAs and on GoVS appear identical, and both with excellent uniformity. The dot density is approximately 5×10^{10} cm^{-2} and the average dot diameter is 22 nm. As shown in Fig. 2(d), the PL intensity is nearly identical for the QDs grown on GaAs and on GoVS. The QDs on GoVS have a slight redshift with respect to QDs on GaAs; this could be related to the additional strain induced by the underlying silicon. The high quality QDs demonstrated bode well for future all MOCVD QD lasers on complementary metal-oxide-semiconductor (CMOS)-compatible (001) silicon.

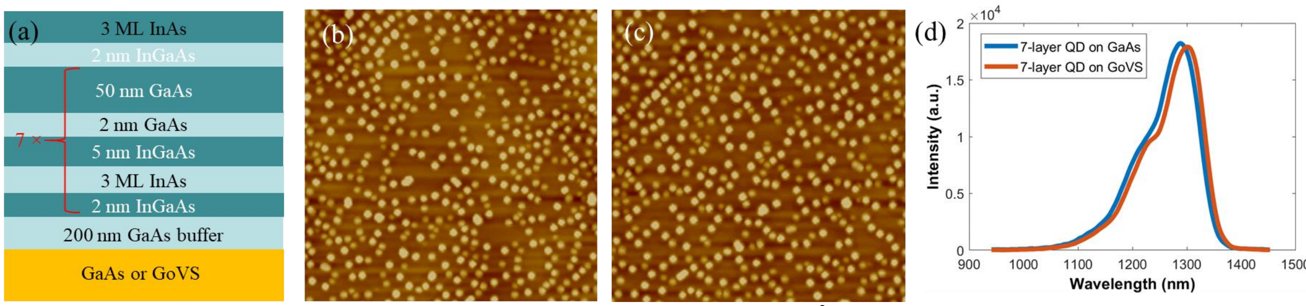

Fig. 2. (a) QD calibration growth with 7-layer QDs. AFM scan with 1×1 μm^2 area for QDs on (b) GaAs and on (c) GoVS. (d) PL spectra for seven-layer QD structures on GaAs and GoVS.

4. Conclusions

Low defect density GoVS templates and high quality QDs have been developed by MOCVD. The QDs show excellent morphology and nearly identical performance on both GaAs and GoVS, which indicates great potential for all MOCVD growth of InAs/GaAs QD lasers on (001) silicon.

5. Acknowledgements

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6. References

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