Selective area heteroepitaxy of antiphase boundary free GaAs microridges on on-axis (001) Si for silicon photonics

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Abstract: Low defect density gallium arsenide microridges were selectively grown on patterned (001) silicon. Antiphase boundaries were eliminated by bending and self-annihilation, enabled by low temperature nucleation and subsequent growth temperature optimization. © 2021 The Author(s)
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1. Introduction

Selective area heteroepitaxy (SAH) of III-V semiconductors on standard on-axis (001) silicon (Si) substrates is attractive for large-scale monolithic integration of high performance active components in silicon photonics. Respectable demonstrations have been reported by growing III-V crystals on intentionally miscut Si wafers or by growing III-V nanowires/nanoridges on patterned Si substrates [1,2]. For the former, a large miscut angle not only affects the performance of complementary metal-oxide-semiconductor (CMOS) devices, but also adds cost and complexity by requiring specific Si wafers. The III-V nanoridge approach presents several challenges including insufficient optical gain, high optical loss, and high contact resistance owing to the complexity of device fabrication.

Previously we reported the SAH of indium phosphide (InP) microridges on CMOS-compatible Si without antiphase boundaries (APBs); elimination of APBs is considered the most critical challenge for III-V/ Si heteroepitaxy [3]. The APB elimination was enabled by etching the Si micro-trenches into trapezoids or v-grooves to generate {111} Si planes. In this work, we present the realization of APB-free GaAs microridges by SAH on flat-bottom Si (001) trenches. The avoidance of APBs is primarily attributed to the low temperature GaAs nucleation and subsequent optimized growth temperatures. Additionally, by introducing $In_xGa_{1-x}As$/GaAs strained layer superlattices (SLSs) as dislocation filters [4], a low surface defect density of 8.5×10^6 cm^{-2} was achieved. The ability to grow APB-free GaAs selectively on Si from a flat Si surface is critical for process integration and will also enable novel device structures.

2. Material growth and characterization

For microridge SAH, 2-inch Si (001) wafers were first thermally oxidized to form 5 µm of silicon dioxide (SiO_2). Conventional lithography and dry etching were then utilized to form flat-bottom Si trenches. Figure 1(a) depicts the

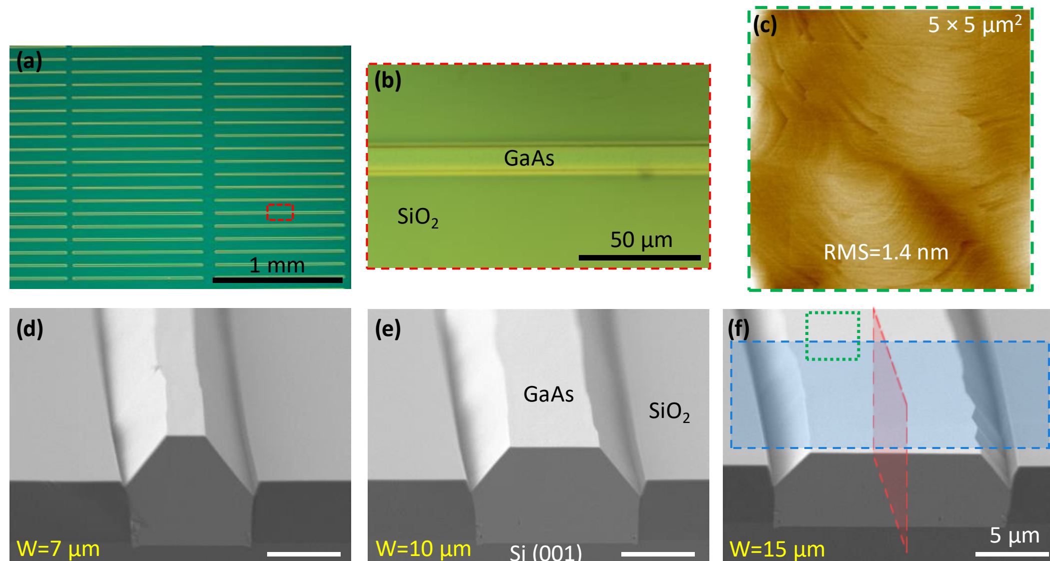

Fig. 1. (a) Optical microscope image of GaAs microridges following SAH and (b) close-up image of a single GaAs microridge revealing the APB-free surface. (c) 5×5 µm^2 AFM image of the surface of a 15-µm-wide GaAs microridge. (d)-(f) Tilted SEM images of as-grown GaAs microridges inside the flat-bottom Si trenches, with the trench opening widths of 7 µm, 10 µm, and 15 µm, respectively.

patterning of the SiO_2 and the excellent selectivity achieved for GaAs growth. The width and length of the Si trenches varied from 7-15 µm and 250-1500 µm, respectively. The pitch was fixed at 100 µm. Following surface cleaning, the patterned Si wafer was subjected to dilute HF treatment to remove the native oxide. Immediately thereafter, the sample was loaded into the metalorganic chemical vapor deposition (MOCVD) system for GaAs growth. The growth began with 815°C annealing under arsenic overpressure for thermal cleaning and surface passivation. The temperature was then reduced to 355°C for GaAs nucleation growth. A low pressure of 35 Torr and a high V/III ratio were used to ensure good selectivity for the kinetic-limited growth and effective GaAs nucleation, respectively. Subsequently, the growth temperature was elevated in stages to 530°C, 580°C and 640°C, to bend and annihilate the APBs. It is importatnt to note that the SAH growth rate is approximately 5-6 times higher than that for planar growth. During the SAH process, the GaAs growth rate gradually decreases as the GaAs microridge grows. The zoomed-in differential interference contrast (DIC) optical microscope image in Fig. 1(b) shows the APB-free surface and smooth surface morphology, as further evidenced by the atomic force microscopy (AFM) image and tilted scanning electron microscope (SEM) images in Figs. 1(c)-(f). The surface roughness was as low as 1.4 nm, with step flows clearly visible. As expected, a higher growth rate was observed for narrower ridges. The corrugations on the edges of GaAs (111) surfaces were caused by micro-trenching and roughness originating from the SiO_2 sidewalls.

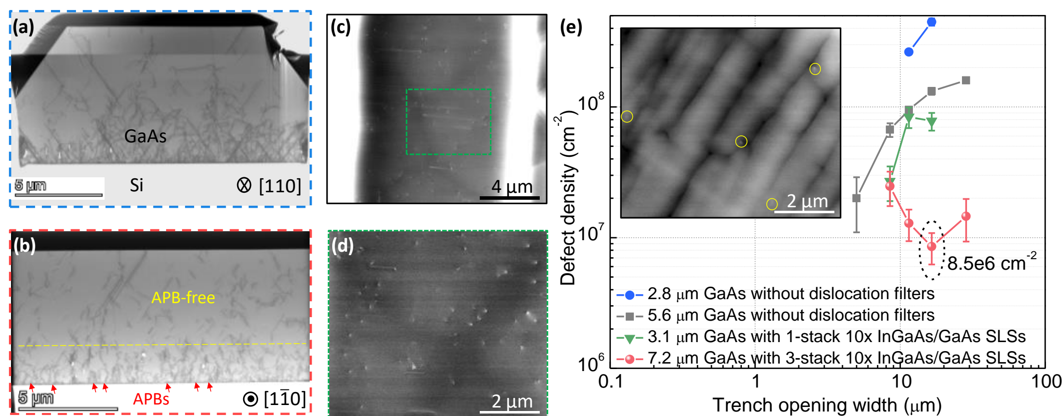

Fig. 2. Cross-sectional STEM images of a 15-µm-wide GaAs ridge (a) parallel and (b) perpendicular to the microridge directions. (c) ECCI measurement of the GaAs ridge and (d) the zoomed-in image. (e) Dependence of the surface defect density on the trench width for different thicknesses of the GaAs buffer. Inset shows one ECCI image of the GaAs surface with the lowest defect density of 8.5×10^6 cm^{-2}.

To study the APB elimination and to quantify the surface defect density, cross-sectional scanning transmission electron microscopy (STEM) and electron channeling contrast imaging (ECCI) were applied, as illustrated in Fig. 2. The formation of {111} GaAs in Fig. 2(a) was due to the faster growth rate along the [001] direction. A high density of APBs was identified near the nucleation interface in Fig. 2(b) (parallel to ridges) as indicated by red arrows. These APBs were annihilated during the higher temperature growth and completely APB-free GaAs was achieved for a GaAs buffer greater than 1.7 µm thick (yellow dashed line). Figure 2(c) shows the ECCI image for a 15-µm-wide GaAs ridge whereby surface defects were clearly imaged as bright spots in Fig. 2(d). Figure 2(e) summarizes the defect density as a function of the Si trench width and the effect of SLS dislocation filters. The lowest defect density achieved was 8.5×10^6 cm^{-2} for the thicker GaAs buffer. The exemplary ECCI image is shown in the inset. No cracks were formed owing to the strain alleviation afforded by SAH. A significantly thinner buffer with similar defect density can be expected by optimizing the dislocation filters further.

3. Conclusion

GaAs microridges with a dislocation density as low as 8.5×10^6 cm^{-2} were selectively grown on flat-bottom Si (001) trenches. The APBs generated at the GaAs/Si hetero-interface were confined and annihilated by the combination of a low-temperature GaAs nucleation and subsequent stepped growth at elevated temperatures. These high quality GaAs microridges can enable a truly monolithic gain in the silicon photonics and other scalable photonic and electronic devices on CMOS-compatible Si substrates.

4. References

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