Heteroepitaxy of III-V materials and photonic devices on silicon

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***Abstract*—We present our recent results on monolithic integration of III-V materials and photonic devices (lasers and photodetectors) on on-axis (001) silicon substrates, by both blanket heteroepitaxy and selective area heteroepitaxy.**

Keywords—Blanket heteroepitaxy, selective area heteroepitaxy, lasers, detectors, integrated silicon photonics

I. INTRODUCTION

The efforts on integration of III-V based materials and devices on silicon (Si) have surged recently to overcome the limitations in Moore's law and to address the exponential data traffic growth. Monolithic integration relying on direct heteroepitaxy is advantageous for high density, low cost, and large scale co-integration of high performance electronic and photonic devices. In this paper, we briefly summarize our advances in integrating lasers and photodetectors on complementary metal-oxide-semiconductor (CMOS) compatible Si substrates through blanket heteroepitaxy. Results on selective area heteroepitaxy (SAH) of high quality III-V microridges on Si is discussed as a perspective toward photonic integrated circuits (PICs) with higher integration density and chip complexity.

II. BLANKET HETEROEPITAXY OF LASERS AND PHOTODETECTORS ON SI

1550 nm indium gallium arsenic phosphide (InGaAsP) based quantum well (QW) lasers and bulk InGaAs PIN photodetectors were realized on (001) Si, by blanket heteroepitaxy. Fig. 1 demonstrates the laser structure and key device performances, including light output-current-voltage (LIV) curves at room temperature and elevated temperatures, as well as small-signal frequency responses. The lasers on Si exhibit a threshold current density of 2 kA/cm^2, together with an output power of 20 mW per facet [1]. The inferior device metrics on Si compared to those on InP substrate were attributed to the dislocations in the InP buffer on Si (dislocation density of 1.1×10^8 cm^{-2}) [2]. The 3-dB bandwidth is measured to be 5.3 GHz, lower than the value on InP (9 GHz) [3]. Moreover, the lasers were aged under both 10°C continuous-wave (CW) and 60°C pulsed current injections. Stable operation over 200 hours (hrs) was achieved at 10°C without any degradation in threshold, output power and slop efficiency. However, a rapid failure was noticed at higher temperatures, suggesting that compared to the recombination enhanced defect reactions under high current injection, the thermal effect is more detrimental to device reliability [3].

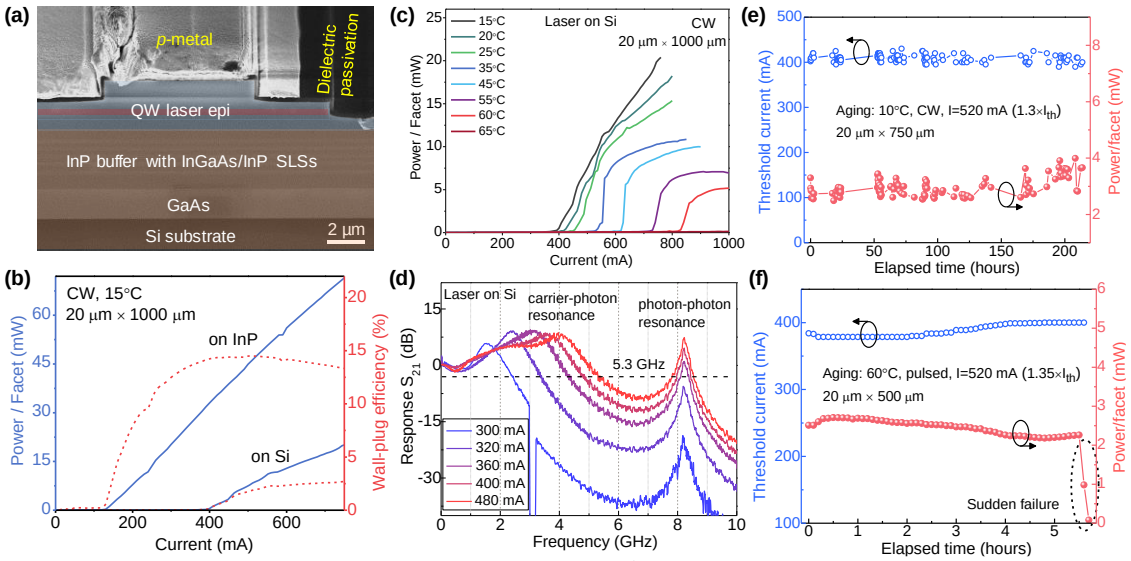

Fig. 1. (a) Cross-sectional scanning electron microscope (SEM) image of the Fabry-Perot (FP) laser. (b) LIV curves and wall-plug efficiencies of 20 μm×1000 μm lasers on InP and on Si. (c) Temperature-dependent LI characteristics and (d) frequency responses for the laser on Si. (e) Aging test of the lasers on Si under 10°C CW and (f) 60°C pulsed current injections.

Fig. 2 presents the layout and characterizations of bulk InGaAs PIN photodetectors grown on the InP-on-Si template, with a surface defect density of 2×10^8 cm^{-2} [4]. In addition to fabricating standalone photodetectors, the 8×8 PIN detector arrays were manufactured. The corresponding dark currents and responsivities were benchmarked with those grown on native InP substrates. The average dark current for 30-μm-diameter pixels on Si under 1 V reverse bias is 5.7 nA (dark current density of 0.45 mA/cm^2), only slightly higher than the value on InP (3.4 nA). Besides, the responsivity at 1550 nm is generally higher for the pixels on Si (0.64 A/W) due the reflection enhancement at interface between Si and III-V materials.

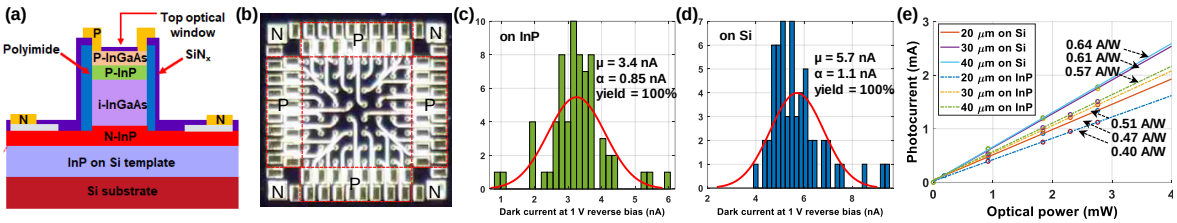

Fig. 2. (a) Cross-section schematic of the photodetector structure on Si. (b) Top view image of fabricated 8×8 InGaAs PIN detector array on Si. The pixel diameter is 30 μm. Histogram plot of measured dark currents for PIN detector arrays (c) on InP and (d) on Si, with pixel diameter of 30 μm. (e) Responsivity of pixels at 1550 nm under 1 V reverse bias for devices with various diameters.

III. Selective Area Heteroepitaxy of Antiphase Boundary Free III-V Microridges on Si

It is foreseeable that compared to planar heteroepitaxy, SAH of III-V microridges on patterned Si or silicon-on-insulator (SOI) is preferred for process integration and for achieving higher quality material, which directly improves device reliability. III-V microridges provide a promising path toward monolithic gain on Si by SAH. The most significant challenge for this approach is to eliminate anti-phase boundaries (APBs) generated during polar-on-non-polar growth on (001) Si [5]. These APBs originate from the III-V/Si hetero-interface and extend to the top surface. Fig. 3 reports our recent work on SAH of APB-free gallium arsenide (GaAs) microridges on flat-bottom Si (001) inside recesses [6]. By carefully optimizing the low-temperature (LT) GaAs nucleation layer growth, the generation of APBs can be minimized. Furthermore, a subsequent high temperature (HT) growth promotes the kink and self-annihilation of APBs, preventing their upward propagation. Both SEM and atomic force microscopy (AFM) characterizations reveal no appearance of APBs and the surface roughness is as low as 1.4 nm in Fig. 3(c). Moreover, the conventional dislocation filtering approaches including thermal cycle annealing (TCA) and strained layer superlattices (SLSs) were introduced and proven effective for SAH, leading to a low surface dislocation density of 8.5×10^6 cm^{-2} based on electron channeling contrast imaging (ECCI) characterization (Fig. 3(e)). The decent peak intensities and full width at half-maximum (FWHM) values in the room temperature photoluminescence (RT-PL) of 3-stack InGaAs/GaAs QWs grown on top of the GaAs microridges demonstrate a great promise toward the monolithic integration of gain chips on Si-based photonic circuits, using the SAH approach.

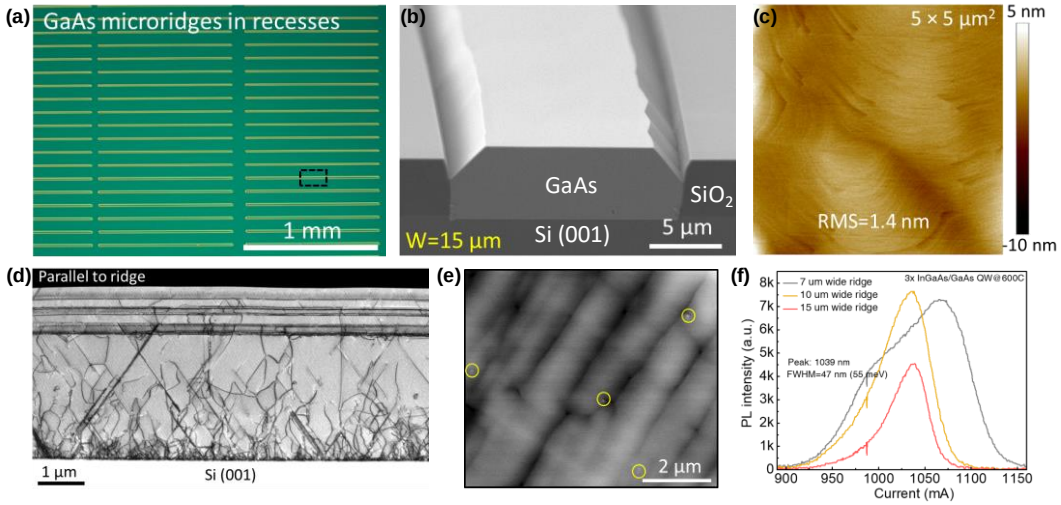

Fig. 3. (a) Large scale optical microscope image of GaAs microridges on Si after SAH. (b) Tilted SEM image of one 15-μm-wide GaAs microridges on flat-bottom Si recesses. (c) 5×5 μm^2 AFM image of the GaAs microridge surface. (d) Cross-sectional scanning transmission electron microscopy (STEM) image of one 15-μm-wide GaAs microridge in parallel direction, inserted with three stacks of InGaAs/GaAs SLSs. (e) Exemplary ECCI image of the high quality GaAs microridge surface. (f) RT-PL spectra of 3-stack InGaAs/GaAs QWs on 3.4 μm thick GaAs microridges with various ridge widths.

IV. Acknowledgement

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V. Reference

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