Report

4854a

Manufacturing report

- Confidential Information -

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Contents

1 Introduction

This document describes the fabrication process of waveguides which were realized to be used for low loss waveguide characterization.

2 Design

The basic design of the structures was done by UCSB. From this design an e-beam mask was created. An overview of the maskdesign is shown below in Figure 1.

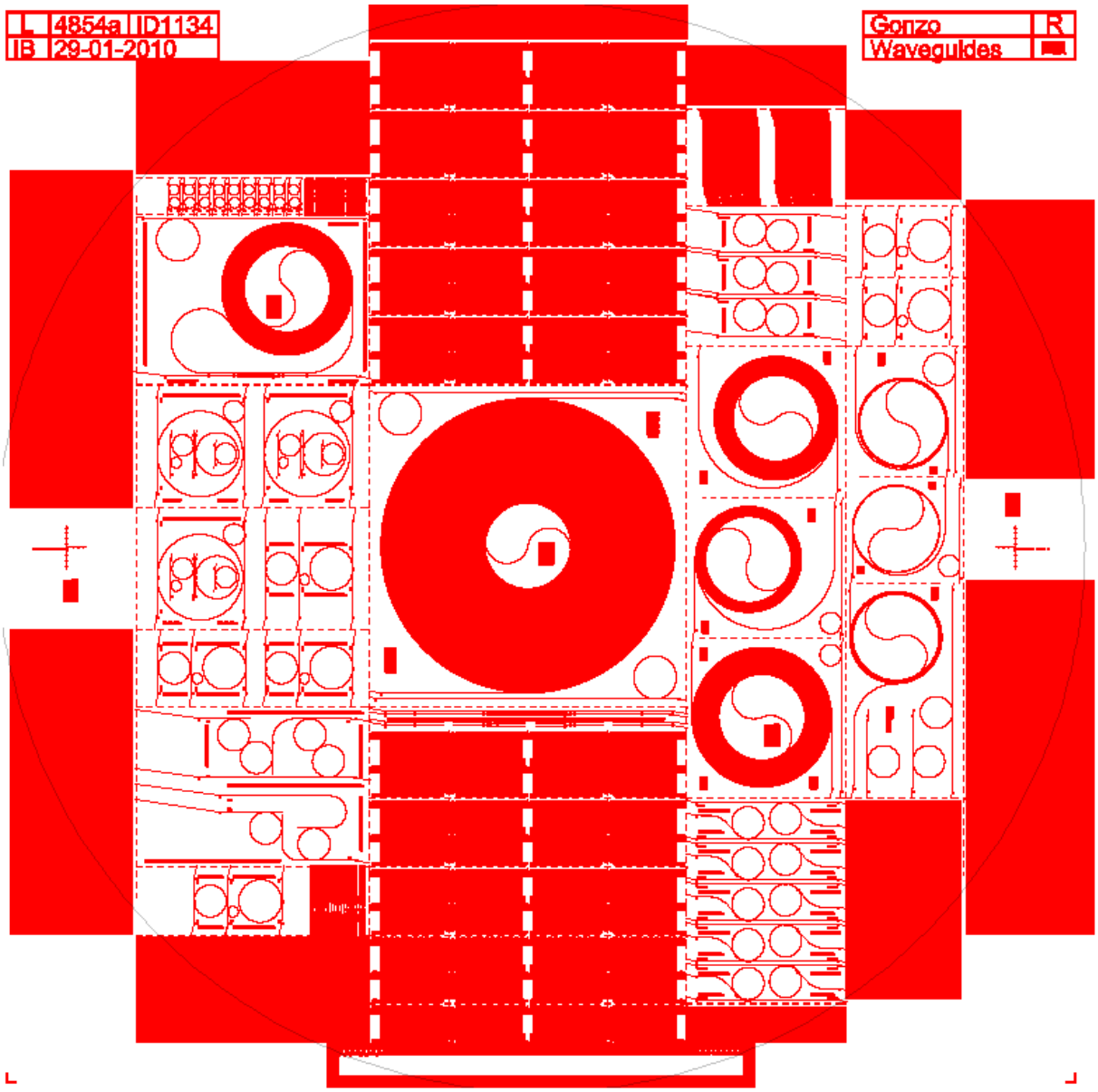


Figure 1: Screenshot of the maskfile from which the e-beam mask was generated.

3 Fabrication

3.1 Grow 8 µm thermal oxide on P-doped silicon substrates (resistivity <5-10 Ωcm)

6 OSP 100 mm heavily *p*-doped Si <100> prime grade wafers,
resistivity 5-10 Ωcm,
thickness 525 µm

3.2 Deposition of 80-90-100 nm LPCVD Si3N4

Three different nitride layerthicknesses (2 wafers each) were deposited (80-90-100 nm).

Wafernumber:	Nitride thickness
2321922-395	80 nm
2321922-394	80 nm
2258305-025	90 nm
2258305-035	90 nm
2258305-028	100 nm
2258305-044	100 nm

In each deposition run bare silicon dummies were included and the nitride thickness was measured on these dummy wafers.
The measured layerthicknesses and Cauchy parameters were.

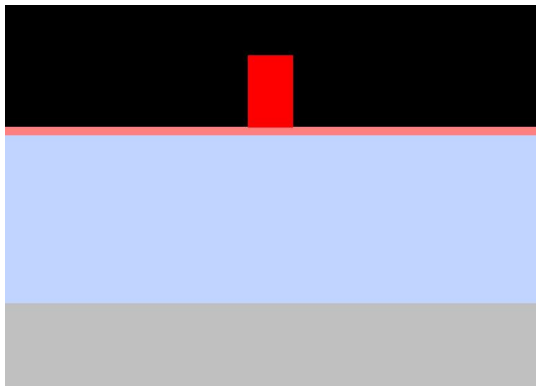
80 nm wafers:
A: 1.9873 +/- 3.41e-3
B: 8.8e-3 +/- 2.0e-3
Thickness: 79.52 +/- 7.1e-2 nm

90 nm wafers:
A: 1.9816 +/- 2.9671e-3
B: 1.2688e-2 +/- 1.7975e-3
Thickness: 92.674 +/- 8.3e-2 nm

100 nm wafers:
A: 1.9785 +/- 2.63e-3
B: 1.51e-2 +/- 1.7e-3
Thickness: 102.07 +/- 9.7e-2 nm

3.3 Lithography

Waveguides of 2.8 µm wide were defined using contact lithography

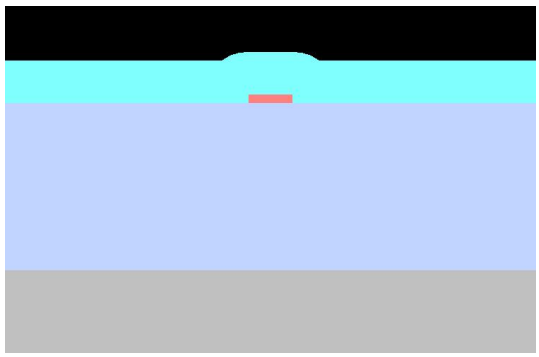


3.4 Waveguide etching

Waveguides are etched by dry etching, after which the resist is removed.

3.5 LPCVD TEOS deposition

~ 1000 nm TEOS is deposited to cover the waveguides. LPCVD oxide is used to avoid voids next to the waveguides. On a dummy wafer (grown in the same run) the layerthickness is characterized with an ellipsometer. The measured values were:
A = 1.425 +/- 2.1e-3
B = 3.5e-3 +/- 2.8e-4
Thickness = 942.0 +/- 2.5 nm



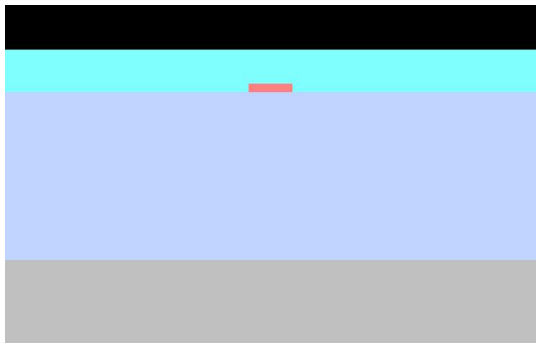
3.6 Anneal the TEOS layer

The layers are annealed at 1150°C for 3 hours, after which the layerproperties on the dummy wafer are measured again with an ellipsometer:

A = 1.448 +/- 1.9e-3
B = 3.7e-3 +/- 2.7e-4
Thickness = 869.9 +/- 2.1 nm

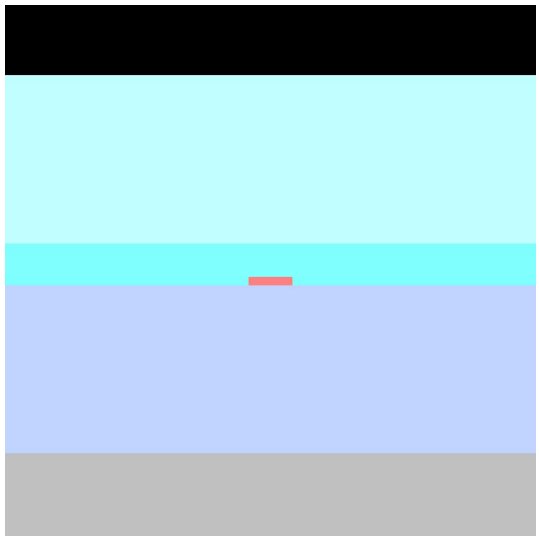
3.7 Chemical Mechanical polishing

The TEOS topsurface is CMPed to get a flat top surface.



3.8 Apply PECVD oxide

On top of the planarized LPCVD oxide PECVD oxide can be applied. A layer > 6 microns was applied. The layer properties were measured by including a bare Si dummy in each of the deposition runs. On these dummies the layer properties were measured with an ellipsometer.



Deposition on 80 nm wafers:
A = 1.4679 +/- 5.98 e-3
B = 4.09e-3 +/- 5.1 e-4
Thickness = 6743.2 +/- 50.8 nm

Deposition on 90 nm wafers:
A = 1.4711 +/- 6.2 e-3
B = 4.27e-3 +/- 5.3 e-4
Thickness = 6789.4 +/- 52.7 nm

Deposition on 100 nm wafers:
A = 1.4663 +/- 7.54 e-3
B = 4.36e-3 +/- 6.9 e-4
Thickness = 6796.1 +/- 65.4 nm

3.9 Anneal the PECVD layer

The layers are annealed at 1150°C for 3 hours.

3.10 Dicing of the wafers

6 wafers were diced and shipped to the customer on blue dice tape.