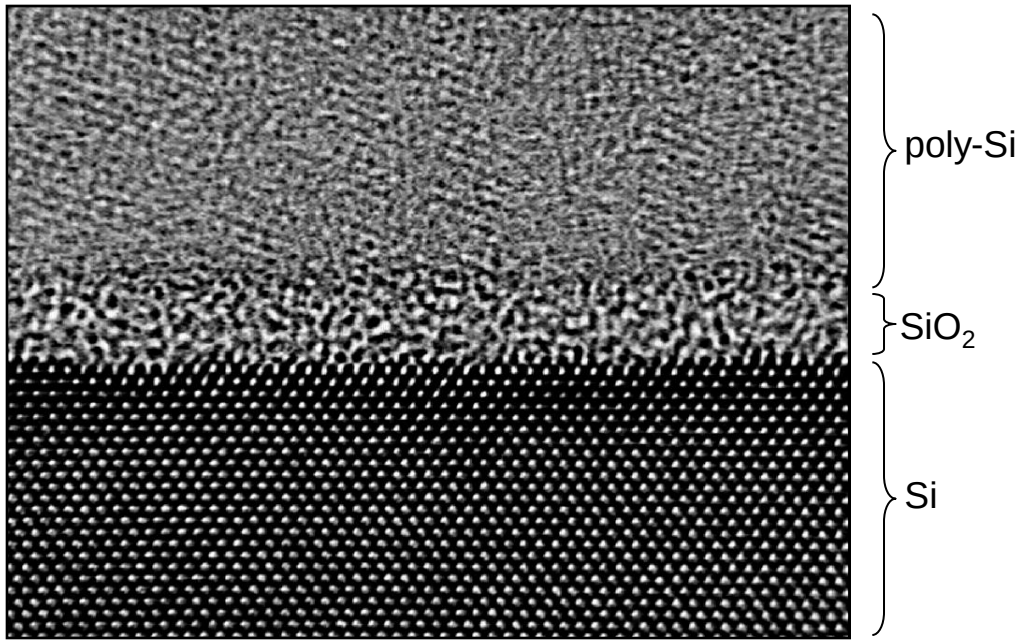
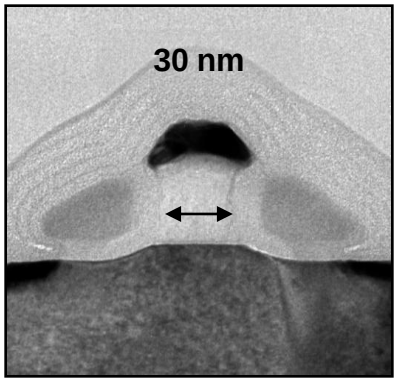
Si – SiO_2 – poly-Si interface

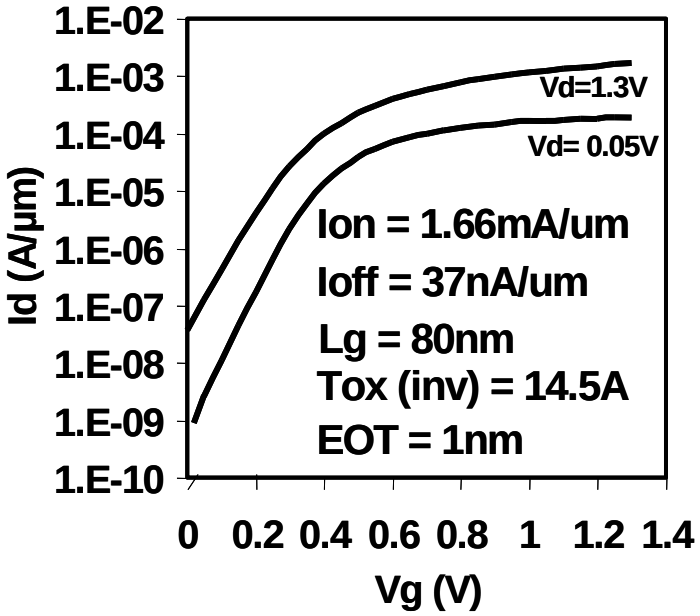


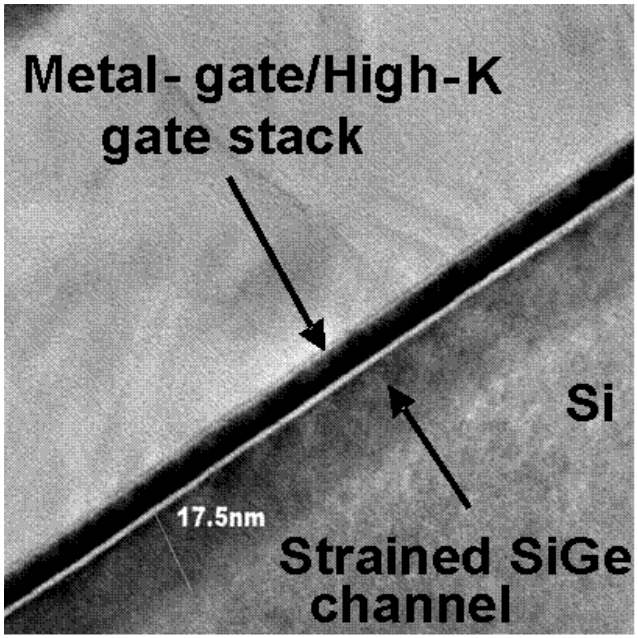
Cross-sectional transmission electron microscopy (XTEM) image of Si - SiO_2 - poly-Si interface, Bell Labs.

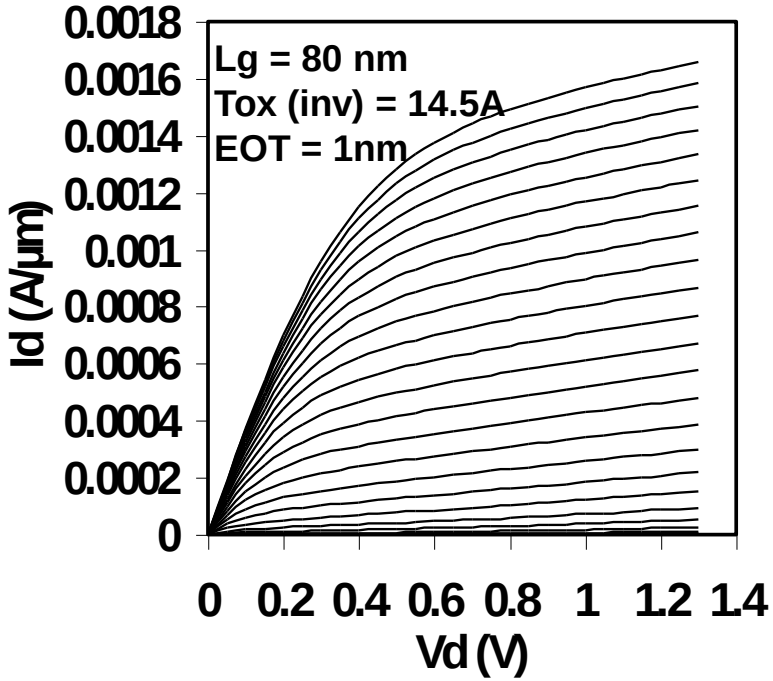


30nm Physical Gate Length CMOS Transistors with 1.0 ps n-MOS and 1.7 ps p-MOS Gate Delays"

Authors: Robert Chau, R. Arghavani, D. Barlage, G. Dewey, B. Doyle, M. Doczy, J. Kavalieros, D. Lionberger, A. Murthy, B. Roberds, R. Schenker
Conference: IEEE International Electron Devices Meeting (IEDM**), December 11, 2000, pp. 45-48.

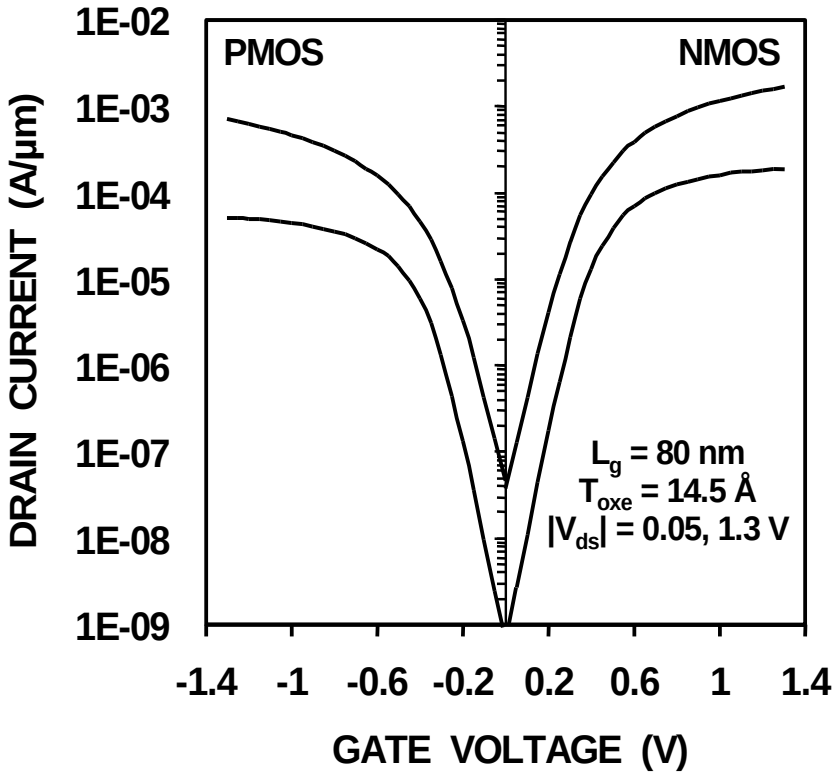


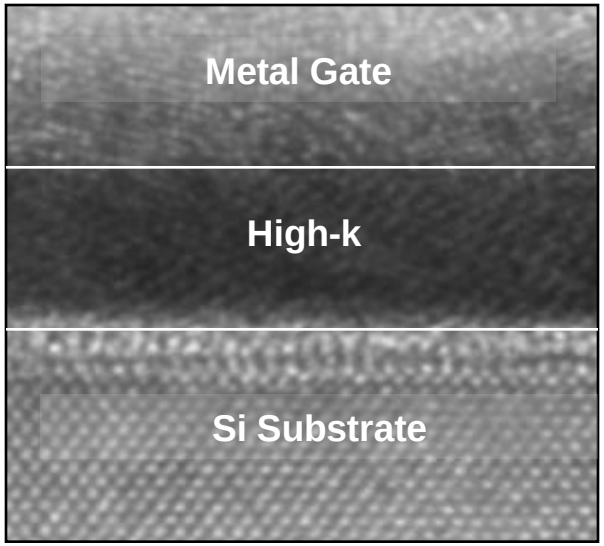




R. Chau et al. **, *IEEE Electron Device Letters*, p. 408-410, June 2004**

"High-k/Metal-Gate Stack and Its MOSFET Characteristics"
Authors: Robert Chau et.al.,
Publication: IEEE Electron Device Letters, Vol. 25, No. 6, June 2004, pp. 408-410
Date: June 2004





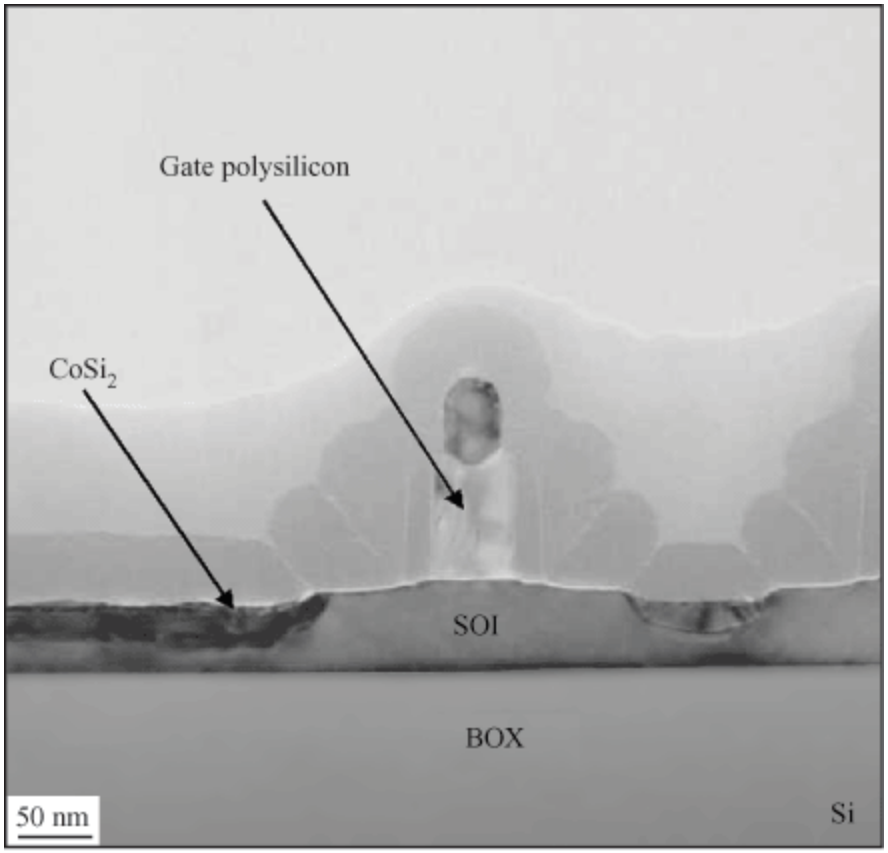
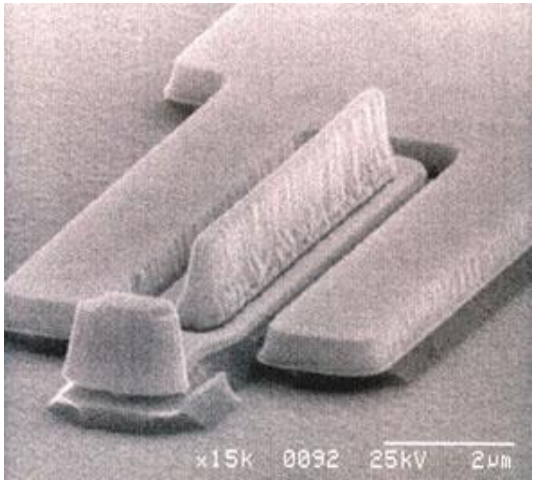


Figure 1

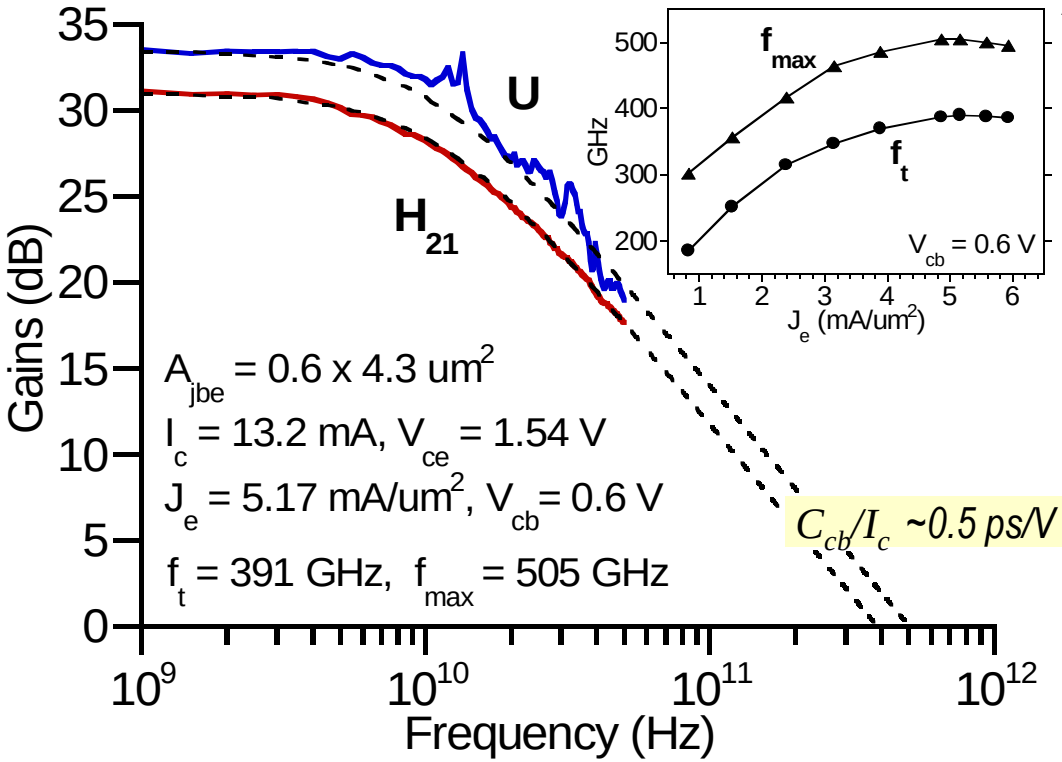
Cross-sectional TEM (XTEM) image of a 90-nm-technology-node device under development, illustrating sub-50-nm physical polysilicon gate.

90-nm MOSFET, IBM

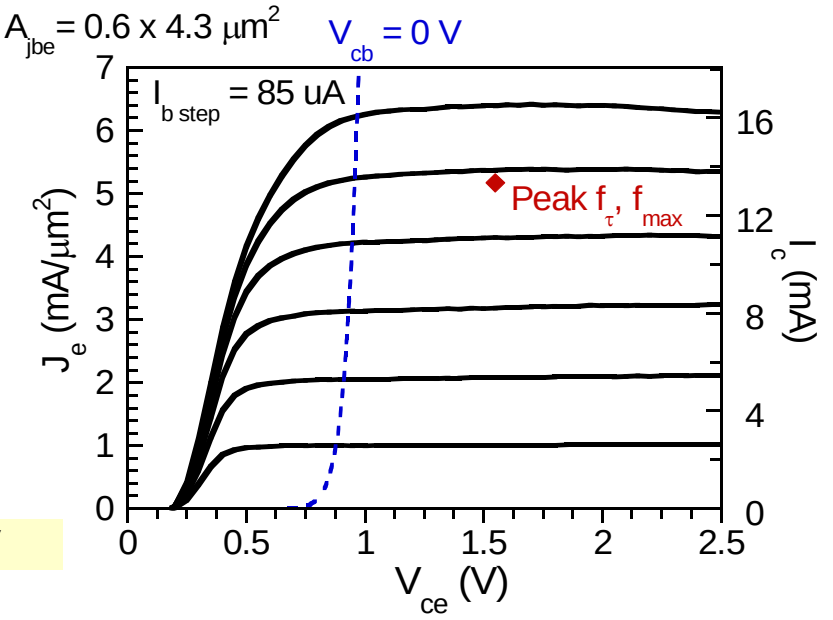


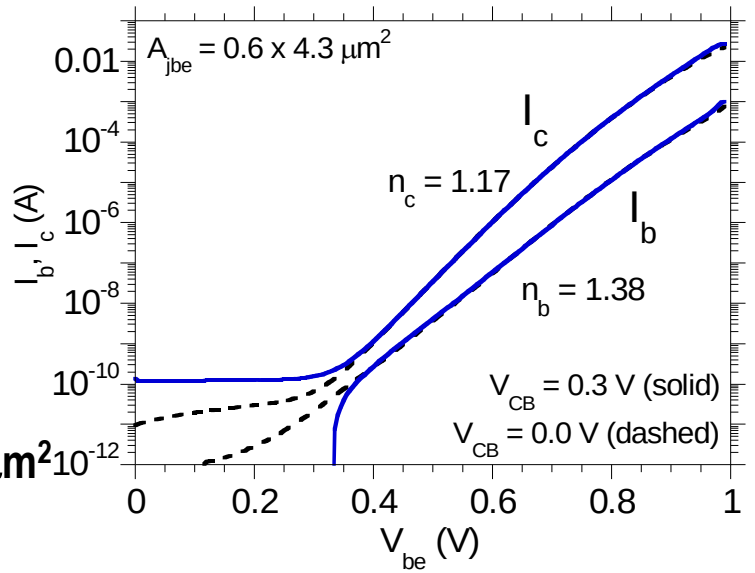
InP-based HBT, Rodwell (Griffith),
I-V curves are on next slide

DC, RF performance—150 nm collector, 47 nm transition



C_{cb}/I_c ~0.5 ps/V





Average $\beta \approx 36$, $V_{BR,CEO}$ = 5.1 V (I_c = 50 μA)

Emitter contact (from RF extraction), R_{cont} = 10.1 Ω·μm²

Base (from TLM) : R_{sheet} = 564 Ω/sq, R_{cont} = 9.6 Ω·μm²

Collector (from TLM) : R_{sheet} = 11.9 Ω/sq, R_{cont} = 5.4 Ω·μm²