Applications for Machine Learning in Semiconductor Manufacturing and Test (Invited Paper)

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Abstract

In this invited paper, applications for Machine Learning (ML) in several areas of semiconductor manufacturing and test are reviewed and potential opportunities are discussed.

(Keywords: Machine Learning, Semiconductor Manufacturing, Test)

Introduction

Utilizing the power of ML and applying it to automate and optimize semiconductor manufacturing process and associated data analysis have strong potential and become a hot hub of research interests at both academia and industry in recent years [1,2].

A wide variety of ML algorithms and models have been developed recently. Depending on whether the label is provided or not for the training data, ML algorithms can be simply categorized into supervised learning and unsupervised learning. On the other hand, from the model perspective, there exist discriminative models and generative models.

Given the large number of well-labelled historical data collected from the existing manufacturing process, supervised discriminative models typically learn from the experience to accelerate future manufacturing and design efficiency. For example, to avoid human intervention in die inking during the die screening, a multilayer perceptron (MLP) classifier model is proposed to automatically identify inking patterns from the failure map with careful post-processing for correction [3].

Moreover, supervised generative models are usually employed to further explore the design space, and facilitate or even replace manual design for better manufacturability. Given its outstanding performance and great extensiveness, one generative model, Generative Adversarial Network (GAN) [4], draws a lot of attention in recent years. In the layout design phase, [5] proposed WellGAN based on conditional GAN (CGAN), a supervised version of GAN, to automatically generate well layouts for analog and mixed signal (AMS) circuits, which was totally relied on manual design before. In the manufacturing process like lithography, CGAN can also be applied to effectively model 3D aerial image [6] and resist patten [7] based on the given mask patterns, which significantly boost the manufacturing efficiency.

Defects are inevitable during semiconductor manufacturing, making it critical to screen them out during production test flow to prevent them from becoming failures in customer applications. For this purpose, unsupervised learning models are utilized to capture and learn the normal wafer data distribution for efficient anomaly detection. Several unsupervised multivariate outlier modeling methods are studied in [8], including both generative covariance-based modeling and discriminative one-class support vector machine (SVM), to capture and analyze rare customer failures. In addition, unsupervised learning helps discover unknown production issue, which is hard to be labelled beforehand. As an example, [9] studied an unsupervised generative model, variational autoencoder (VAE), to identify and cluster wafer map patterns.

In this paper we review applications of ML algorithms for different manufacturing phase. First, we discuss ML for smart manufacturing including yield prediction, process excursion detection, and flow simplification. Then, we present ML based Design for Manufacturability (DFM) tools and checkers for more robust and reliable manufacturing. Finally, we explore recent development in advanced outlier detection for manufacturing test using unsupervised ML techniques.

ML for Smart Manufacturing

A. Yield Prediction and Analysis

It is important for semiconductor manufacturing to predict yield and understand the impact of process parameters on yield. Fig. 1 shows an example of correlation of product yield drop and process recipe change causing two parameters to change. Such correlation can be recognized automatically by certain supervised discriminative ML algorithms such as regression and Convolutional Neural Networks (CNN) for pattern recognition. For

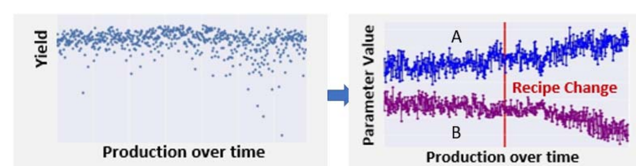

Fig. 1 Product yield vs. process parameters analysis.

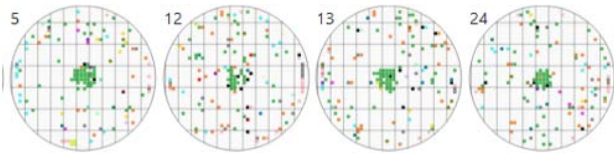

Fig. 2 Wafers with center abnormality.

example, [10] proposed to apply multivariate adaptive regression splines (MARS) with features selected by genetic algorithm (GA) to efficiently estimate yield production across different fabrication processes and design generations, which greatly reduces the number of required simulation or fabrication data.

B. Manufacturing Process Excursion Detection

At wafer fab, as the technology feature size keeps scaling down, the number and complexity of process steps and tools keep increasing, which make process excursions unfortunate but inevitable occurrences. Detecting process excursions as early as possible will be critical to avoid huge scrap and test cost, as well as potential quality issues. Unsupervised generative ML algorithms such as GAN or autoencoder for abnormal pattern recognition [11] and hot spot checking can be used for such excursion detection based on process KLA inline scan data, process tool data, as well as probe wafer map as shown in Fig. 2.

C. Manufacturing Flow Simplification

In addition, unsupervised ML algorithms can be used to optimize the manufacturing test flow, such as enabling package Burn-In (BI) elimination [12,13] based on KLA defect and probe test data to identify “risky” materials to send to BI stress. [14] describes a kernel-based clustering (KBC) algorithm which is a type of unsupervised learning. It is based on wafer probe test data to identify potential cluster defect and send the nearby risky dies to extended stress, e.g., package BI. Fig. 3 shows one example of NVM contact to gate misalignment process issue identified by the KBC.

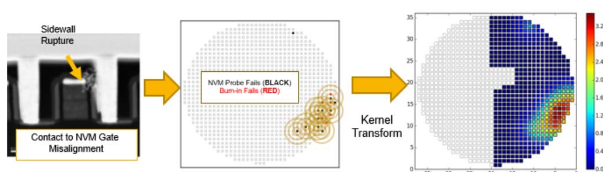

Fig. 3 Kernel based clustering for NVM misalignment.

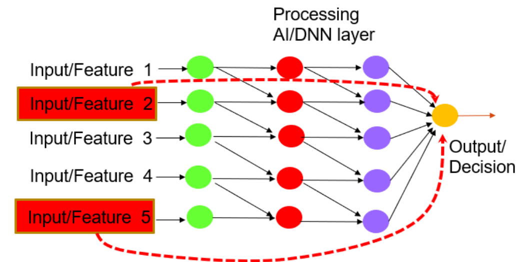

Fig. 4 DNN to improve DFM.

ML to Improve Design for Manufacturability

Design for Manufacturability (DFM) tools and checkers are instrumental to semiconductor manufucturing with important objectives: robust process capability tolerant to variations, higher manufacturing gross margins, as well as stringent automotive reliability and functional safety requirements. This necessitates a high level of automation to check the sign off items, some of which are currently done with manual checklists and reviews. Machine learning, especially Deep Neural Network (DNN), can be naturally applied to automoate and improve the DFM tools taken all the critical inputs and key metrics into consideration. As shown in Fig. 4, a DNN is trained to predict possible design violations/failures. The inputs can include, but not limited to, previous CQC (customer quality complaint) database info, technology metal options, Design Rule Checks (DRCs), physical integration, yield criteria, etc. Scoring guidelines for each of the different requirement and a pass/fail criterion with corresponding goals to optimize, would also be inputs. The decision making of these neural networks will be interpreted to identify “critical design/layout features” that are strongly correlated with the predicted violations/failures. Critical features can be found based on the output decision’s high sensitivities and be provided as feedback to the design/test process.

ML for Manufacturing Test

Manufacturing test process is crucial to prevent chip failure at customer side. As shown in Fig. 5,

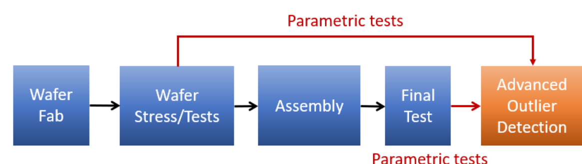

Fig. 5 Semiconductor manufacturing test flow.

parametric tests are one of the major types of tests during the manufacturing test flow. To analyze and learn from rare customer return failures, parametric tests play an important role during the advance outlier detection process for screening out future failures. Multivariate unsupervised outlier detection using ML methods have shown great potential in this area, with recent developments including SVM, VAE, Gaussian and Isolation Forest models [8,9].

In [15] we proposed a novel unsupervised discriminative self-labeling technique with reversible transformation to effectively screen out rare customer return failures. Specifically, as shown in Fig. 6, for each input data sample, we perform multiple distinct transformations to generate a new dataset labelled with its corresponding transformation types, then a classifier is trained to learn the decision boundaries across different transformations over normal data distribution. During the inference of customer return failures, outlier tends to have worse classification accuracy compared to normal data, as the classifier well captures the transformed normal data manifold. In addition, reversible neural network is incorporated to well preserve data information after transformation with good flexibility to generate large number of distinct transformations. The rare customer failures can be well captured by this approach, proved by industrial automotive microcontroller datasets to reduce yield loss and avoid test escape.

Conclusion

We have reviewed the recent development in ML algorithms and the applications of ML for semiconductor manufacturing and test areas.

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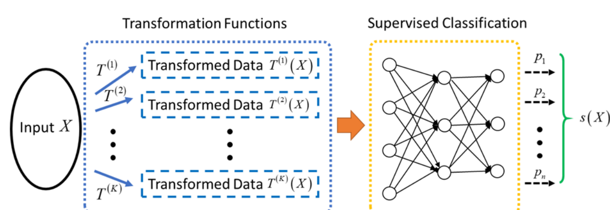

Fig. 6 Unsupervised self-labeling framework.

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