Bias Circuit Design for Microwave Amplifiers

ECE145A/218A UCSB/ECE

We need to provide a stable bias condition for our device in any amplifier application.

Bipolar transistors: Must force the DC (average) value of VCE and IC to desired values and keep them constant using feedback techniques.

Never fix VBE: $IC = ISE\ e^{VBE/VT}$. IC varies exponentially with temperature.

Never fix IB: $IC = \beta\ IB$ β varies tremendously from device to device and increases with temperature as well (0.7%/degree C).

Field Effect Transistors: Force VDS and ID to desired values and keep them constant. The main weakness of microwave FETs is the variation in threshold voltage, VT, and the transconductance g_m from device to device and with temperature.

In some cases, bias stabilization may be accomplished with passive circuit elements. An emitter or source resistor provides negative feedback to stabilize bias current. For example, as seen in Fig. 1, RS is a self-bias resistor. VGS = - ID RS in order to provide a negative gate-source voltage. If ID increases, VGS decreases to compensate. But, wiring inductance is introduced in the source circuit, even with a bypass capacitor across RS. This will become significant when $\omega L = 1/(10g_m)$ which is generally a very small inductance.

Referring again to Fig. 1, the BJT circuit uses the conventional 4 resistor bias approach where the emitter resistor provides negative feedback stabilization against drift of the bias point with temperature or device parameter variation from batch to batch of devices.

But, these circuits are not often used for RF applications because the biasing resistances also load the circuit and reduce the gain. Therefore, circuit techniques that permit use of a directly grounded source or emitter connection are preferred for high frequency amplifiers when implemented using discrete components on PC boards. In RFIC implementations, more flexibility is possible. One can use CC, CB, CG, CD connections as well as choosing device areas to optimize circuit performance.

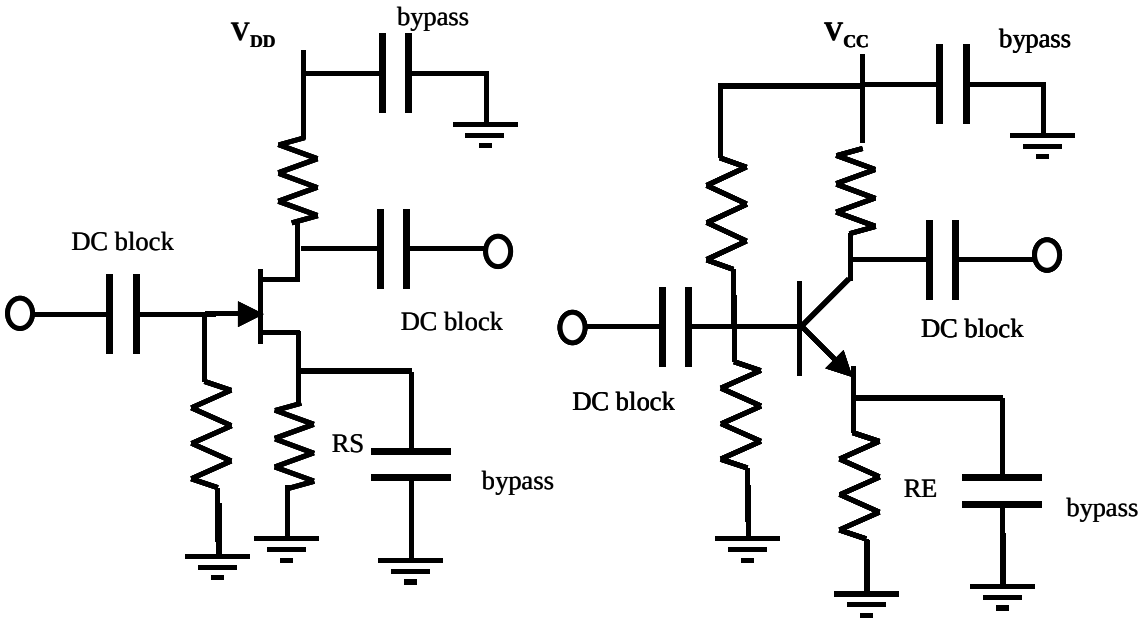


Fig. 1. Passive bias circuits for MESFET (usually depletion mode) and BJT.

The MESFET (or JFET or PHEMT) circuit uses two power supplies when the source is grounded on a PCB because the threshold voltage of a typical microwave FET is negative. Microwave FETs are always n-channel.

So, in some cases, RFCs are used for biasing as shown in Fig 2. They provide high Z at the design frequency and so will not usually sacrifice gain. However, they always have resonances, so a complete RFC equivalent circuit model is essential if the circuit performance is to be accurately predicted.

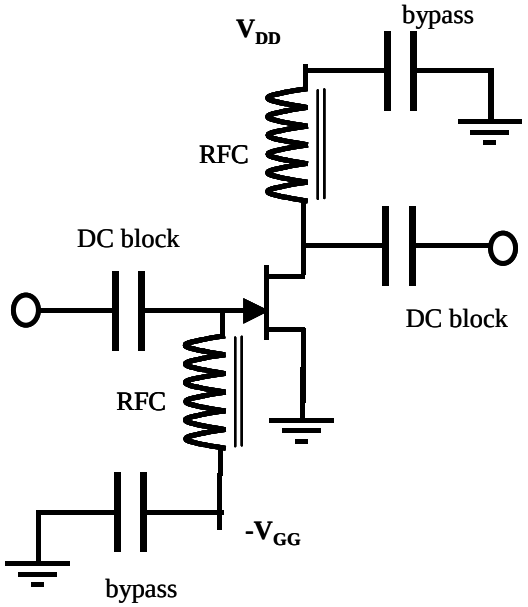


Fig. 2. Example of GaAs or InP FET bias insertion using 2 power supplies and RFC.

When possible, a better approach to bias insertion than resistors or RFCs is to use the matching network itself to insert bias voltages. This is possible when a shunt shorted stub or shunt inductor is connected to the input or output terminals of the device without any series DC blocking or impedance matching capacitor. The grounded end is bypassed with a grounded capacitor with low impedance over the full range of frequencies. See fig. 3.

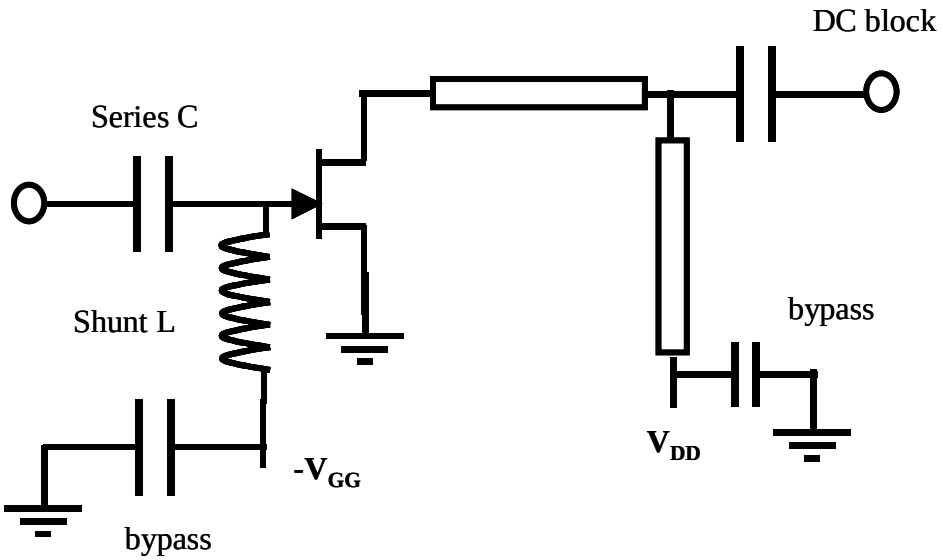


Fig. 3. Biasing the device through the matching networks. Examples of lumped and distributed element matching are shown.

Another bias insertion method that is widely used and more suitable for microwave circuits utilizes high impedance lines that are one-quarter wavelength at the design frequency. This is shown in fig. 4 as a bias feed for the drain. If a low impedance bypass capacitor is used to short the bias feed end, the $\lambda/4$ line transforms the short into an open at f_O. An added bonus comes from short circuiting the even harmonics because the line is also $\lambda/2$ at $2f_O$, λ at $4f_O$, etc. This can improve efficiency of some power amplifiers or can be used with a resistor to force the stability factor $k > 1$ at $2f_O$ by killing high frequency gain with lossy loading.

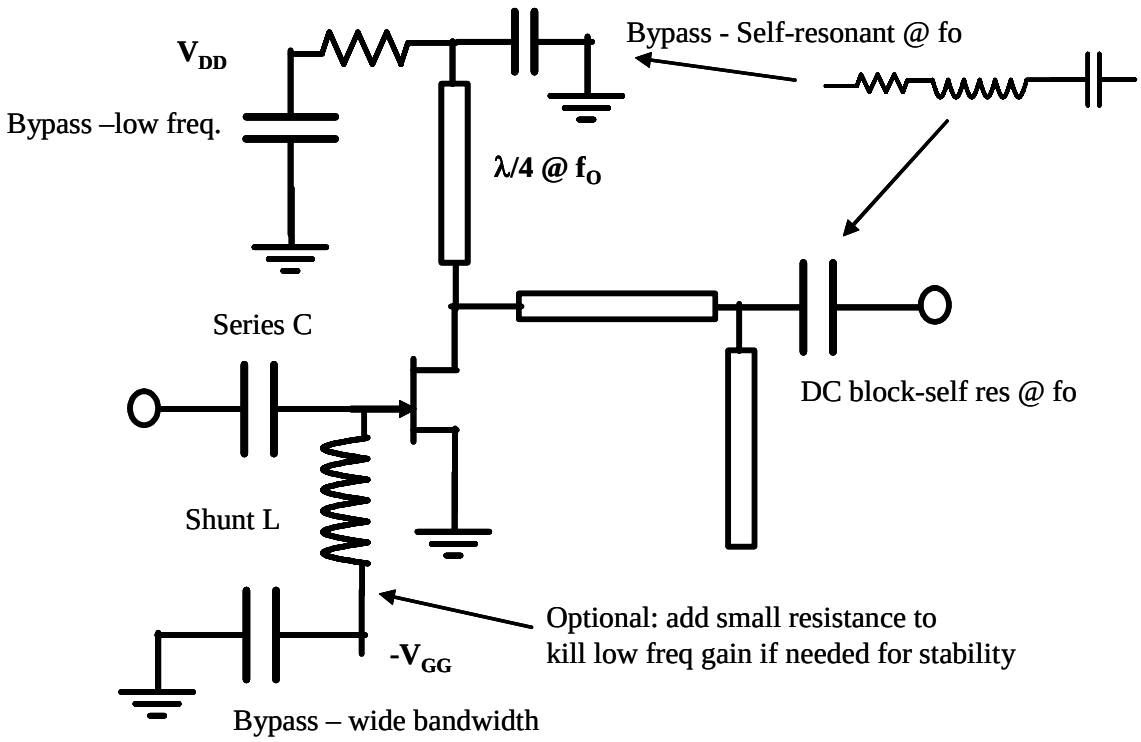


Figure 4. Bias insertion with quarter wave high impedance line.

Active bias circuit

We have shown in Fig. 1 that passive bias circuit approaches using resistors can load the amplifier creating extra losses and add source or emitter inductance. The best practice is to directly ground the emitter or source for microwave amplifiers. But, grounding the emitter or source leaves the devices wide open to DC bias problems such as thermal runaway on the BJTs or temperature drift of the bias point for FETs. So, an active feedback circuit such as shown in Fig. 5 is widely used for biasing. While an op amp could be used, this requires an extra power supply, so a simpler approach using a PNP transistor is frequently more efficient.

Q2 can be nearly any lower frequency PNP with sufficient current capability. V_{DS} is set by the voltage divider

$$V_1 = V_{DD}\left(\frac{R2}{R1+R2}\right) - V_{D1} \qquad \text{and} \qquad V_{D1} = -V_{BE,Q2} = 0.7\text{V}$$

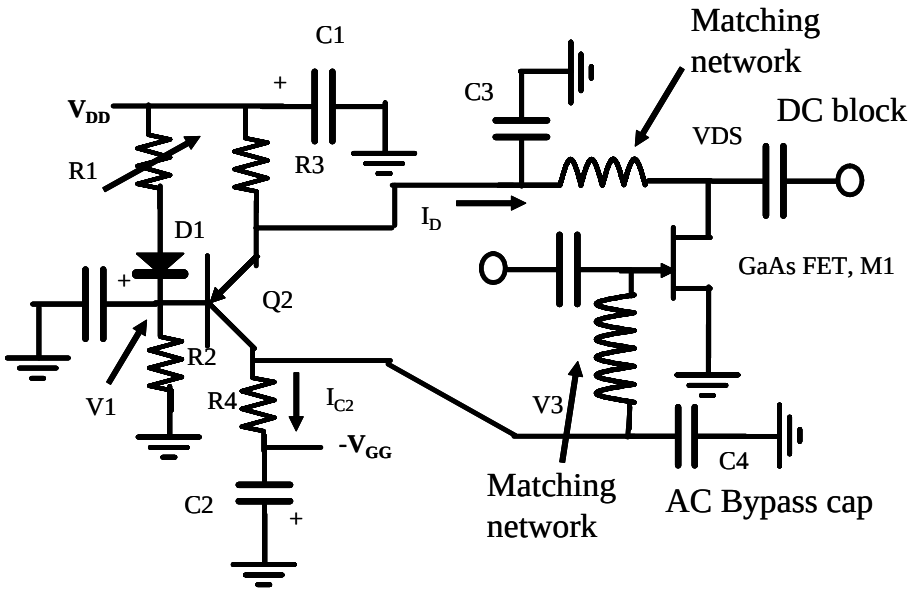


Fig. 5. Active bias generator (on left) provides gate and drain voltages to the GaAs FET.

So, $V_{DS} = V_1 - V_{BE,Q2} = V_{DD}[R2/(R1+R2)]$.

$I_D + I_{C2} = (V_{DD} - V_{DS})/R3$ $\qquad$ $I_{C2} << I_D$

$I_{C2} = (V3 + V_{GG})/R4$

D1 is provided for temperature compensation and can be a diode-connected PNP of the same type as Q2.

The DC feedback can be seen as follows: Suppose that

1. I_D increases (maybe due to temperature variation or change in device)
2. Then, the voltage drop across R3 will increase, reducing $V_{BE,Q2}$.
3. I_{C2} drops, reducing the voltage drop across R4. This reduces V_{GS} and I_D to correct for the change in step 1.

C1 and C2 are low frequency bypass capacitors. These are typically polarized tantalum or electrolytic caps that are used for stability of the active bias circuit. C3 and C4 are high frequency bypass caps. These must NOT be tantalum or electrolytic types, but must be high quality ceramic chip caps with very low series inductance. Any series L must be included as part of the matching network.

When choosing values for C3 and C4, we must recognize that the active bias generator is a feedback system. R3C3 and R4C4 add two low frequency poles in the feedback loop. A second order FB system can be underdamped (ringing) or oscillatory if the phase margin is insufficient. For stability, create a dominant pole with one of the two RC networks with one time constant at least 10 times larger than the other. This should provide nearly a 90 degree phase margin.

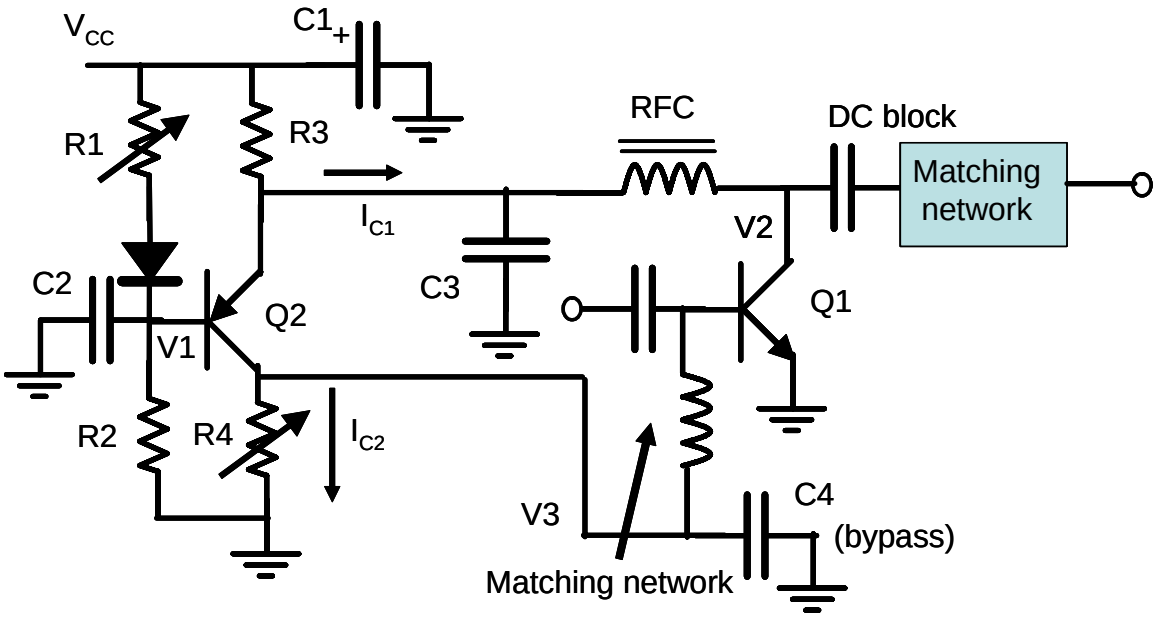


Fig. 6. A similar active feedback approach can be used for biasing a BJT.

DC Biasing of RF feedback amplifiers. This approach provides good bias stability for microwave feedback amplifiers. See Fig. 6.

I3 = VBE/R3

I2 = I1 if IB is small

VCE = VBE + I2 R2

I1 = (VCC – VCE)/R1

IC = I1 – I2

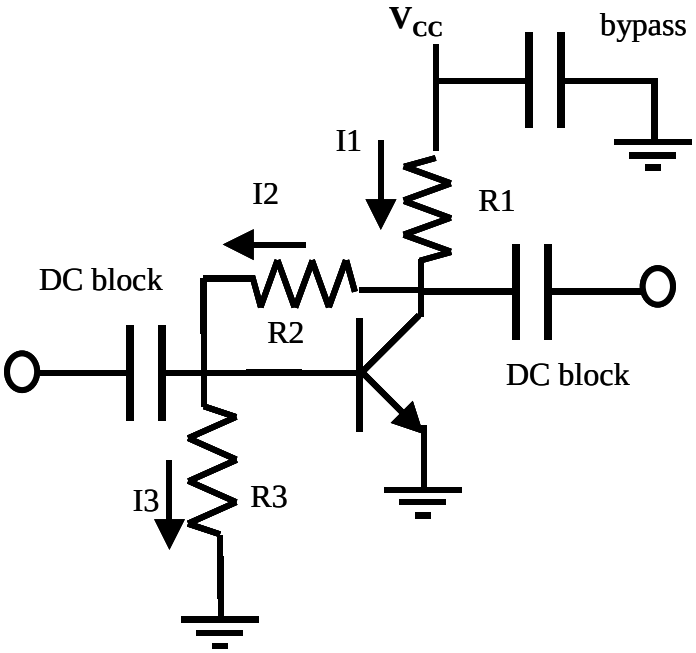
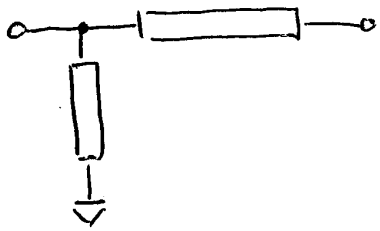


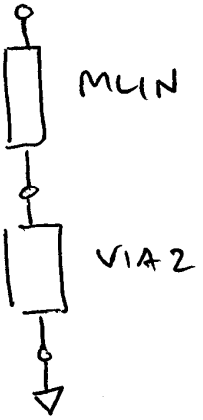
Fig. 7. Shunt-shunt feedback DC biasing example.

Implementation Issues for amp.

1. Shunt shorted stub. can implement shunt L or C



Tlines - Microstip library



MSub

use linecalc to determine W, L of line.

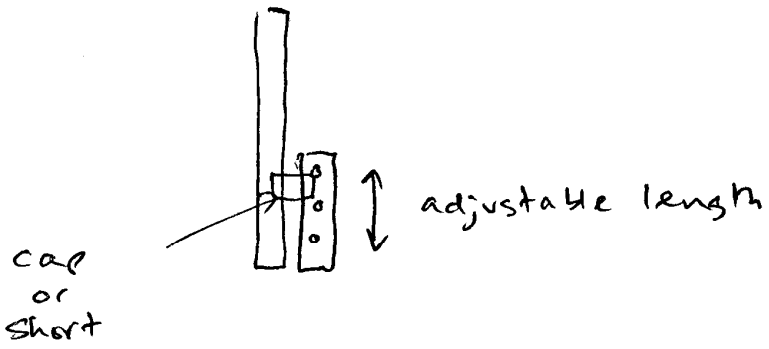
Copper: $\sigma = 5.8 \times 10^{7}$ S/m

~~T = 43 μm~~

T = 43 μm.

50Ω $\epsilon = 4.5$ $K_{eff} = 3.41$ $v_p = \frac{c}{\sqrt{3.41}} = 1.62 \times 10^{10}$ cm/s

Alternate form of construction:

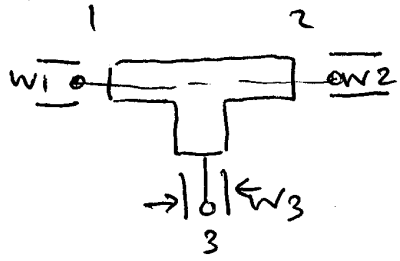


2. Open Stub Shunt C or L

MLEF model calculates end capacitance.

3. Corners. Mcorn 

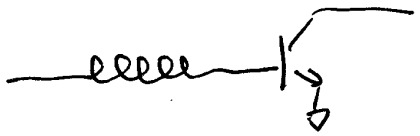
4. T junction.



MTEE

length measured from center of line

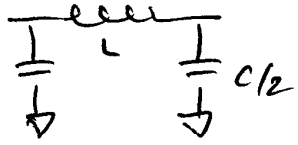
5. Series inductor - implements series T-line.



estimate: $L = \frac{Z_0 l}{v_p}$

but, will have some error since

use high Z_0 line.



$C = \frac{l}{v_p Z_0}$

ex. $Z_0 = 100\Omega$

$L \cong 6\,nH/cm$

For more accurate design, use Smith chart

Normalize chart to Z_0.

ex. suppose $z_L = 1 + j1$ at 50Ω. Simple series L

$z_L = 0.5 + j0.5$ at 100Ω

match from 0.5 to z_L

problem. constant $|\Gamma|$ circle is not on same center as const. r circle.

we get $z_L = 0.67 + j0.45$

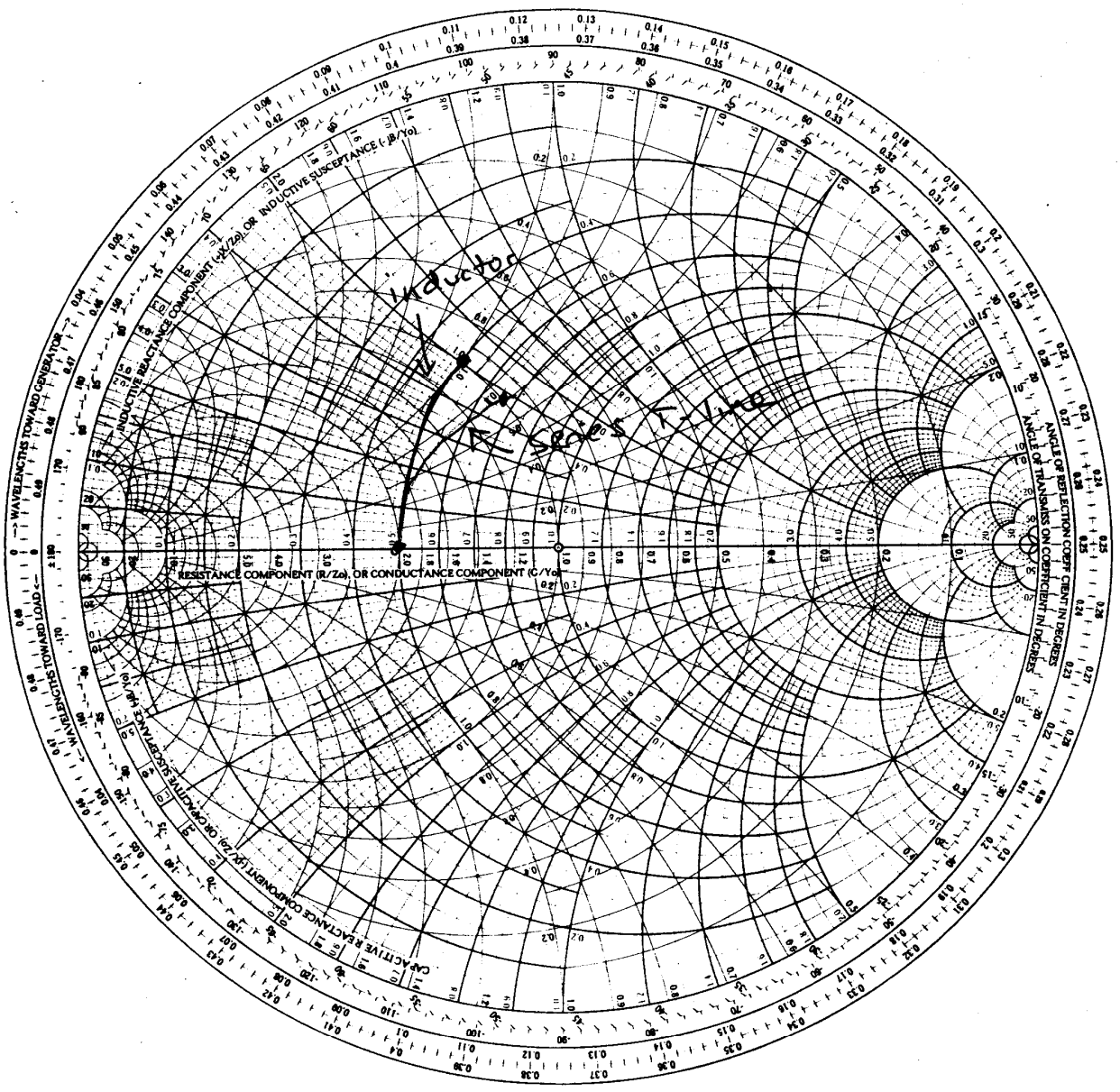
some error. will get worse for more L.

NAME | TITLE | DWG. NO.

DATE

SMITH CHART FORM ZY-01-N | COLOR BY J. COLVIN, UNIVERSITY OF FLORIDA, 1997

NORMALIZED IMPEDANCE AND ADMITTANCE COORDINATES



RADIALLY SCALED PARAMETERS

TOWARD LOAD —> | <— TOWARD GENERATOR

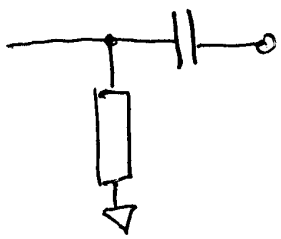
SWR | RTN LOSS (dB) | RFL COEFF. ρ

ATTEN. (dB) | S.W. LOSS COEFF | RFL LOSS (dB) | S.W. PEAK (CONST. P) | TRANSM. COEFF. P | TRANSM. COEFF. E or I

CENTER

ORIGIN

what about series C ?

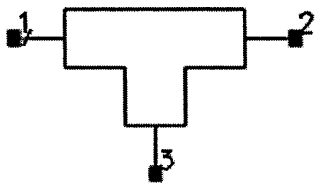


- no t-line implementation
  must use chip cap with model.
  (or MIM)
- verify with NA

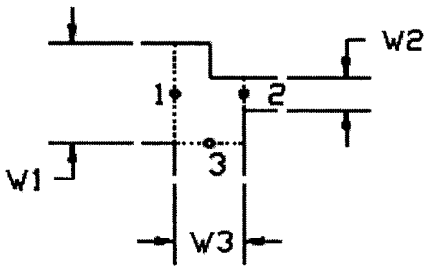
Distributed Components >Chapter 2: Microstrip Components
Print version of this Book (PDF file)

MTEE (Microstrip T-Junction)

Symbol



Illustration



Parameters

Subst = microstrip substrate name

W1 = conductor width at pin 1, in specified units

W2 = conductor width at pin 2, in specified units

W3 = conductor width at pin 3, in specified units

Temp = physical temperature, in °C

Range of Usage

$0.05 \times H \leq W1 \leq 20 \times H$
$0.05 \times H \leq W2 \leq 20 \times H$
$0.05 \times H \leq W3 \leq 20 \times H$
$Er \leq 20$
$Wlargest/Wsmallest \leq 5$
where
Wlargest, Wsmallest are the largest, smallest width among W2, W2, W3
$f(GHz) \times H\ (mm) \leq 0.4 \times Z0$
where
Z0 is the characteristic impedance of the line with Wlargest

Notes/Equations

1. The frequency-domain model is an empirically based, analytical model. The model modifies E. Hammerstad model formula to calculate the Tee junction discontinuity at the location defined in the reference for wide range validity. A reference plan shift is added to each of the ports to make the reference planes consistent with the layout.

2. The center lines of the strips connected to pins 1 and 2 are assumed to be aligned.

3. For time-domain analysis, an impulse response obtained from the frequency-domain analytical model is used.

References

[1] E. Hammerstad, "Computer-Aided Design of Microstrip Couplers Using Accurate Discontinuity Models," *MTT Symposium Digest,* 1981.

Equivalent Circuit