# Direct Digital Synthesis (DDS)

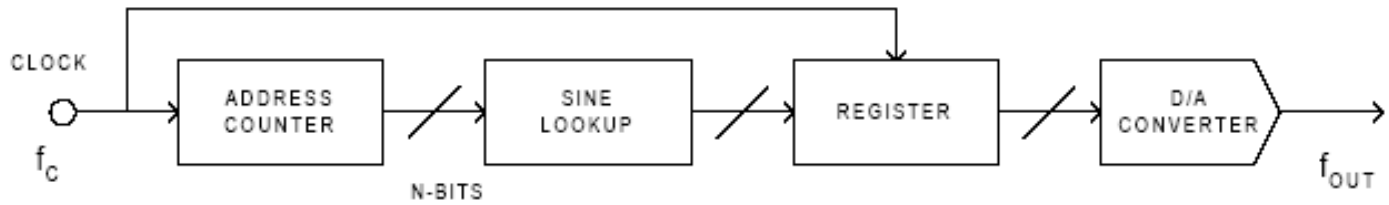



Figure 1-1. Simple Direct Digital Synthesizer

- Micro-Hertz frequency, sub-degree phase resolution
- Extremely fast hopping – no settling time constraints
- Phase-continuous frequency hops
- Digital control
- Precise quadrature phase generation for I - Q

Ref: Analog Devices DDS Tutorial, 1999.

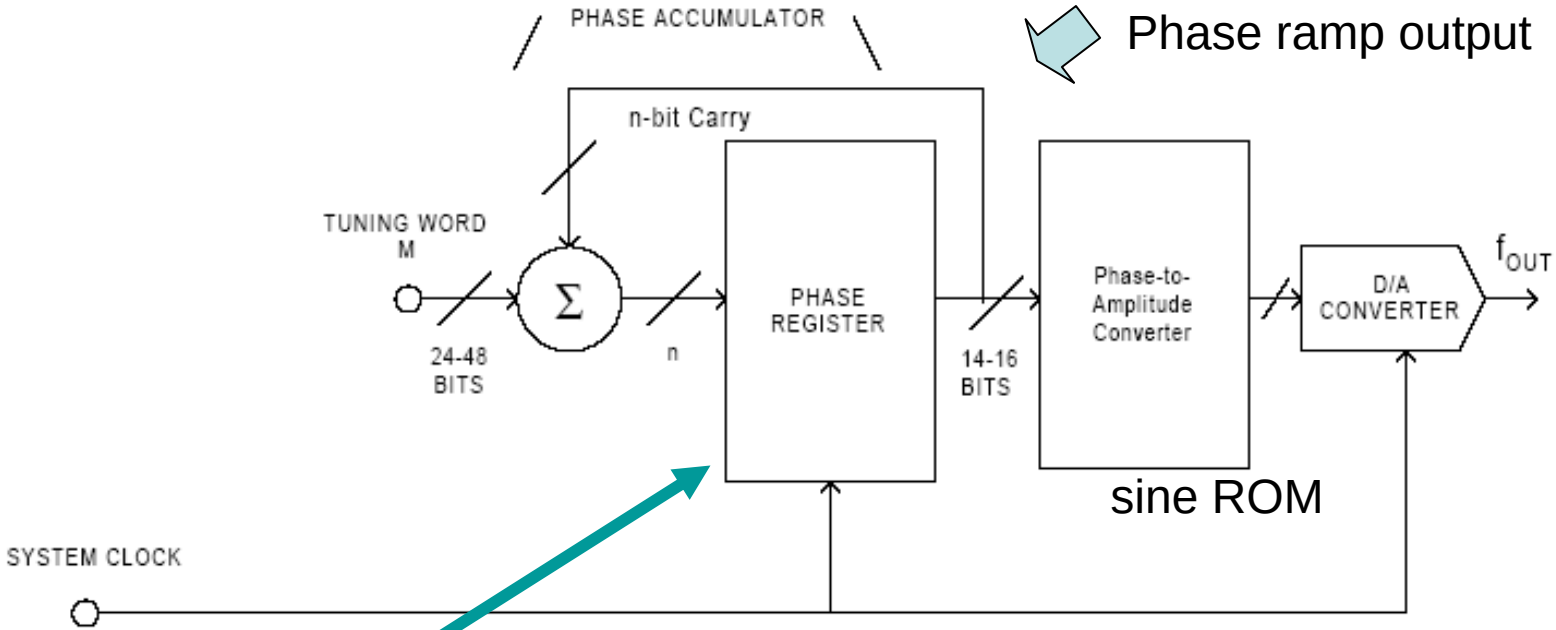



Figure 1-2. Frequency-tunable DDS System

Phase accumulator replaces the address counter
Modulus M determines the phase increment for each ref clock cycle

Ref: Analog Devices DDS Tutorial, 1999.

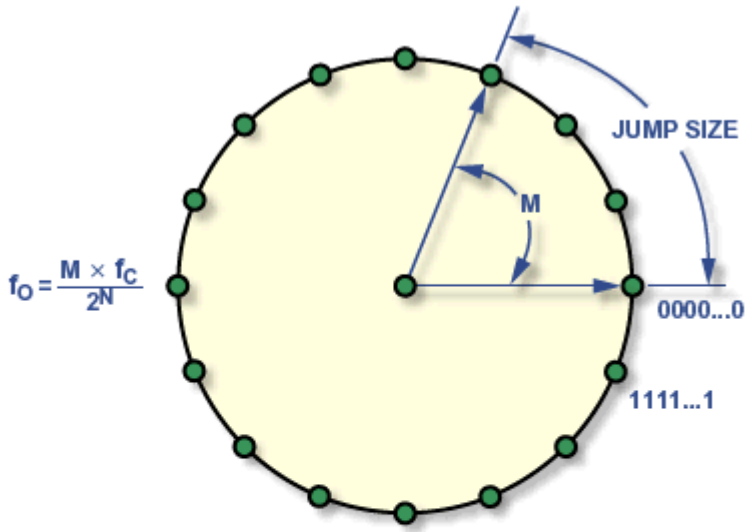
# Phase Wheel

Each rotation around the wheel corresponds to one cycle

$$F_{out} = M \bullet F_{REF} / 2^N$$

N = # bits of phase accumulator
M = binary tuning word

Ex. N = 32; M = 1
One full cycle every $2^{32}$ clocks
N = 32; M = 31
One full cycle every 2 clocks

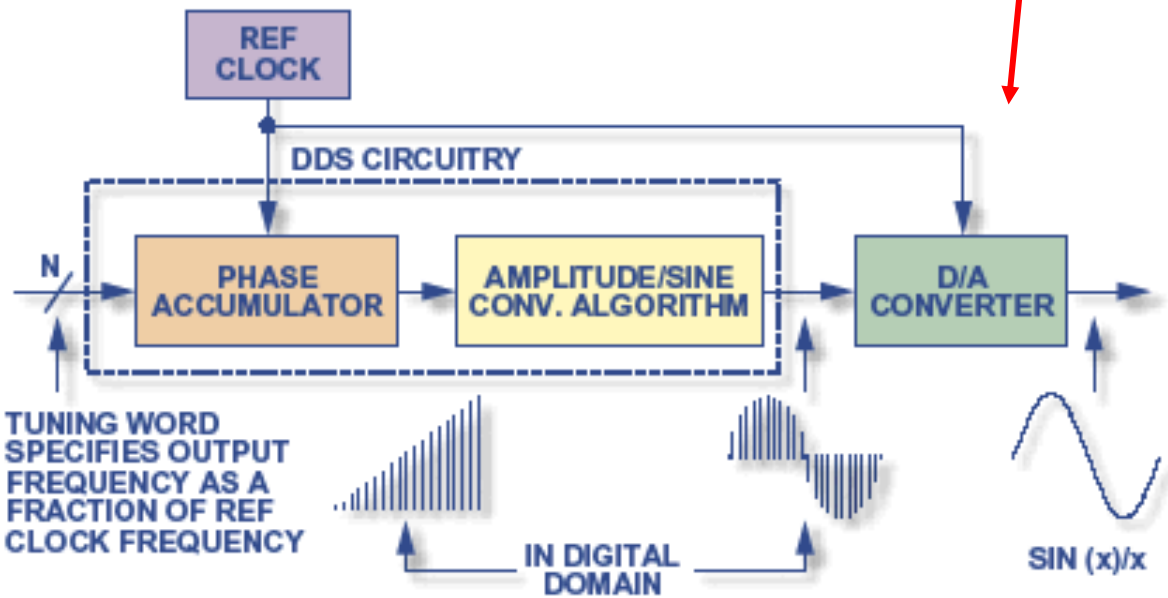



| n | NUMBER OF POINTS |
|---|---|
| 8 | 256 |
| 12 | 4096 |
| 16 | 65535 |
| 20 | 1048576 |
| 24 | 16777216 |
| 28 | 268435456 |
| 32 | 4294967296 |
| 48 | 281474976710656 |

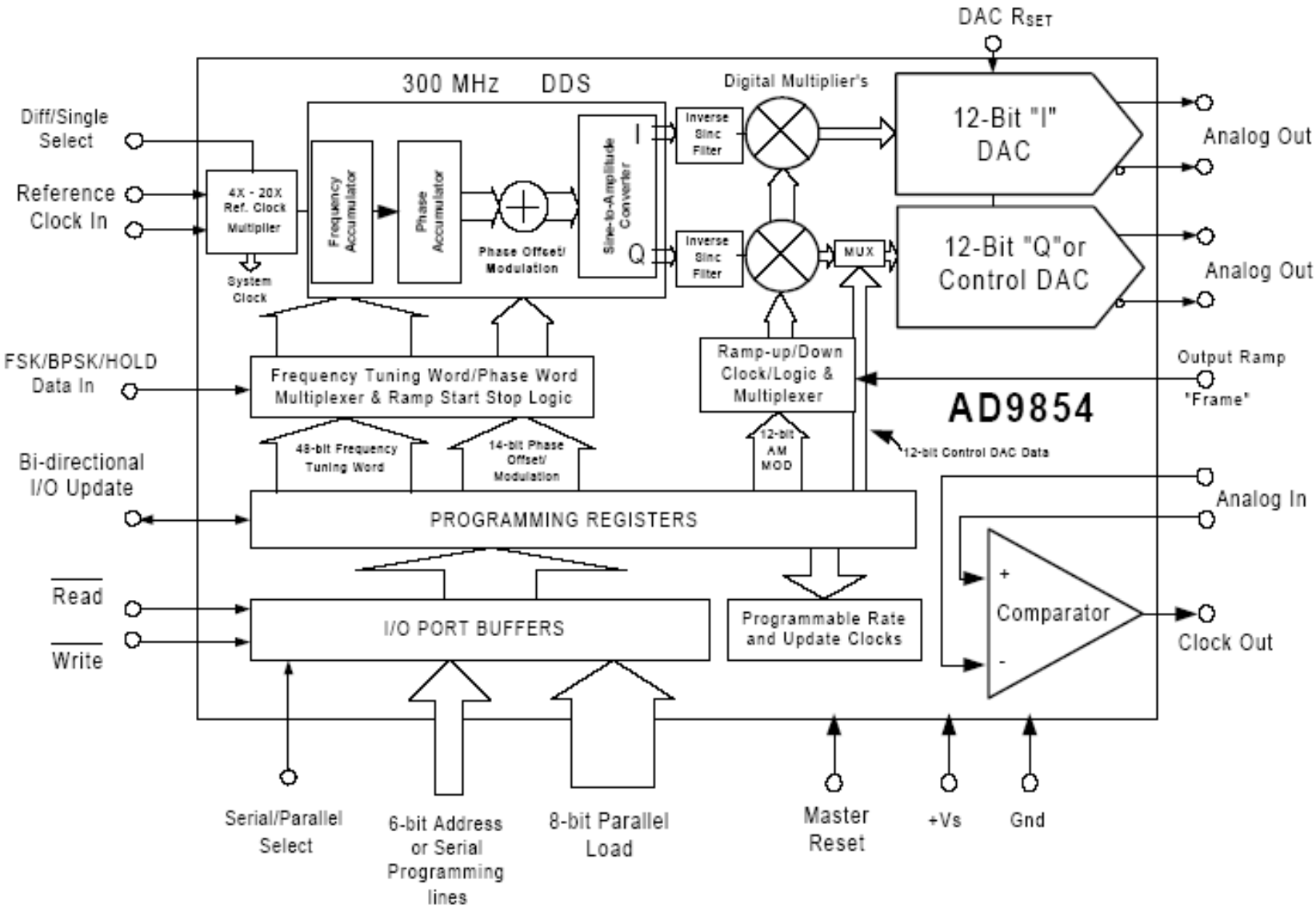
Ref: Analog Devices DDS Tutorial, 1999.

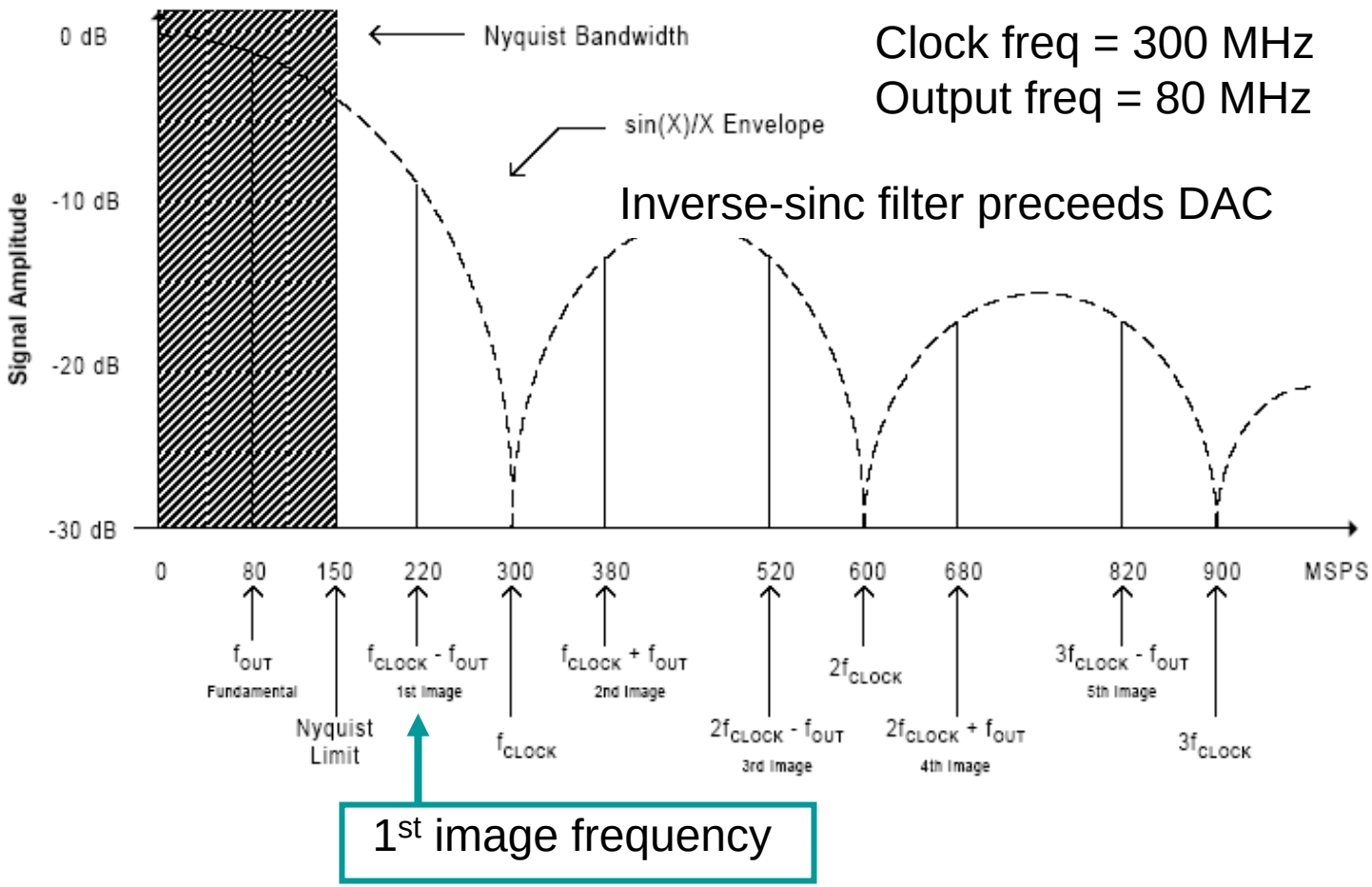
# Signal Flow

Signal power/quantization noise
= 1.76 + 6.02N




Ref: Analog Devices DDS Tutorial, 1999.


DAC RSET
300 MHz DDS
Digital Multiplier's
Diff/Single Select
Reference Clock In
4X - 20X Ref. Clock Multiplier
System Clock
Frequency Accumulator
Phase Accumulator
Phase Offset/ Modulation
Sine-to-Amplitude Converter
I
Q
Inverse Sinc Filter
Inverse Sinc Filter
MUX
12-Bit "I" DAC
12-Bit "Q"or Control DAC
Analog Out
Analog Out
FSK/BPSK/HOLD Data In
Frequency Tuning Word/Phase Word Multiplexer & Ramp Start Stop Logic
Ramp-up/Down Clock/Logic & Multiplexer
Output Ramp "Frame"
AD9854
48-bit Frequency Tuning Word
14-bit Phase Offset/ Modulation
12-bit AM MOD
12-bit Control DAC Data
Bi-directional I/O Update
PROGRAMMING REGISTERS
Analog In
Read
Write
I/O PORT BUFFERS
Programmable Rate and Update Clocks
Comparator
+
-
Clock Out
Serial/Parallel Select
6-bit Address or Serial Programming lines
8-bit Parallel Load
Master Reset
+Vs
Gnd




Analog low-pass anti-aliasing filter
Is needed at the output

Ref: Analog Devices DDS Tutorial, 1999.

Oversampling can be used to reduce the quantization noise

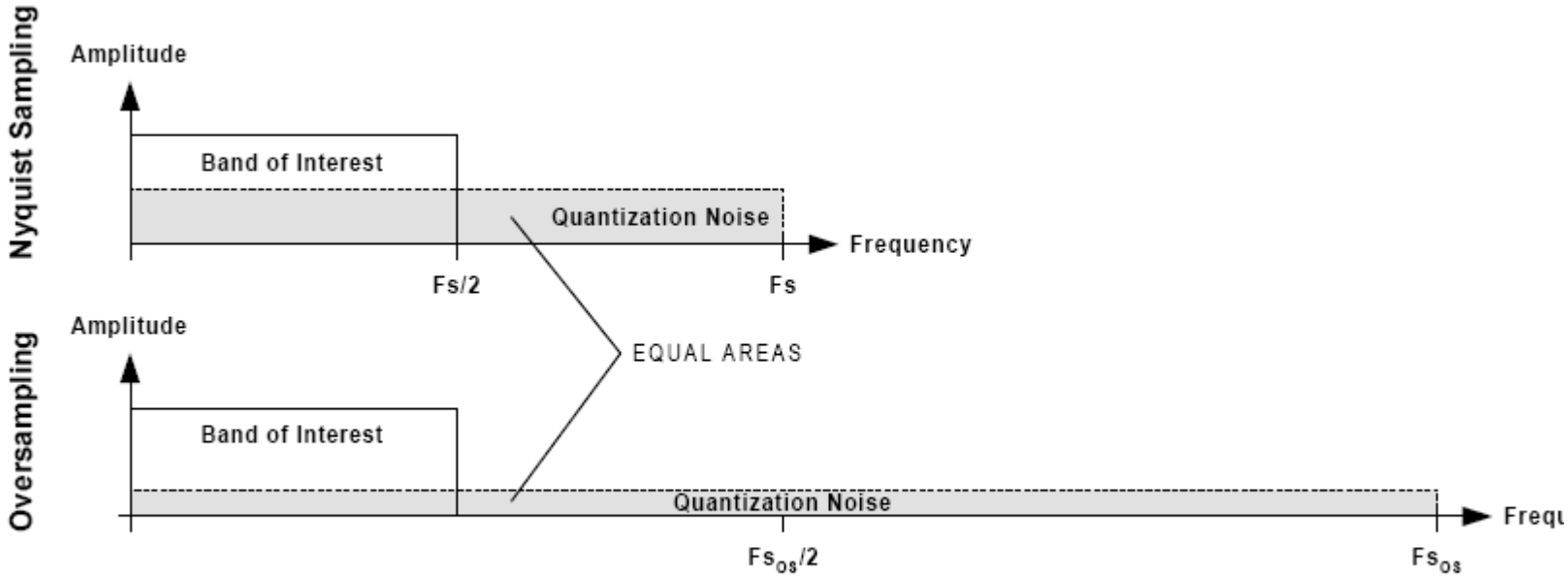
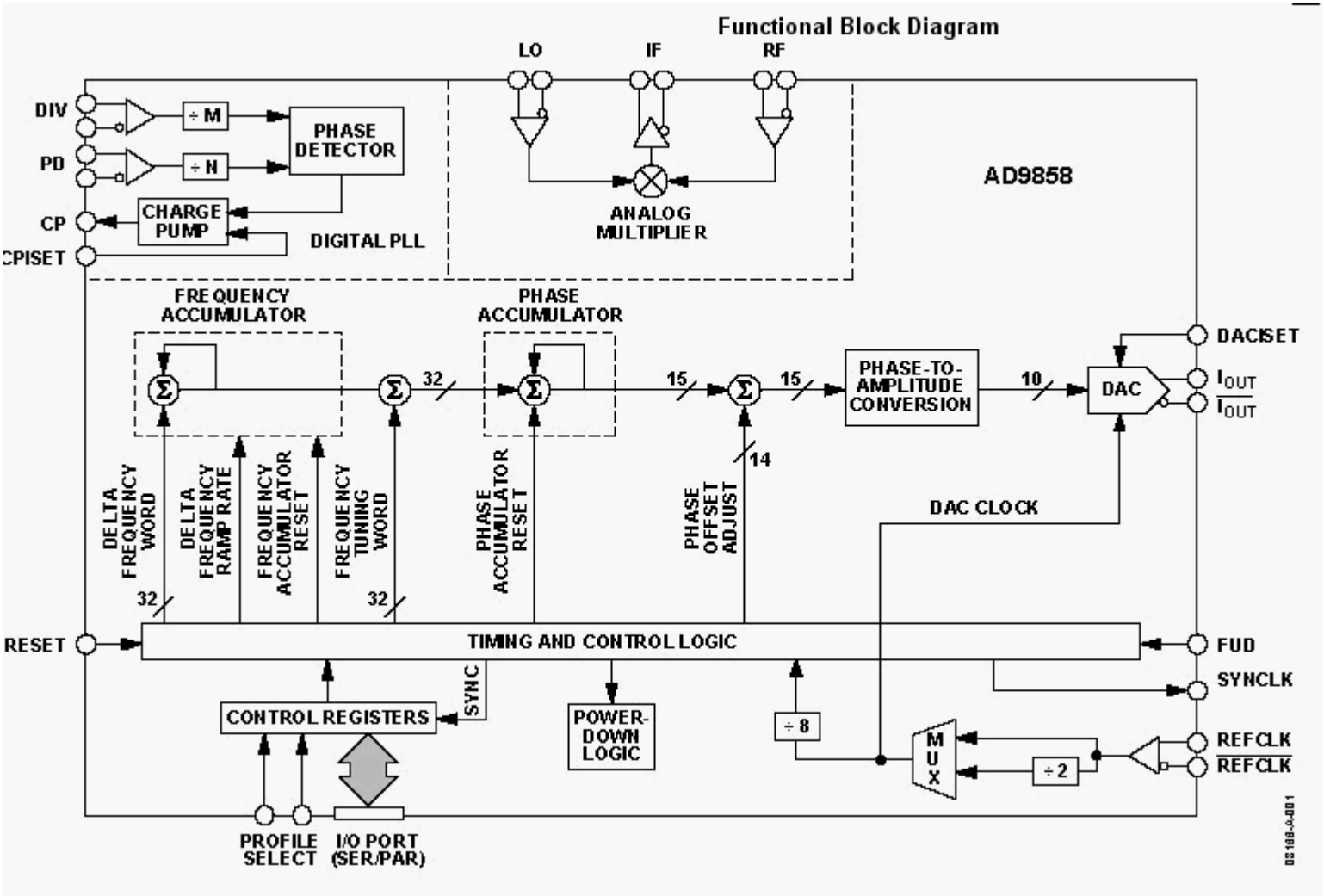



Figure 4.3. The Effect of Oversampling on SQR

$$10\log(F_{OS} / F_{Nyquist})$$

Ref: Analog Devices DDS Tutorial, 1999.

# AD9858 DDS




Clock freq = 1 GHz

Resolution: 10 bits

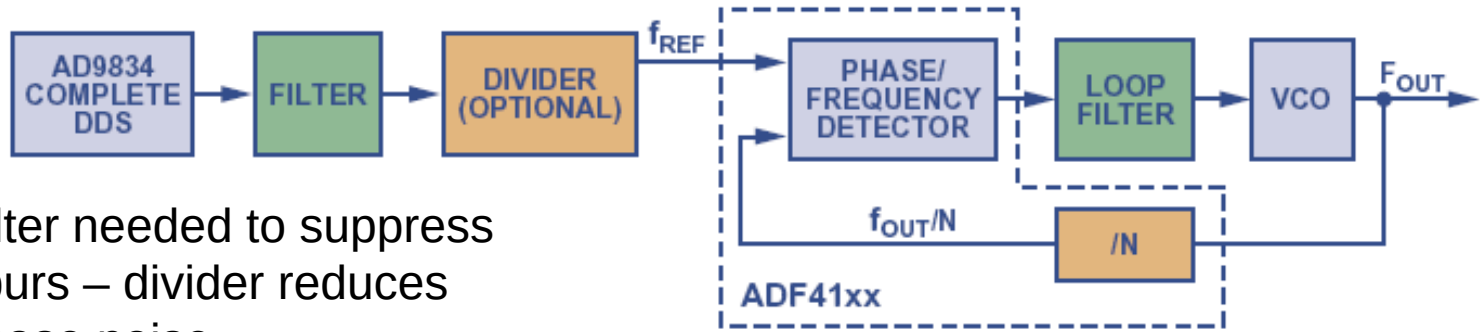
# Hybrid synthesizers

- Integer-N and DDS synthesizers can be combined for
  - better SNR
  - Finer tuning steps with wide loop BW
  - Higher reference frequency
  - Avoid complications of Fractional-N

Ex. $f_{REF}$ = 5 MHz; $F_{out}$ = 100 – 500 MHz; N = 20 – 100

each step is 5 MHz

But: $f_{REF}$ can be very finely adjusted to give frequencies between steps




Filter needed to suppress spurs – divider reduces phase noise

Figure 3. DDS as reference-frequency generator for a PLL.

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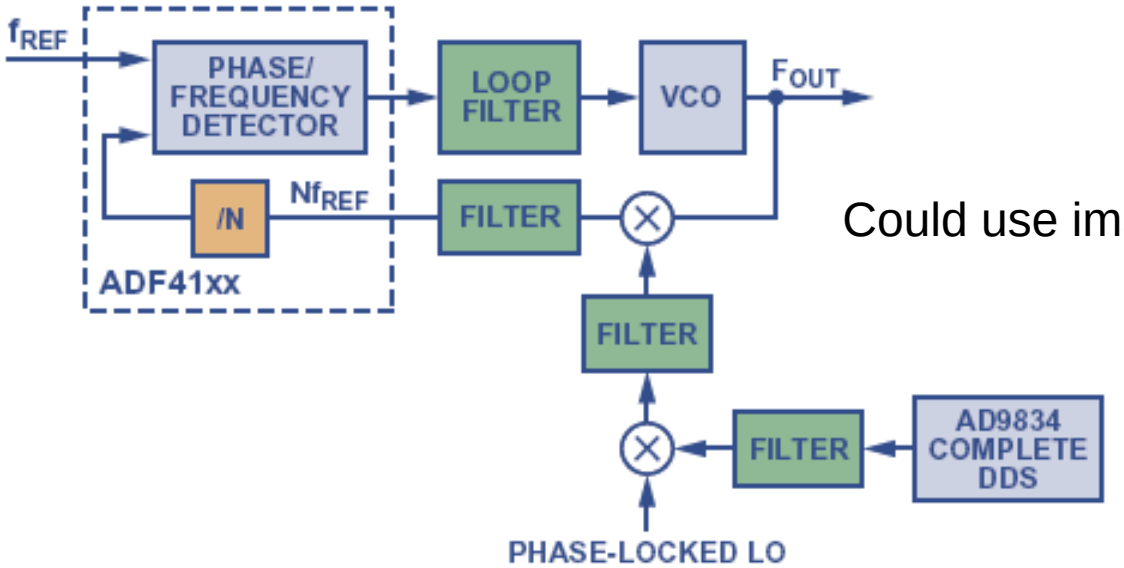
$$F_{OUT} = Nf_{REF} \pm (f_{LO} \pm f_{OFFSET})$$




Could use image-reject mixers

Figure 4. The AD9834 DDS generates the frequency offset for the ADF41xx PLL.

DDS provides small incremental frequency steps between each coarse step of the PLL.

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