VCO Design Project

ECE218B Winter 2011

Report due 2/18/2011

VCO DESIGN GOALS. Design, build, and test a voltage-controlled oscillator (VCO).

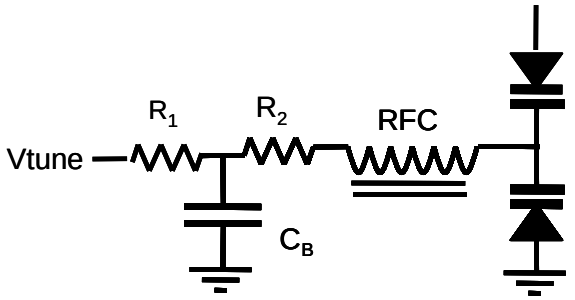
1. Design VCO for highest center frequency (< 400 MHz).
2. At least 10 MHz tuning range.

In addition, you need to observe the following specs:

Varactor tuning voltage range	1 to 5 volts
Supply voltage	+6 V
Output power	-3 to 0 dBm in 50 ohm load
Second and third harmonic	-25 dBc minimum

1. You will determine the oscillator type that you will design based upon achieving a center frequency as high as possible but below 400 MHz. You decide on either common gate/base or common drain/collector configuration. You can use either the J310 N-channel JFET or 2N5179 for the oscillator and the 2N5179 BJT for the buffer amp. Data sheets are on the course web page, and there are ADS models for these devices in the RF Transistor Library/Packaged BJTs (pb_mot_2N5179_19921211) and Analog Parts Library (ap_NJF_J310_19930601).

2. The electrical tuning of the oscillator will make use of the BB131 varactor diode. Connect two of these diodes back-to-back for improved harmonic distortion. Refer to the data sheet on the course web page**.** The varactor Q is typically 150 at 200 MHz and 5 volts reverse bias. You should avoid biasing the varactor under 1 volt reverse bias so that the Q remains high. Isolate the bias port with an RF choke, series resistor (to De-Q the choke), R_1 to isolate C_B from the tuning port, and bypass capacitor (choose value for series resonance at 135 MHz). The time constant of R_1C_B should be no larger than 10μS.



The varactor diode TC is shown on the data sheet – roughly +250 ppm/^{o}C. This is an unacceptably high TC for the entire resonator, however, the varactor provides only a small part of the total capacitance. You should implement the fixed capacitors in the resonator with zero TC (NP0) capacitors. The inductor core material has a TC of 0 ppm/^{o}C.

Chip inductors are not recommended for the resonator because their unloaded Q is quite low, on the order of 20 to 30 at 200 MHz, therefore you will fabricate wirewound inductors on toroidal core material. The inductance of the toroidal inductor can be estimated by the equation below; use an $A_L = 3$ for the type 0 material with 0.125 OD. Typical unloaded Q at 200 MHz is on the order of 100 and is better when turns are bunched together.

$$\#\,turns = 100\sqrt{\frac{L(\mu H)}{A_L\,(\mu H / 100\,turns)}}$$

Verify that your inductance is correct with the network analyzer to avoid needless frustration. The formula is only approximate.

A cylindrical wire coil can also be used, but will be sensitive to bending and position and will also have a temperature coefficient.

3. Do a detailed hand analysis of your oscillator, predicting startup conditions and the oscillation amplitude. Do not use high bias current for your oscillator – this is neither necessary nor desirable for good startup and stability and will increase power dissipation. Include the 5V voltage regulator to power your oscillator. The oscillator is intended to operate from a 6V battery, and you want the V_{CC} to remain constant as the battery voltage drops.

The hand analysis should be followed by ADS simulations before attempting to build the oscillator. A large-signal nonlinear analysis on the closed loop oscillator can be done by transient analysis or harmonic balance. Starting the oscillator in the transient simulator will require an impulse of current at the resonator since there is no naturally occurring noise to cause the oscillator to start. Harmonic Balance is the faster tool for oscillator simulations. Explore the bias current as a variable in the design. Make sure your design limits in cutoff (current limited) rather than saturation. Do a small-signal open loop AC analysis to find the loop gain vs. bias current.

Compare analysis with the measured result. (note that the simulation will be optimistic unless you include estimates for the PC board parasitic capacitances).

4. Tuning range. Predict tuning range with hand analysis. Then, build an ADS diode model from the information on the BB131 data sheet. Use this model for simulation of the VCO tuning range.

4. The output from your oscillator must be buffered in order to avoid pulling the oscillator frequency with variations in the load impedance and to drive a low load impedance. Use a 2N5179 BJT as a buffer stage to provide this isolation and to drive the 50Ω output. Either a CE or CC stage can be made to work. The oscillator output amplitude will most likely be too high, so a series resistance between the oscillator output and the buffer amp input can be used to reduce the voltage swing and improve harmonic distortion. Make sure your bias conditions are within the acceptable peak current and voltage of the device according to the data sheet on the web site. The final application

only requires -3 to 0 dBm (0.32V) into a 50 ohm load, so don't overdesign the buffer amplifier.

Design the buffer amplifier so that it will provide the required output drive power while using the least DC power.

You should perform a small signal stability analysis and modify the basic amplifier circuit to assure stable operation at the expected source and load impedances. Note that the amplifier need not be unconditionally stable, since you can control the Γ_S and Γ_L.

5. Implementation. You can use the generic VCO PCB to implement your oscillator. A plot of the board top layer is attached. It is recommended that you sketch on the plot which components are to be installed at each needed location. Note that some locations may remain empty depending on which configuration you choose. Solder down your components, keeping leads short, and build the oscillator. You will need to use both leaded and chip capacitors and resistors. Remember to use the NP0 caps for resonator components. Some layout examples can be found on the course website.

You will need some additional components beyond what is in the parts kit for implementation of your design. Prepare a parts list of what you will need beyond your parts kit, and take this to the electronics shop or check with the TA.

Include the hand analysis, the ADS simulations, and well-documented final design in your report.

The following measurements should be made and documented in the report:
You can check out a wideband 10X probe from the TA for oscilloscope measurements.

1. Electrical tuning range Plot frequency vs. Vtune. Use a frequency counter for this measurement for more accuracy. Determine Kv = $\Delta f/\Delta V$tune by measurement of Δf for a small ΔVtune at the low, middle, and high ends of the tuning range.

2. Measure RF Output power and DC input power

3. Output spectrum:

   A. Harmonics. Use the spectrum analyzer to determine the amplitude of each harmonic. Be careful to set the attenuation to avoid overloading the analyzer. If the 2nd and 3rd harmonics are strong (<20 dBc) your oscillator is probably voltage limiting instead of current limiting and the biasing should be changed to improve harmonic suppression. Use the oscilloscope to determine the limiting mode. Or, the buffer amplifier may be overdriven. Add more resistance in series between the oscillator and the base connection to the buffer amp.

   B. Sidebands. These might be caused by parasitic oscillations or the "squegging" effect. They are usually caused by improper bias circuit design that allows a low frequency feedback path to cause a spurious oscillation. You need to get rid of them through proper bypassing and isolation methods. You will only be able to

see them by using a narrow resolution bandwidth on the spectrum analyzer. You must show that you have checked your oscillator for sidebands at an appropriate setting.

C. Spurious outputs (UHF oscillations). Measure the amplitude and frequency of any non-harmonically related output and try to identify its source and eliminate it.

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Parts Kit (To obtain additional leaded components, prepare a parts list for the shop.)

2	2N5179
1	J310 JFET
2	BB131 Varactor diode (SOT-23 package)
1	LM2931Z-5.0 voltage regulator
4	1 uH leaded inductor (RFC)
1	100 uF/25V radial electrolytic capacitor (for LOW freq. VDD Bypass)
1	0.1 uF ceramic leaded cap
1	T-12-0 (tan) powdered iron core (for resonator) (For data on this core material see the web site for the class)
1	Generic VCO PC board
1	board mounted SMA female connector (for output)
2'	#30 enameled wire
2	2 ft. twisted pair of insulated wire (for tuning port input and for power supply connection)

Model parameters for the BB131 Varactor Diode.

ADS uses the SPICE diode model. This model uses the equation below to describe the capacitance of a reverse-biased pn junction diode:

$$C(V)=CJO\left(1-\frac{V}{VJ}\right)^{-M}$$

CJO = Diode capacitance at V = 0
VJ = built-in voltage of diode (default value 0.8V)
M = grading coefficient. (typically 0.5 for abrupt junction)
CJO, VJ, and M can be determined by fitting the given capacitance voltage characteristic to this equation.

The diode equivalent circuit also includes a series resistance Rs due to the resistance of the semiconductor material and contacts. The varactor data sheet specifies this either through the unloaded Q defined as

$$Q=\frac{reactance}{resistance}=\frac{1}{\omega CR_S}$$ at frequency ω and at a specific reverse bias voltage,

or states Rs specifically.

Temperature Compensation of Resonant Circuits

Oscillators are frequently used to set the transmit or receive frequency in a communication system. While many applications use a phase locked loop technique to correct for frequency drift, it is good practice to build oscillators with some attempt to minimize such drift by selecting appropriate components.

Inductors and capacitors often drift in value with temperature. Permeability of core materials or thermal expansion of wire causes inductance drift. Variations in dielectric constant with temperature in capacitors is the main source of drift for these components.

Temperature drift is expressed as a temperature coefficient in ppm/^{o}C or %/temp range.

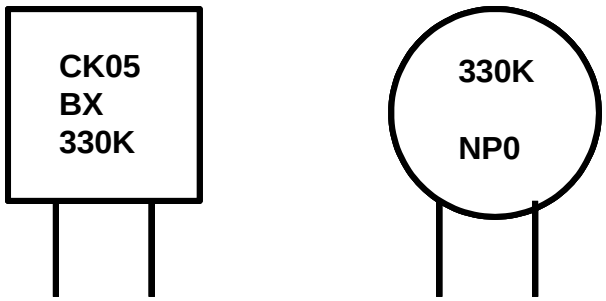
Capacitors

The 3 most common types of dielectrics for RF capacitors are:

Dielectric type	Temp coefficient (TC)	Temp range
C0G (or NP0)	+/- 30 ppm/^{o}C	-55 to +125C
X7R (BX)	- 1667 (+15% to -15%)	-55 to +125
Z5U	- 10^{4} (+22% to -56%)	10 to 85

Clearly, the Z5U is not much good for a tuned circuit and should be used for bypass and AC coupling (DC block) applications where the value is not extremely critical. At lower radio frequencies, polystyrene capacitors can be used. These have a – 150 ppm/C TC.

The C0G and X7R can be used in tuned circuits if their values are selected to compensate for the inductor drift.



The two leaded capacitors above illustrate the labels found on typical capacitors of the X7R and NP0 types. The value is given by the numerals: 330. In this example, this is 33 pF. It goes 1st significant digit (3), 2nd significant digit (3), and multiplier (10^{0}). The letter K is the tolerance, which is +/- 10%.

As always, the parasitic inductance and self resonance of any capacitor must be considered for RF applications.

Inductors

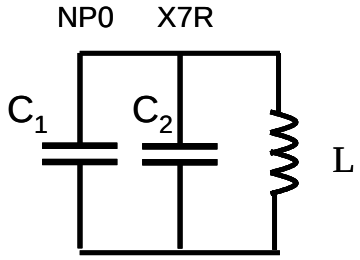
There are many types of inductor core materials which are intended for different frequency ranges, permeability, and TC. Powdered Iron and Ferrites are the two categories of these materials.

For example, the material you will have available for the VCO lab is powdered iron. Type 12 (green/white) is useful from 50 to 200 MHz and gives Qu in the 100 – 150 range. $\mu/\mu_0 = 4$. Manufacturer's data sheets can be found on the web (www.amadoncorp.com) that specify TCs for the many materials. This one has a weird TC vs temperature behavior, but we are mainly interested in the 25 to 50C range for this project.

Temperature range	TC
25 – 50C	+50 ppm/C
50 – 75	- 50
75 – 125	+ 150

The type 0 toroids (tan) have smaller AL values and temperature coefficient. Better Q above 200 MHz.

So, how can you compensate for component drift?



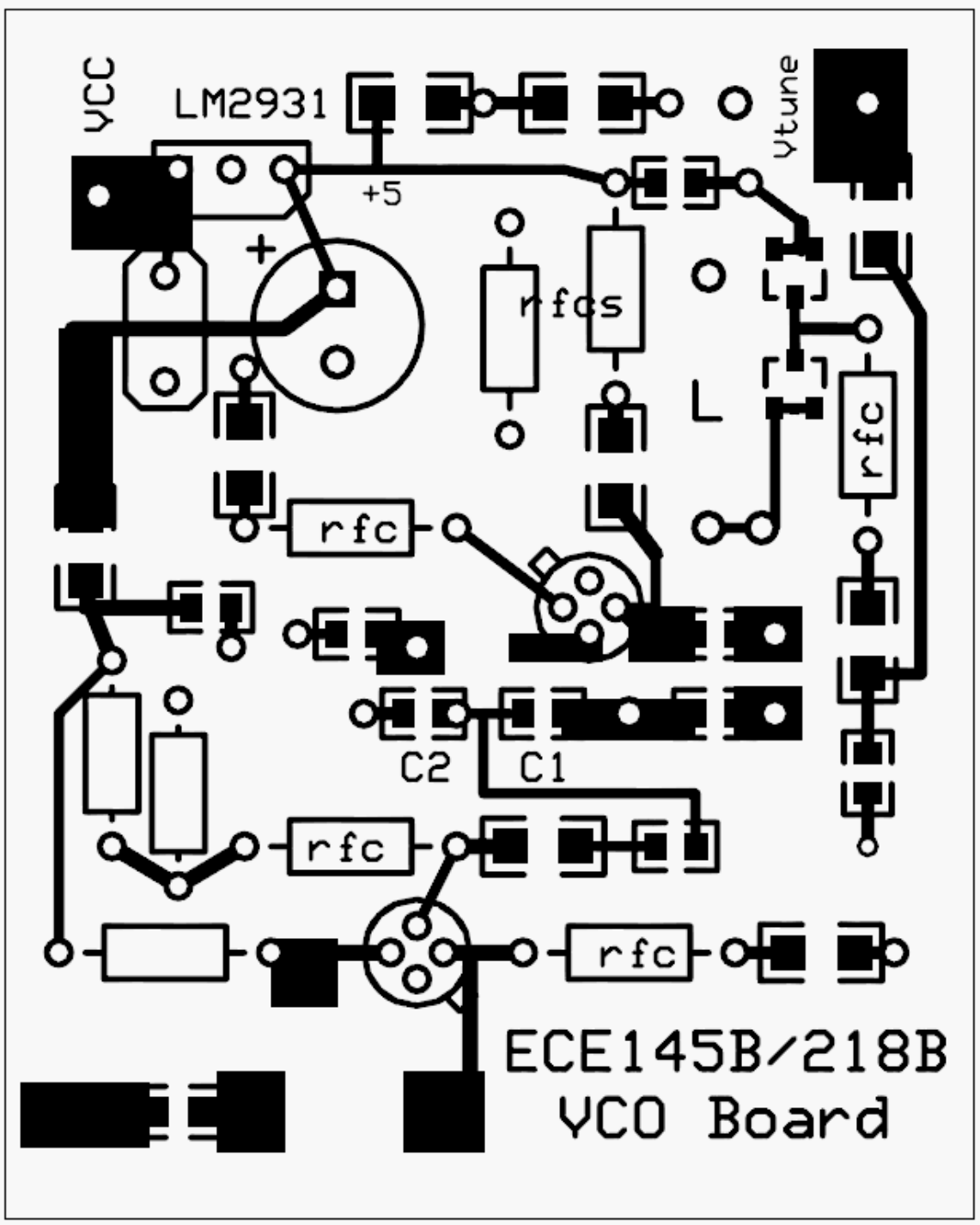
The equation below shows how the TCs of individual components combine[1]. Suppose that the inductor was resonated with a drift free capacitor (NP0). The frequency drift will be – 25 ppm/C. If the design frequency is 100 MHz, this corresponds to a drift of 2.5 kHz/C. But, the equation shows that you can set the total frequency TC (TCF) of a circuit to zero by combining capacitors with different TCs.

$$TCF = \frac{\Delta f}{f_0} = -\frac{1}{2}\left(TC_L + TC_{C1}\frac{C1}{C_{TOTAL}} + TC_{C2}\frac{C2}{C_{TOTAL}} \right)$$

Thus, if the inductor has a positive TC, you can correct for temperature drift with the right combination of non drift and drifty capacitors. In this case, we want the total

[1] W. Hayward, R. Campbell, and B. Larkin, Experimental Methods and RF Design, ARRL Press, 2003.

capacitance of C1 and C2 to have a net TC of – 50 ppm/C. The best oscillators will be designed with components with low intrinsic TCs so that you do not have to compensate them with different components having large and possibly unreliable TCs.


VCC
LM2931
+5
Vtune
rfcs
rfc
rfc
rfc
rfc
C2
C1
ECE145B/218B
VCO Board