

PA notes #3: Higher Efficiency Power Amplifiers

Efficiency limitations --

Class A: at best 50%
 at worst 0%

For really high power or battery applications, Class A efficiency is not good enough.

How do we improve this? Reduce the conduction angle.

The conduction angle is the portion of the RF cycle in which the device is conducting (ie. Not in cutoff).

How?

Change the bias condition from fully on (class A) to partially in cutoff.

Class B: Device is biased right at cutoff.

Consequences:

1. P_{DC} is reduced for same P_{out}
2. Harmonic termination is now required
3. RF drive signal drives device into conduction
4. More drive is required for Class B than Class A

(typically, 6 dB of gain is lost since the input voltage and current swing must be doubled).

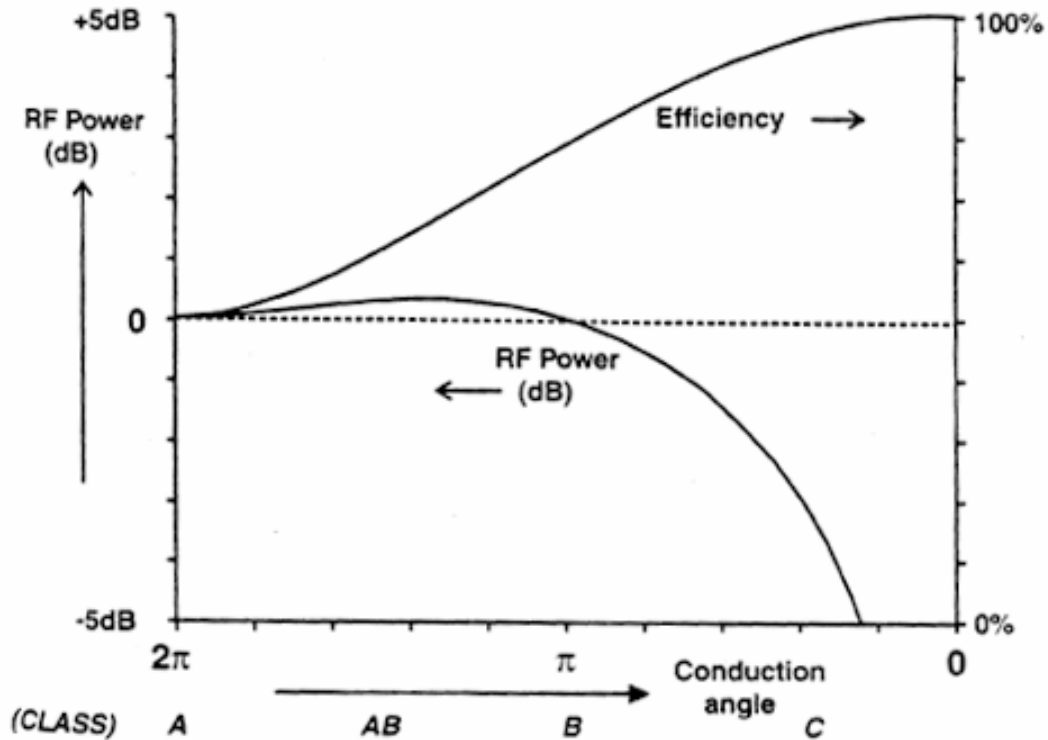


Figure 3.4 RF power and efficiency as a function of conduction angle; optimum load and harmonic short assumed.

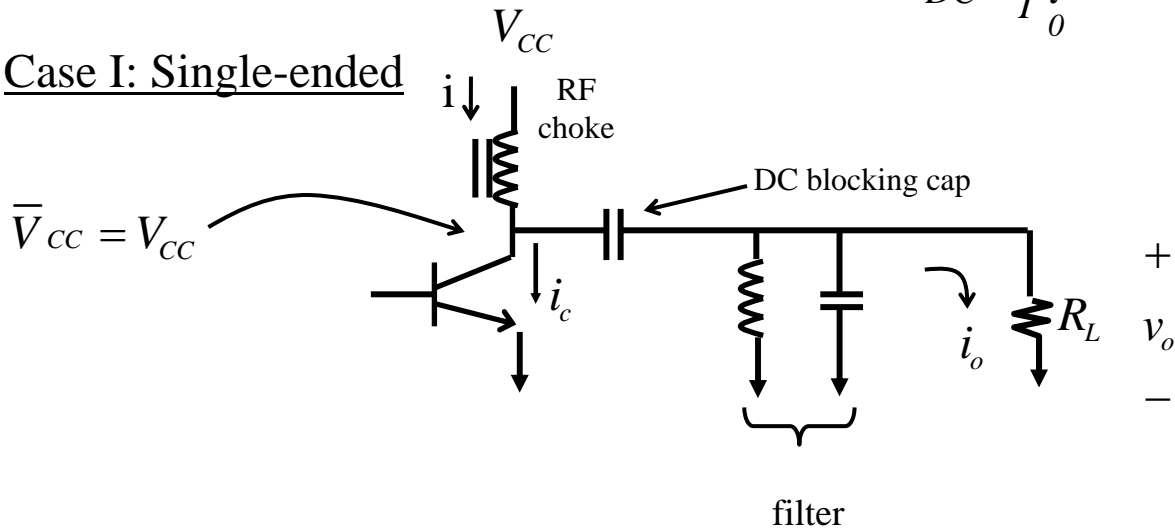
Ref. S. Cripps, RF Power Amplifiers for Wireless Communications, Artech House, 1999.
Preliminary Observations

1. P_{OUT} roughly the same between Class A and B
2. Class B reduces P_{DC} by factor of $\frac{\pi}{2}$
3. Class C provides rapidly increasing efficiency, but rapidly decreasing P_{OUT}

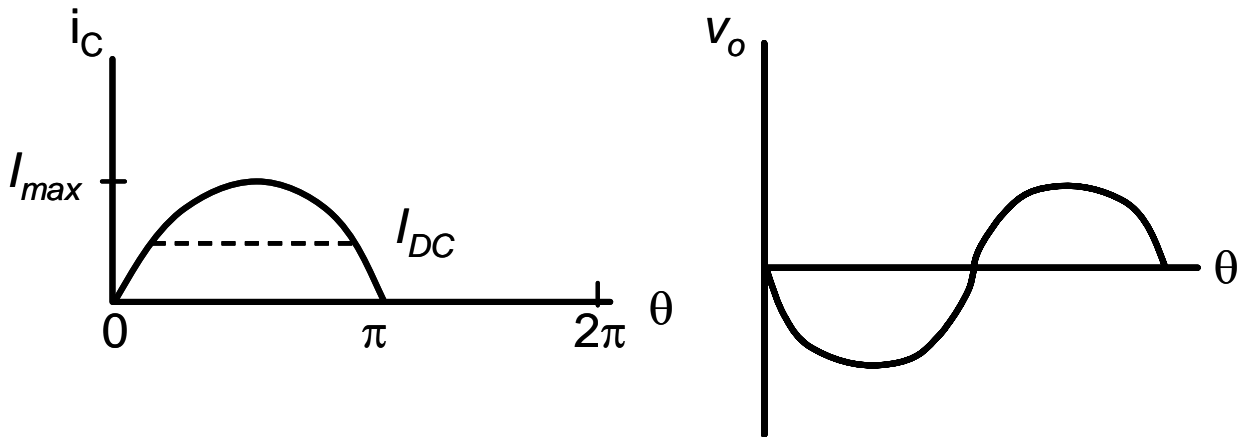
Class B Device biased at cutoff

$$i = i_o + i_c \quad I_{DC} = \frac{1}{T} \int_0^T i dt$$

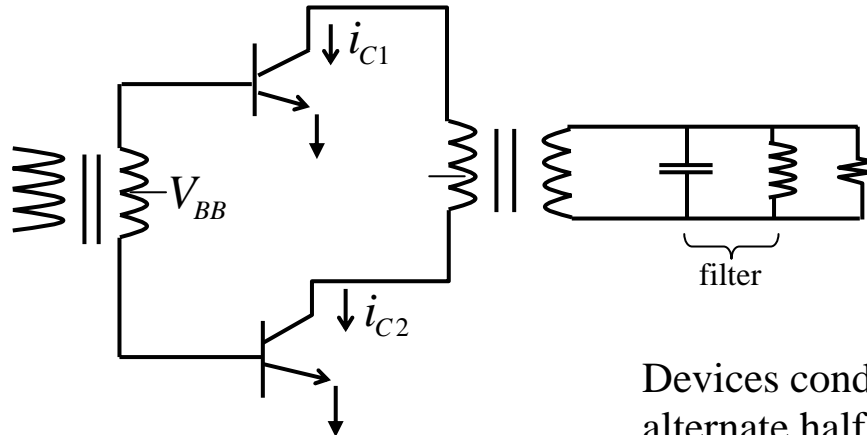
Case I: Single-ended



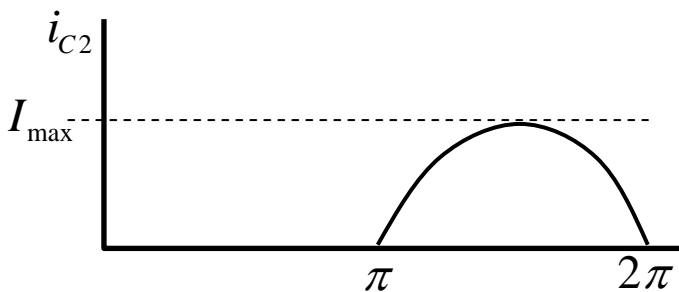
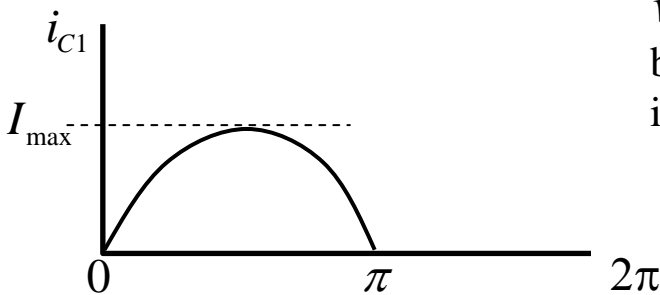
i_o = amplitude of fundamental component of i_c . The LC resonator shorts harmonics. Only the fundamental component of the current can appear at the load resistor. The collector current is a half sinusoid because the device conducts only 50% of the time.



Case II: Push-Pull



Devices conduct on alternate half cycle to provide fully sinusoidal v_o . A transformer or balun is needed at the input and output.

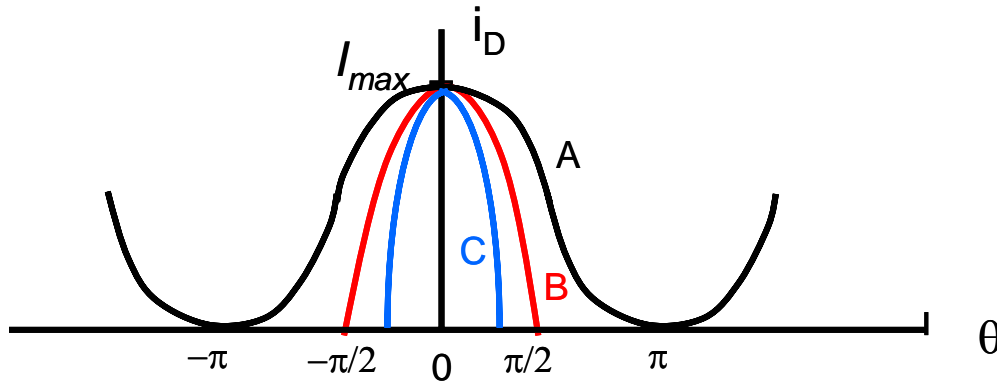


Push-pull is all about balun design. Transmission line baluns can be made to work well at 500 MHz and below. PC board balun structures are physically large. Unless a balanced amplifier is really necessary (for bandwidths an octave or greater, for example), there is no need to incur this added complication. The single ended class B works fine.

Class B. Case I.

Base bias level is adjusted so that the conduction angle = π (50% duty cycle)

Now, drain current is a half cosine function. We will discuss Class C later.



$$i_c(\theta) = I_{\max} \cos \theta \quad -\frac{\pi}{2} \leq \theta \leq \frac{\pi}{2}$$

$$= 0 \quad \left\{ \begin{array}{l} \frac{\pi}{2} < \theta < \pi \\ -\frac{\pi}{2} > \theta \geq -\pi \end{array} \right.$$

Since current is not a complete sine wave, we must calculate DC power and AC fundamental and harmonics from Fourier components.

$$i_D(\theta) = a_0 + a_1 \cos \theta + a_2 \cos 2\theta + a_3 \cos 3\theta + \dots$$

=0 by even function

$$a_0 = \frac{1}{2\pi} \int_{-\pi/2}^{\pi/2} I_{max} \cos \theta d\theta = \frac{I_{max}}{2\pi} \underbrace{\left[\sin \frac{\pi}{2} - \sin \left(-\frac{\pi}{2} \right) \right]}_2$$

$$= \frac{I_{max}}{\pi} = I_{dc}$$

$$a_1 = \frac{1}{\pi} \int_{-\pi/2}^{\pi/2} I_{max} \cos^2 \theta d\theta = \frac{I_{max}}{\pi} \left[\frac{\theta}{2} \right]_{-\pi/2}^{\pi/2} = \frac{I_{max}}{2} = I_1$$

I_1 is the fundamental current component. $V_1 = I_1 R_L$

$$\begin{aligned} a_2 &= \frac{I_{max}}{\pi} \int_{-\pi/2}^{\pi/2} \cos \theta \cos 2\theta d\theta = \frac{I_{max}}{2\pi} \int_{-\pi/2}^{\pi/2} [\cos 3\theta + \cos \theta] d\theta \\ &= \frac{I_{max}}{2\pi} \sin \theta \Big|_{-\pi/2}^{\pi/2} + \frac{I_{max}}{6\pi} \sin 3\theta \Big|_{-\pi/2}^{\pi/2} = \frac{I_{max}}{\pi} - \frac{I_{max}}{3\pi} \\ &= \frac{2I_{max}}{3\pi} = I_2 \end{aligned}$$

I_2 is the second harmonic current. Higher harmonics can be calculated in the same way.

$$\begin{aligned}
 a_3 &= \frac{I_{max}}{\pi} \int_{-\pi/2}^{\pi/2} \cos \theta \cos 3\theta d\theta = \frac{I_{max}}{2\pi} \int [\cos 4\theta + \cos 2\theta] d\theta \\
 &= \frac{I_{max}}{8\pi} \sin 4\theta \Big|_{-\pi/2}^{\pi/2} + \frac{I_{max}}{4\pi} \sin 2\theta \Big|_{-\pi/2}^{\pi/2} = 0
 \end{aligned}$$

ω odd terms = 0

ω even terms finite, but shorted by LC resonator.

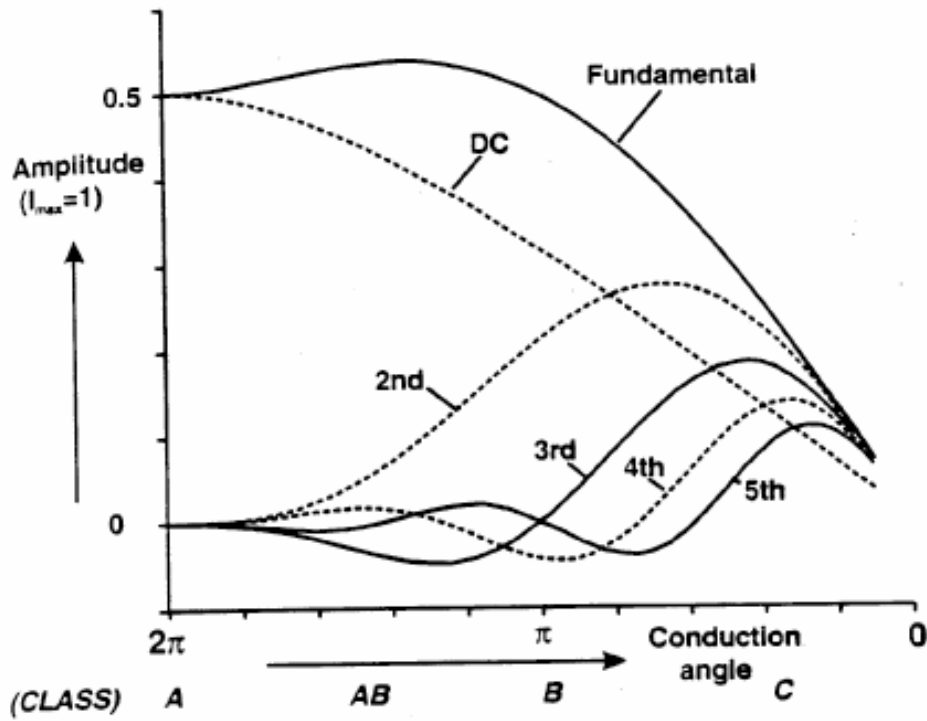
Thus, the total current, $I_{max} \cong I_{dc} + I_1 + I_2 + I_4 + \dots$

This must be equal to the peak current that the device is capable of providing. Choose the device accordingly.

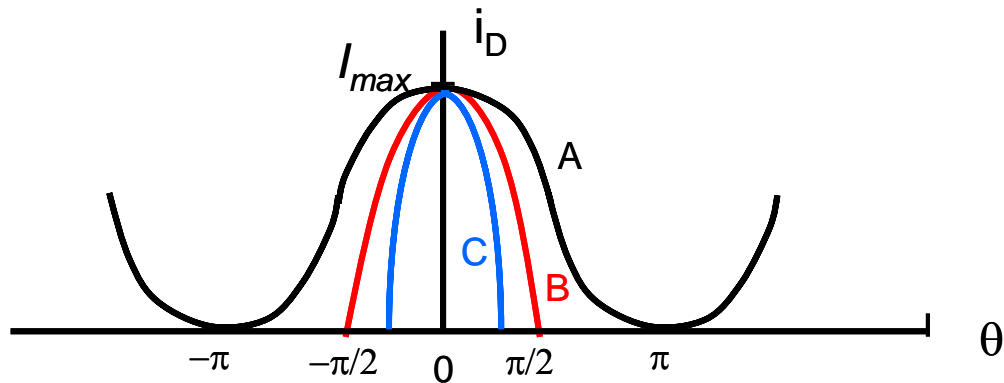
The current that actually is delivered to the load is the fundamental

frequency component, $I_1 = \frac{I_{max}}{2}$. This is the current that must be used to determine the optimum load resistance.

The figure below shows the amplitudes of the fundamental and harmonic currents (relative to an $I_{max} = 1$) as a function of the conduction angle.



From: S. Cripps, RF Power Amplifiers for Wireless Communications, Artech House 1999.



Class C reduces the conduction angle even more. PDC and Pout are both reduced. Efficiency approaches 100% as Pout approaches 0! Large harmonic currents are required. Not a very effective means of increasing efficiency.

Choosing load resistance: The best load resistance is the large signal load resistance that allows full voltage and current swing at the device collector or drain. To get the full voltage swing across R_L , $V_O = V_{DC}$, (neglecting knee voltage V_K)

we must choose
$$R_L = \frac{V_{DC}}{I_1} = \frac{2V_{DC}}{I_{max}}$$

Or, when V_K is considered,

$$R_L = \frac{V_{DC} - V_K}{I_1} = \frac{2(V_{DC} - V_K)}{I_{max}}$$

I_2 (and higher harmonics of the current) are assumed to be shorted by the LC resonator or bias network.

Note that this load resistance is the same as was optimum for class A.

Now, the output power, DC power and efficiency can be calculated for Class B. Recall that $I_1 = I_{max}/2$.

$$P_O = \frac{1}{2} I_1^2 R_L = \frac{I_{max}^2 R_L}{8} = \frac{1}{2} \frac{V_{DC}^2}{R_L}$$

$$P_{DC} = \frac{I_{max} V_{DC}}{\pi} = \frac{2V_{DC}^2}{\pi R_L}$$

$$\eta = \frac{P_O}{P_{DC}} = \frac{V_{DC}^2 / 2R_L}{2V_{DC}^2 / \pi R_L} = \frac{\pi}{4} \quad (79\%)$$

The efficiency is much greater than Class A: 79% vs 50%

Harmonic Termination

We have seen that I_c has a strong second harmonic current amplitude

$$I_2 = \frac{2I_{\max}}{3\pi} = 0.21I_{\max}$$

all I_n for $n = \text{even}$ are present

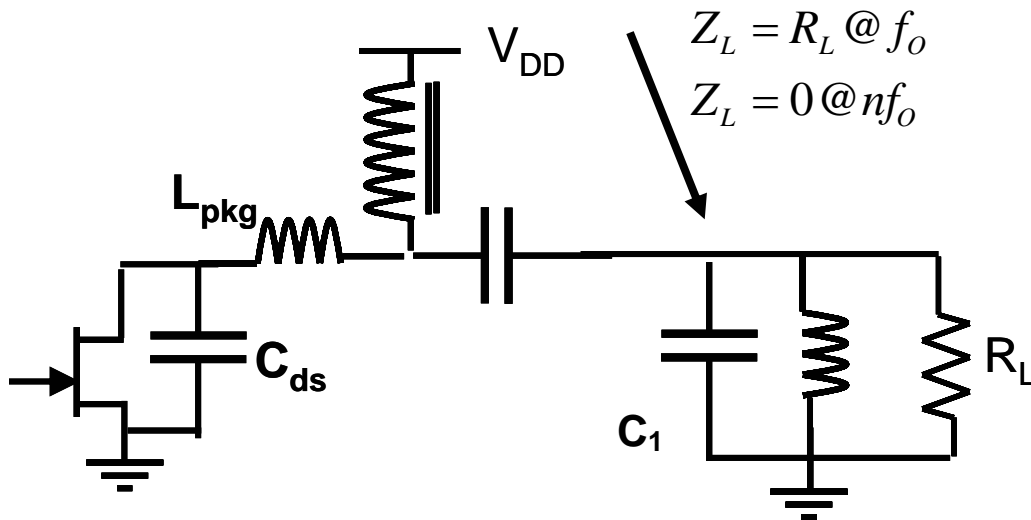
all $I_{n+1} = 0$ for odd harmonics

How do we provide the even harmonic short?

To get half sinusoidal current, at least I_2 must be shorted.

1. RFC DC feed:

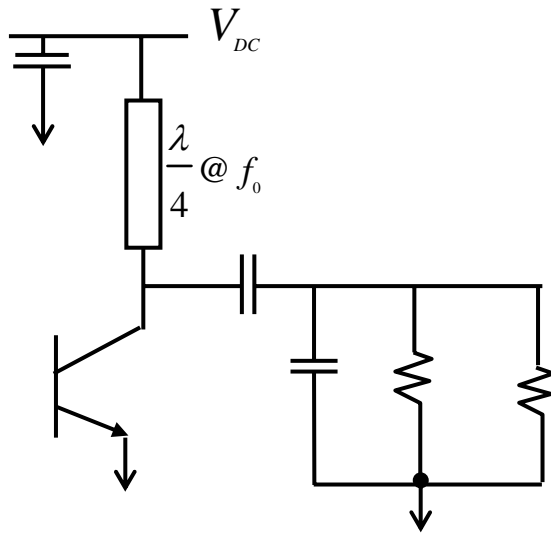
$$\text{high } Q_L = \frac{\omega C_1}{G_L}$$



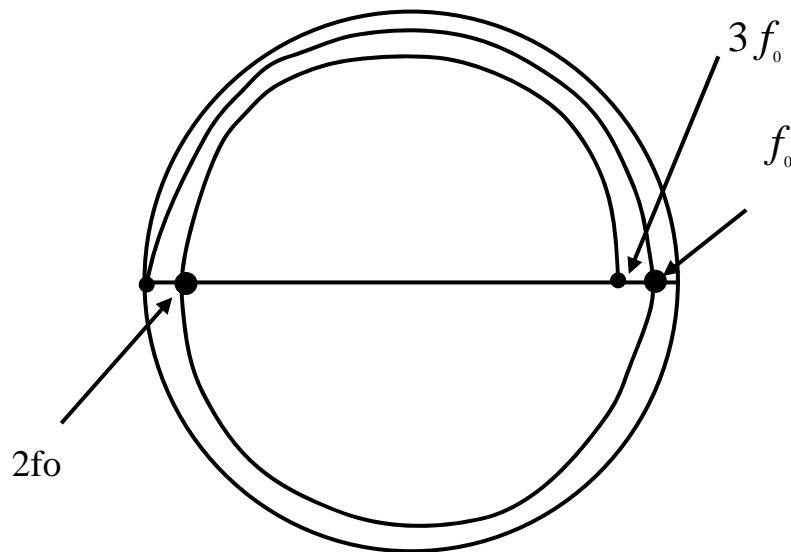
If C_{ds} is large, the harmonic short happens by default at device.

If L_{pkg} is small, C_1 can provide the termination at $2f_o$, $4f_o$.

2. At higher frequencies with low parasitic packages or no package, $\frac{\lambda}{4} @ f_0$ line works well.



Quarter-wave line:

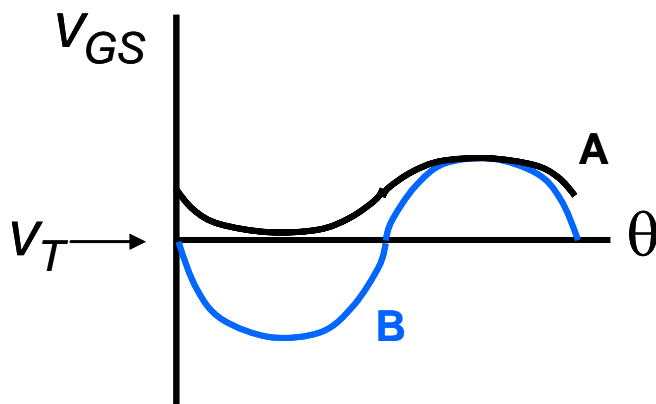
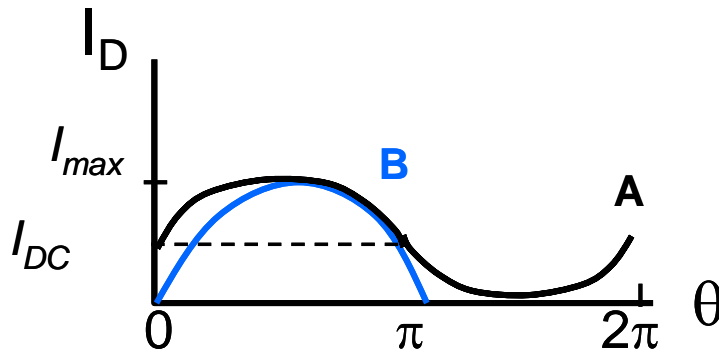


Are there costs to using reduced conduction angle?

1. Input Drive.

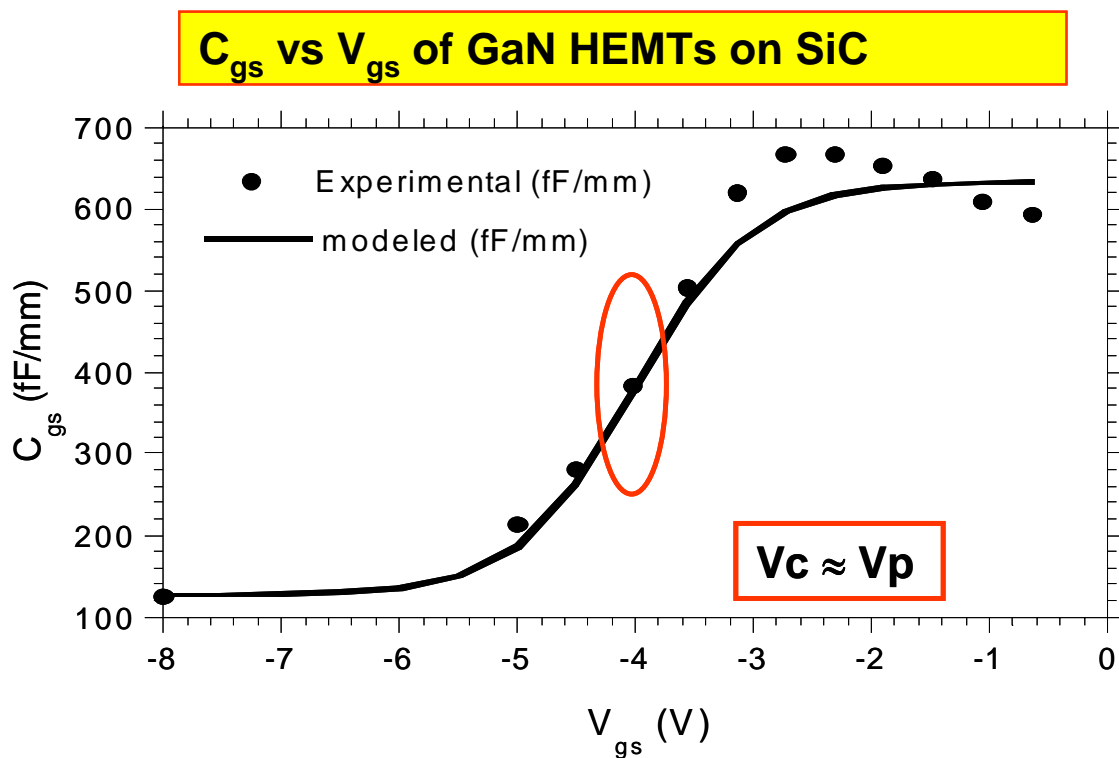
We must still achieve the I_{max} of the device to maintain peak current. For a MOSFET or HEMT in class B, this requires that the gate voltage swing is double that of Class A because the negative swing must go below cutoff for half of the period. This requires a 6 dB increase in drive power – a problem for maintaining PAE unless the device has very high f_{max} .

Not as severe with BJT or HBT because of the nonlinear base voltage collector current relationship.

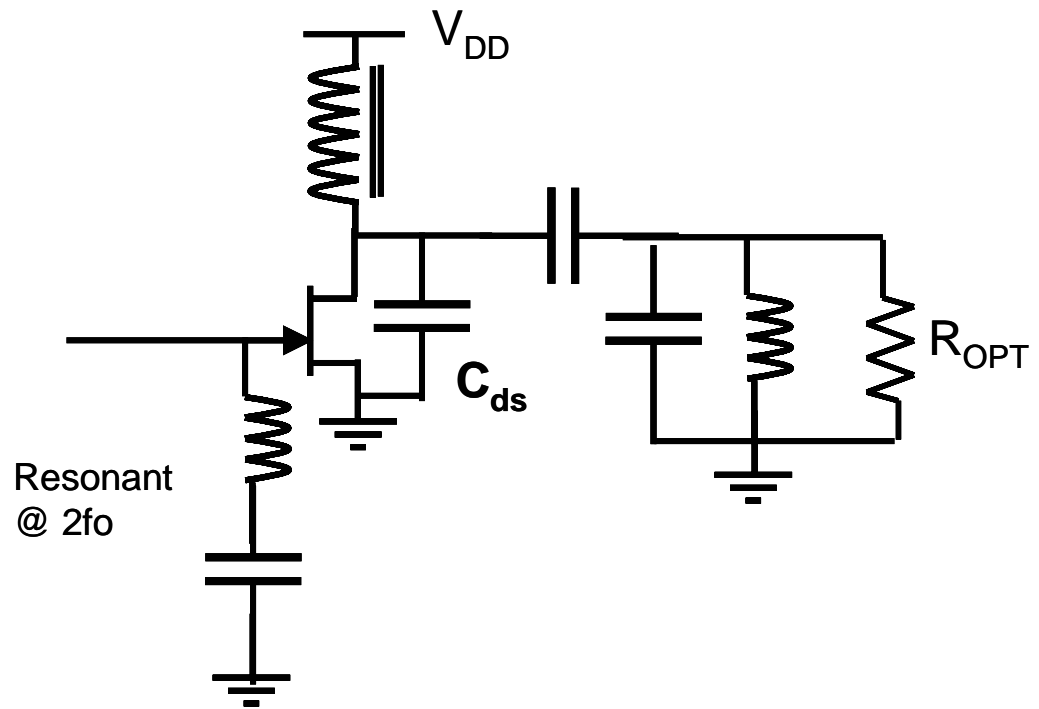


2. Nonlinear gate capacitance.

The gate capacitance of all FETs can be quite nonlinear. Specifically, it drops very fast as the device is biased below threshold into cutoff. Then, if the drive current from the source remains roughly constant, the voltage swing on the gate in the negative direction can be much larger than in the positive direction. This is detrimental to breakdown because the maximum drain voltage occurs at the same time that the gate voltage is at minimum. Thus, V_{dg} is increased. It also produces a strong even harmonic voltage on the gate.



An even harmonic trap has been found to be effective in reducing the impact of these factors. By shorting the even harmonic voltage, the gate voltage can remain either sinusoidal or if some odd harmonics are possible, can even become slightly square. [1]



Other costs:

3. Peak drain current is increased.
4. Difficult to realize a wideband even harmonic short circuit.

[1] P. M. White, "Effect of input harmonic termination on high efficiency Class B and Class F operation of PHEMT devices," Proc. IEEE Intl. Microwave Symp., 1998, paper THIF-05.

Power Output Capability

Before going on, we need to introduce another metric for PA performance, the power output capability, or POC. Recall that efficiency increases as conduction angle is reduced. This benefits the thermal problem of removing dissipated heat, but can also affect how much voltage and current stress the device experiences.

Since devices are expensive, we want to get as much output power as we can from the maximum voltage and current that the device can provide. Hence, POC is defined to compare maximum output power with maximum voltage and current on the device.

$$POC = \frac{P_{OUT}}{V_{D,max} I_{D,max}}$$

We find for the linear operating classes that there is very little difference. Class AB is slightly better because output power can increase by up to 0.5 dB over Class A or B. However, we see Class C is a disaster. Too little power output for the stress on the device.

| Class | Conduction angle | Maximum drain efficiency | Power output capability |
|--------------------------|-------------------------|---------------------------------|--------------------------------|
| A | 2π | <50% | 1/8 |
| AB | $\pi < \theta < 2\pi$ | 50 – 75% | ~ 1/8 |
| B | π | < 79% | 1/8 |
| C (nonlinear) | $< \pi$ | < 100% | << 1/8 |

Path to higher efficiency

OK. So, class B can give us up to 79%. Can we do any better?

Not with a linear amplifier. Classes A, AB, B are fairly linear if properly designed. We saw that Class C does not use the device power output capability effectively plus it is highly nonlinear.

To achieve better efficiency than Class B, we must intentionally overdrive the input to drive output power into saturation. This, with the correct harmonic tuning, can produce efficiencies well above 79% but at the cost of linearity.

Class F. What if we could produce a square wave voltage at the collector or drain?

$$V_1 = \frac{1}{\pi} \int 2V_{DC} \cos \theta d\theta = \frac{2V_{DC}}{\pi} [\sin(\pi/2) - \sin(-\pi/2)] = \frac{4}{\pi} V_{DC}$$

or $1.28 V_{DC}$ as opposed to V_{DC} for Class B.

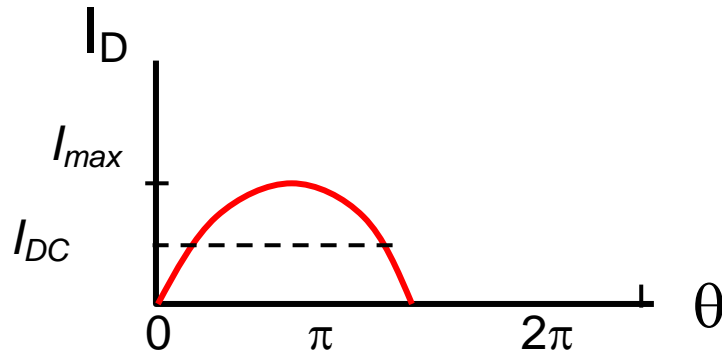
This gives us a large increase in fundamental output power for the same V_{DC} and I_{DC} .

$$I_1 = \frac{I_{\max}}{2} \quad I_{DC} = \frac{I_{\max}}{\pi}$$

$$P_{out} = \frac{1}{2} V_1 I_1 = \frac{1}{2} \left(\frac{4V_{DC}}{\pi} \right) \left(\frac{I_{\max}}{2} \right) = \frac{V_{DC} I_{\max}}{\pi} = V_{DC} I_{DC}$$

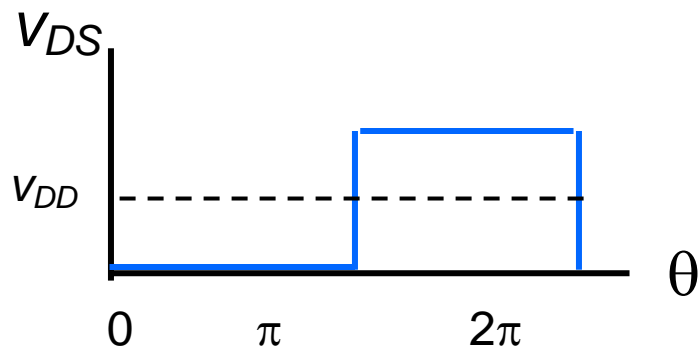
So, $P_{out} = P_{DC}$! 100% efficiency.

Then all we need to do is produce an ideal square wave voltage.
How?



$$I_{DC} = \frac{I_{\max}}{\pi}$$

$$I_1 = \frac{I_{\max}}{2}$$



$$V_{D,\max} = 2V_{DD}$$

$$V_1 = \frac{4V_{DD}}{\pi}$$

Class F current and voltage

Unfortunately, ideal square wave voltage and half sine wave current can't be done. We would need all odd harmonics in voltage and all even harmonics in current. But, this requires infinite bandwidth to produce all harmonics, and all devices have an upper frequency limitation, f_{\max} . Also, we have neglected knee voltage.

But, we can apply a finite number of harmonics. We can show that each harmonic, properly applied, increases the efficiency toward 100%.

| Class F Harmonics | 1 (class A) | 2 | 3 | 4 | 5 |
|---------------------------------|--------------------|----------|----------|----------|----------|
| Ideal drain efficiency % | 50 | 71 | 82 | 87 | 91 |
| Power output capability | 0.125 | | 0.144 | | 0.151 |

So, retain the even harmonic short as in Class B, but open circuit as many odd harmonics as possible. Overdrive the amplifier to clip the voltage so that we approach a square wave.

Consider only third harmonic:

$$V_D(\theta) = V_1 \cos \theta - V_3 \cos 3\theta$$

If $V_3/V_1 < 1/9$, the voltage waveform has a single peak. At $1/9$,

$$V_{\text{peak}} = V_1 - V_3 = 8V_1/9$$

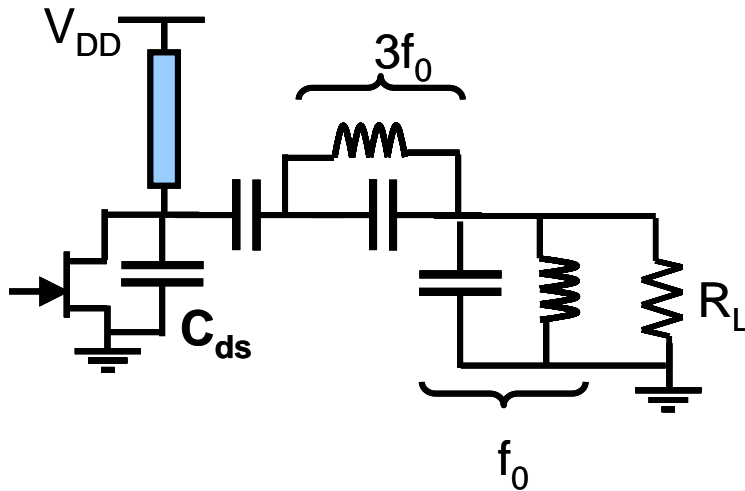
The reduction in peak voltage allows us to increase V_1 by increasing R_L .

In general, we can increase the fundamental voltage from $V_1 = V_{\text{max}}$ (Class B) to a higher value, $V_1 = V_{\text{max}}/\kappa$

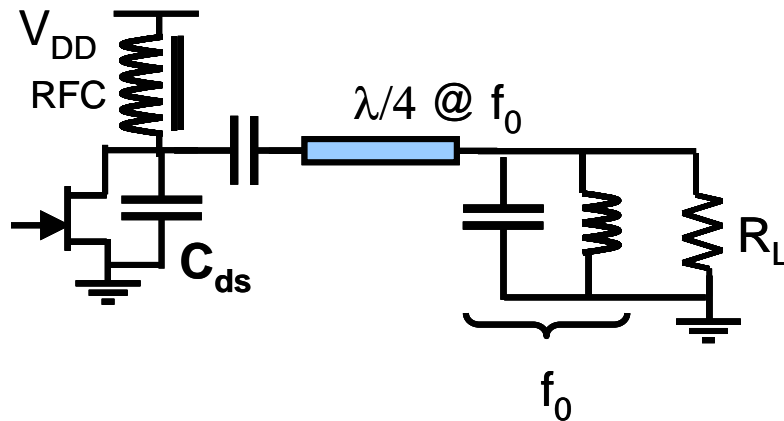
$$\text{Where } \kappa = \frac{V_{\text{peak}}}{V_1}$$

Note that P_{DC} is not affected by squaring the voltage. The DC current I_{DC} remains fixed at I_{max}/π .

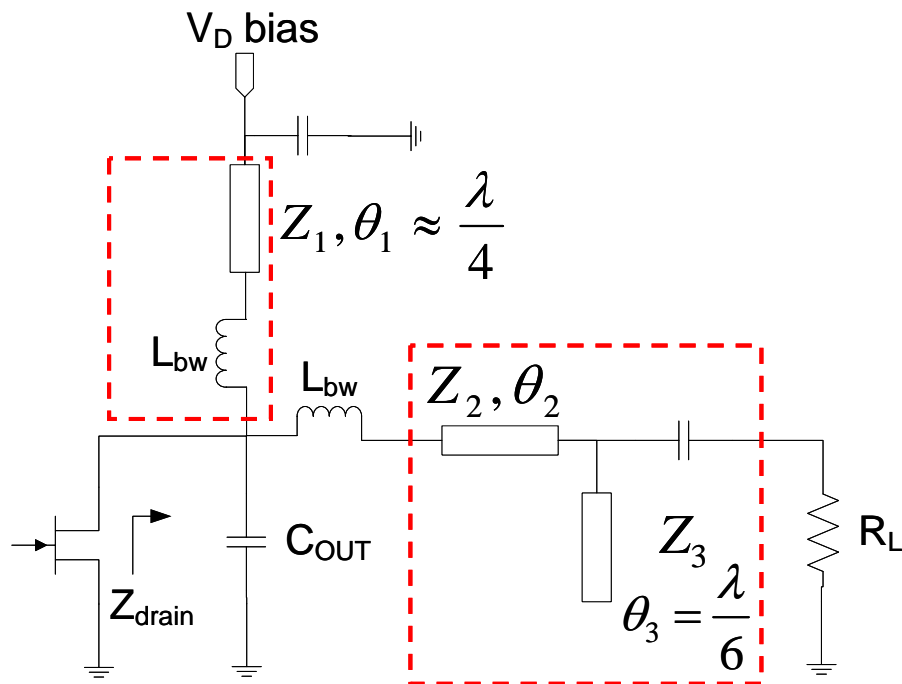
Class F circuits:



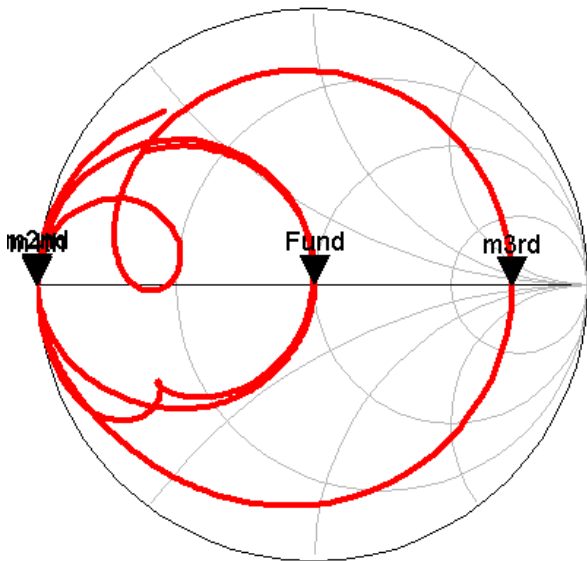
Circuit above gives low Z_L at even harmonics and high Z_L at $3f_0$.

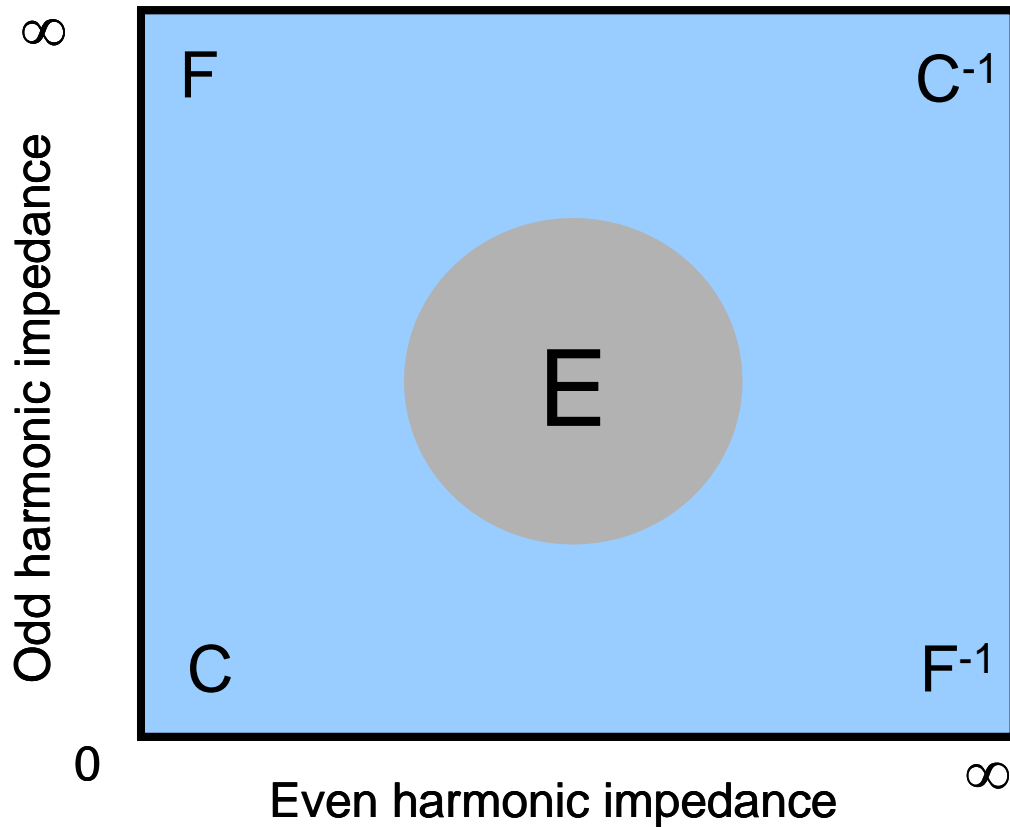


This circuit gives gives low Z_L at even harmonics and high Z_L at odd harmonics due to the impedance transforming nature of the quarter wave line (assuming the capacitive reactance of the tank C is small at harmonic frequencies).



- Dual bondwires off the drain pad improve even harmonic short
- Low impedance even harmonic termination (2nd and 4th)
- R_L and the 3rd harmonic peaking is set by Z_2, θ_2 and Z_3
- Matching network facilitates tuning after assembly

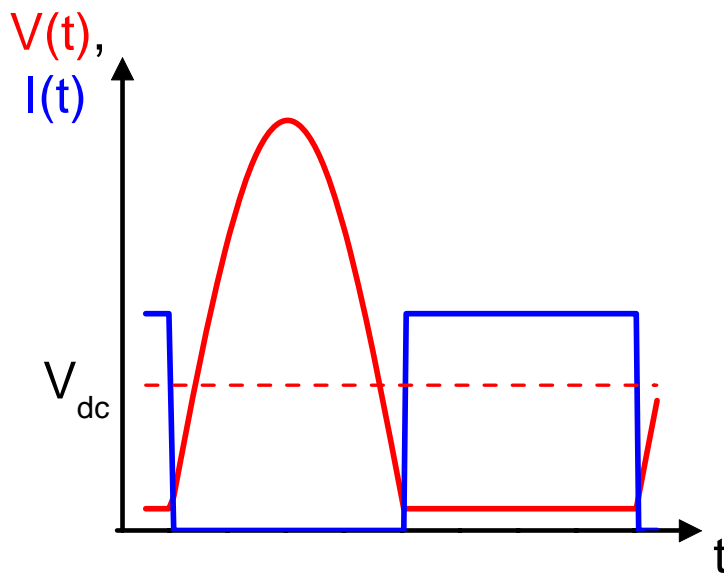
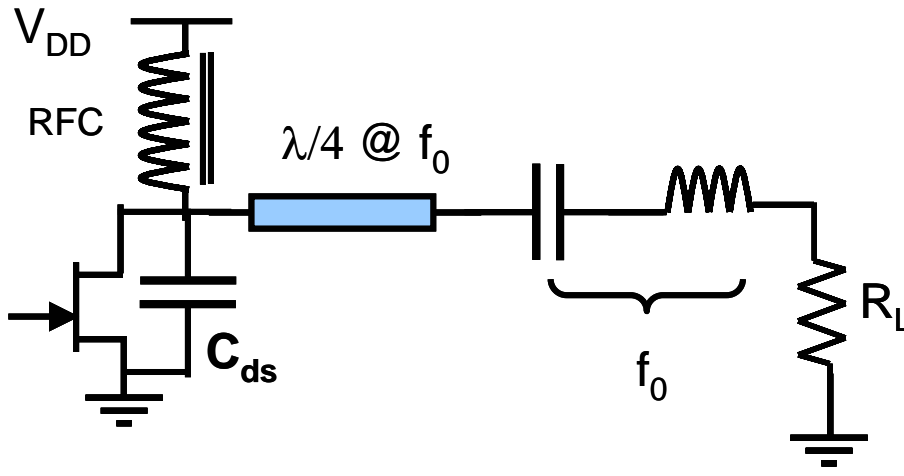




Let's also consider inverse F, the dual of Class F. It has the opposite harmonic requirements: high Z_L for even; low Z_L for odd harmonics.

F. Raab, "Class E, C and F Power Amplifiers based upon a finite number of harmonics," IEEE MTT, Vol. 49, #8, pp. 1462 – 1468, August 2001.

Inverse F circuit:



Inverse F voltage and current.

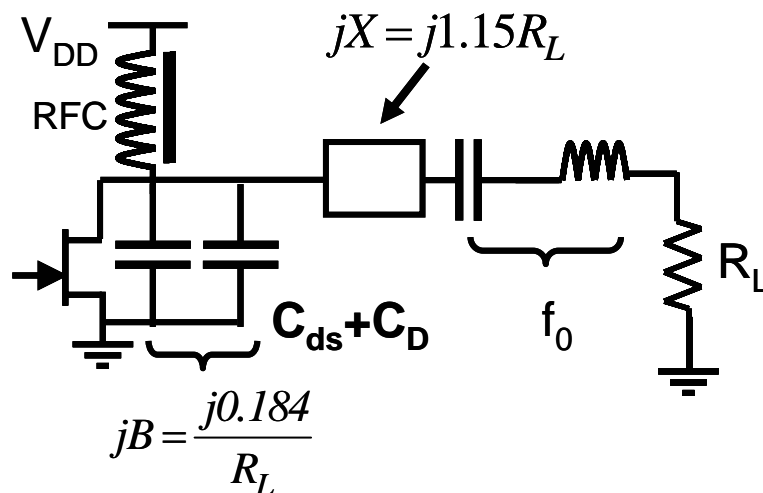
Class E PAs

- **Very popular on paper**
- **Very effective for most devices below 100 MHz**
- **Serious power/freq limitations above 1 GHz**
 - LDMOS, HBT, GaAs PHEMT
- **Power output capability less than AB or F**
- **GaN HEMT is clearly best device for Class E**
 - Needs low C_{DS} , high f_T and high V_{BR}
 - Require $f_T \gg 10 f_0$ for fast switching

$$V_{D,max} = 3.56V_{DD}$$

$$I_{D,max} = 2.86I_{DC}$$

$$POC = 0.098$$



Class E typical circuit implementation.

Design equations:

$$R_L = \frac{8V_{DD}^2}{P_{OUT}(\pi^2 + 4)}$$

Higher V_{DD} gives higher load resistance which is desirable for efficient implementation of the output network.

$$f_{E,\max} = \frac{P_{OUT}}{2\pi^2 C_{DS} V_{DD}^2}$$

The maximum Class E frequency of operation is limited by C_{DS} , the drain capacitance. While it appears that higher power leads to higher frequency, this is not the case. Consider V_{DD} fixed. Then, P_{OUT} scales with I_{\max} . The I_{\max}/C_{DS} ratio is a constant, thus the upper frequency is really determined by the device. Devices such as the GaN HEMT with a large I_{\max}/C_{DS} ratio perform at higher frequency than other devices such as LDMOS which have rather low I_{\max}/C_{DS} .

It is also evident that Class E stresses the device more than Class F or inverse F. Both the peak voltage and current are higher, thus POC at best is 0.098 rather than 0.159.

For example, a typical GaAs PHEMT might be constrained by:

- **Suppose $V_{D,\max}=10V$ $f_o = 2$ GHz $P_{OUT} = 1W$**

$$V_{DD} = 2.8v$$

$$R_L = 4.5 \Omega$$

$$\text{Maximum } C_{DS} = 3.2 \text{ pF}$$

$$I_{DC} > 1 \text{ A}$$

Summary

Reduced conduction angle can be used to improve efficiency of power amplifiers

Class B:

- Conduction angle π
- Same P_{out} as Class A, but P_{DC} is reduced. $POC = 0.125$.
- Maximum efficiency is 79%

All reduced conduction angle amplifiers require specific harmonic terminations as well as fundamental frequency load impedances in order to shape the current or voltage at the collector or drain of the power transistor.

Class F, inverse F and E can attain over 90% drain efficiency provided sufficient harmonics are possible. This requires a high performance device with high I_{max} , low CDS, and high f_{max} .

Read: S. Cripps, "Conventional High-Efficiency Power Amplifier Modes," Chap. 3 from RF Power Amplifiers for Wireless Communication, Artech House, 1999. (on RBR website)