CMOS Mixers and Polyphase Filters for Large Image Rejection

Farbod Behbahani, *Member, IEEE*, Yoji Kishigami, John Leete, *Member, IEEE*, and Asad A. Abidi, *Fellow, IEEE*

***Abstract*—This paper presents an in-depth treatment of mixers and polyphase filters, and how they are used in rejecting the image in transmitters and receivers. A powerful phasor-based analysis is used to explain all common image-reject topologies and their limitations, and it is shown how this can replace complex trigonometric equations commonly found in the literature. Practical problems in design and layout that limit the performance of image-reject upconversion and downconversion mixers are identified, and solutions are presented or limits explained. This understanding is put to work in a low-IF CMOS wideband, low-IF downconversion circuit, which repeatedly rejects the image by 60 dB over the wide band of 3.5 to 20 MHz without trimming or calibration.**

***Index Terms*—Analog complex filter, analog polyphase filter, image rejection, quadrature generation, radio receivers.**

I. Introduction

OBTAINING adequate image rejection with on-chip circuits poses the main obstacle to full integration of a superheterodyne wireless receiver (RX). In a zero-IF RX, the image of one half of a channel is the other half of the same channel; thus it is sufficient to reject the image by, say, 15 dB or so relative to the final required signal-to-noise ratio (SNR), and this is easily obtained with conventional quadrature downconversion. However, zero-IF suffers from several drawbacks such as dc offset and flicker noise, which cannot be easily eliminated without also removing valuable spectral energy around dc in the downconverted spectrum. By contrast, a low-IF receiver downconverts the desired channel to frequencies beyond the flicker noise corner. Although the IF amplifiers and filters operate at frequencies substantially the same as in a zero-IF receiver, the image now consists of some other unrelated channel two times the IF away in frequency, which may be substantially larger than the desired channel. This unrelated channel might have to be suppressed by up to 60 dB.

The image channel may be rejected by filtering prior to downconversion, or by signal cancellation. However, it is difficult to build active filters with sufficient selectivity and dynamic range at the high frequencies prior to final downconversion. A practical alternative is to cancel the image, by mixing quadrature phases of RF with the local oscillator (LO), or vice-versa, and following this with a Hilbert filter at the IF. A Hilbert filter responds to the complex representation of a signal, rather than to only its magnitude. This is relevant here because after downconversion, the signal and its image lie at the same frequency, but with conjugate complex representations. The ultimate image rejection is limited by the quadrature accuracy of the mixer input phases, gain matching of the mixers, and the accuracy of the phase shifts within the Hilbert filter. Without tuning, the repeatable image rejection of a simple quadrature mixer is limited to about 40 dB.

An interesting extension of the basic structure is the *double-quadrature architecture* [1]. It uses four mixers with both RF and LO inputs in quadrature phases. This structure is shown to be much less sensitive to the unbalance in the phase and amplitude of the RF and LO inputs of the mixers. The image rejection is now limited by the gain mismatch between mixers, and by inaccuracies in the IF phase shifter. It will be shown that in practice a carefully designed polyphase filter can repeatedly reject the image by 60 dB, comparable to what is possible with an off-chip IF filter.

II. Analog Polyphase Filter: Evolution and Principle of Operation

Before discussing the details of the passive polyphase filter, it is important to understand Hilbert filters in general. A conventional bandpass scalar filter is synthesized from a lowpass prototype by the symmetric lowpass-to-bandpass transformation, $s/j\omega_0 \mapsto (s/j\omega_0 + j\omega_0/s)$. It cannot distinguish between an input frequency and its image on the negative frequency axis, and offers the same frequency response to both [Fig. 1(a)]. On the other hand, a Hilbert filter creates a bandpass response by translating a lowpass prototype with the *shift transform*, $s \mapsto (s + j\omega_0)$, so the frequency response is no longer mirrored about zero frequency, and the desired frequency may lie in the passband, while the image frequency lies in the stopband [Fig. 1(b)].

With this in mind, a Hilbert filter may be synthesized to null the image while passing the desired frequency. The prototype is the single-pole *RC* filter with a notch at dc. The constitutive relation of the circuit is

$$(v_{\mathrm{in}} - v_0)sCR = v_0. \tag{1}$$

Applying the shift transform to this equation leads to

$$\begin{aligned}(v_{\mathrm{in}} - v_0)(s + j\omega_0)RC &= v_0\\ \Rightarrow (v_{in} - v_0)sC &= \frac{1}{R}(v_0 - j\omega_0 RC v_{\mathrm{in}}) + \frac{1}{R}j\omega_0 RC v_0\\ \Rightarrow (v_{\mathrm{in}} - v_0)sC &= \frac{1}{R}(v_0 - jv_{\mathrm{in}}) + \frac{1}{R}jv_0\\ \text{when}\quad \omega_0 RC &= 1.\end{aligned} \tag{2}$$

Manuscript received July 5, 2000; revised January 17, 2001.

The authors are with the Electrical Engineering Department, University of California, Los Angeles, CA 90095-1594 USA.

Publisher Item Identifier S 0018-9200(01)04136-1.

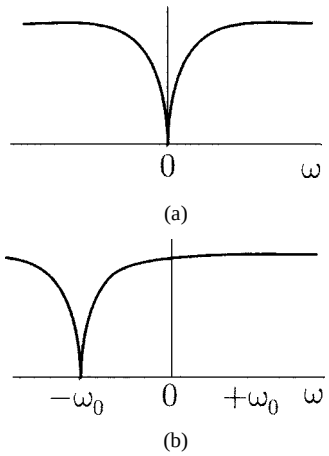

Fig. 1. (a) Conventional highpass filter with notch at dc. (b) Hilbert filter, which gives asymmetric response to positive and negative frequencies, obtained by shifting the characteristic of (a) on the frequency axis.

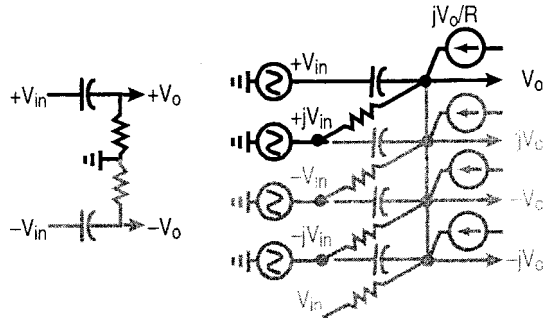

Fig. 2. Evolution of the simple *CR* highpass network into the corresponding Hilbert filter.

If the input signals are present in differential and quadrature phases, that is, as $\pm v_{\rm in}$ and $\pm jv_{\rm in}$, then resistor or capacitor connections between these signals and additional controlled sources realize the filter circuit. Repeating this structure for each of the four inputs, the circuit naturally extends to a differential quadrature topology (Fig. 2). At the image frequency when the filter produces $v_0 = 0$, the four controlled sources carry zero current. This means that the filter null is unaffected if these sources are deleted from the circuit. It is easily seen that removing the controlled sources only raises the passband gain by $\sqrt{2}$. This gain is unimportant as long as it is at least unity. The circuit that remains after deletion of the controlled sources is the classic passive *RC* polyphase filter [2].

The polyphase filter is a symmetric *RC* network with inputs and outputs symmetrically disposed in relative phases (Fig. 3). Consider applying four inputs, all sinewaves at the same frequency but with arbitrary amplitudes and phases as represented by the phasors shown in Fig. 4 (vector set i). Crucial to understanding the action of the polyphase filter in a simple geometrical way is the notion of input sequences, or basis functions [2]. The input phasor set can be decomposed into four balanced sequences: quadrature clockwise (phasor set C), quadrature counterclockwise (phasor set A), collinear differential (phasor set B), and collinear in-phase (phasor set D). The collinear components produce two pairs of common-mode outputs, which are rejected with differential sensing. The balanced components are found

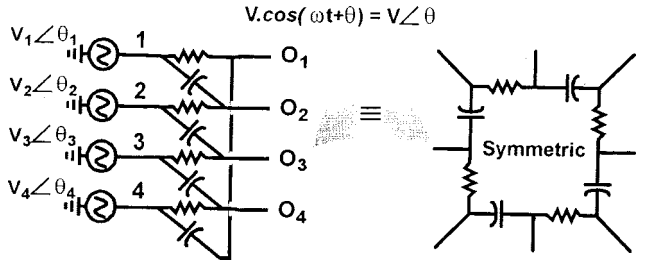

Fig. 3. Classic *RC* polyphase filter, shown in two different ways.

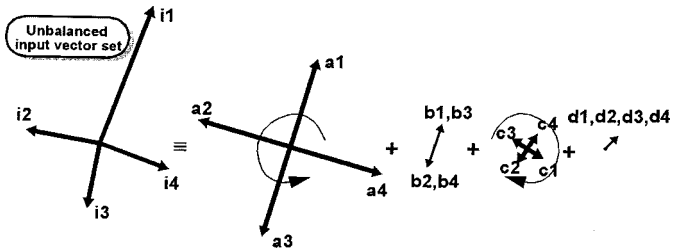

Fig. 4. Decomposing four inputs with arbitrary magnitude and phase into basis functions.

using

$$\begin{bmatrix} a1 \\ b1 \\ c1 \\ d1 \end{bmatrix} = \tfrac{1}{4} \cdot \begin{bmatrix} 1 & -j & -1 & j \\ 1 & -1 & 1 & -1 \\ 1 & j & -1 & -j \\ 1 & 1 & 1 & 1 \end{bmatrix} \cdot \begin{bmatrix} i1 \\ i2 \\ i3 \\ i4 \end{bmatrix}. \tag{3}$$

Fig. 5 shows the response of the filter to the two sets of phasors. If the input frequency is $1/2\pi RC$, two adjacent inputs are shifted by $+45°$ and $-45°$ to the output. The outputs of the branches add constructively (destructively) for counterclockwise (clockwise) quadrature inputs. Thus, the polyphase filter rejects the counterclockwise, collinear differential, and collinear in-phase components, and only passes the counterclockwise set at the *RC* pole frequency. The collinear phasors are rejected at all frequencies, whereas at frequencies other than the *RC* pole the counterclockwise sequence is rejected less.

The polyphase filter may be used in two places in a wireless receiver: to generate balanced quadrature phases from a single phase, and to reject the image. Fig. 6 shows how *differential quadrature* phases are generated from a *differential* input. The differential signal may be decomposed into two equal amplitude quadrature sequences, one clockwise and the other counterclockwise. When the input signal frequency is at the *RC* pole, the polyphase rejects the clockwise sequence and only the counterclockwise sequence comprising perfect balanced quadrature survives at the output.

For image rejection, the image and desired signals are first downconverted by quadrature LO phases, which maps them to the same frequency but into two opposite sequences. This follows from the trigonometric identities

$$\begin{aligned} &\sin(\omega_{\rm LO} \pm \omega_{\rm IF})t \times \sin \omega_{\rm LO} t \\ &\quad = \tfrac{1}{2}(+\cos \omega_{\rm IF} t - \cos(2\omega_{\rm LO} + \omega_{\rm IF})t) \rightarrow +\tfrac{1}{2}\cos \omega_{\rm IF} t \\ &\sin(\omega_{\rm LO} \pm \omega_{\rm IF})t \times \cos \omega_{\rm LO} t \\ &\quad = \tfrac{1}{2}(\pm \sin \omega_{\rm IF} t + \sin(2\omega_{\rm LO} + \omega_{\rm IF})t) \rightarrow \pm\tfrac{1}{2}\sin \omega_{\rm IF} t. \end{aligned} \tag{4}$$

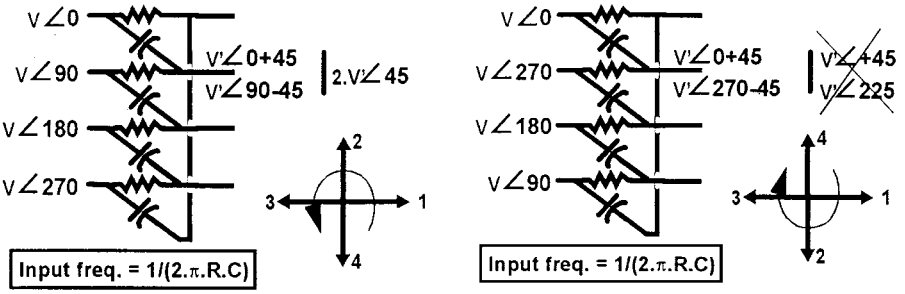

Fig. 5. Polyphase filter passes one input sequence (counterclockwise in this example), and nulls the other input sequence.

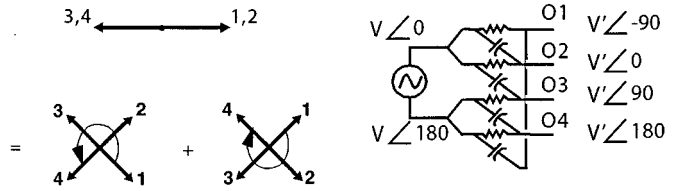

Fig. 6. Polyphase filter used to generate differential quadrature phases from a differential input. The input is the sum of two opposite sequences, one of which is nulled.

Then a polyphase filter tuned to $\omega_{\rm IF}$ following the mixers passes the desired signal but nulls the image.

Fig. 7 shows two possible arrangements for downconversion, referred to as single-quadrature downconversion. When either the RF inputs are in quadrature [Fig. 7(a)] or the LO inputs [Fig. 7(b)], the desired and its image downconvert into opposite quadrature sequences.

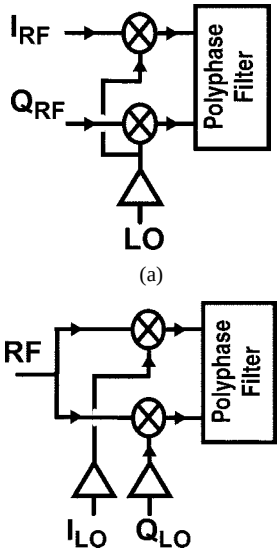

Fig. 7. Two possible image-reject downconversion arrangements, referred to as single-quadrature downconversion. (a) RF inputs in quadrature. (b) LO in quadrature phases.

III. Practical Design Considerations

This section addresses the practical design issues for an RX polyphase filter.

A. Bandwidth

The polyphase filter fully rejects an input sequence at only the *RC* frequency. Away from this frequency the rejection is weaker. Several stagger-tuned stages of the polyphase filter must therefore be cascaded if strong image rejection is required across a wide band. Fig. 8 shows the image rejection through a five-stage polyphase filter, whose pole frequencies are logarithmically spaced for equiripple response [3].

The larger the image rejection desired, or the higher the ratio of maximum to minimum signal frequency, the more polyphase stages needed in cascade (Fig. 9) [3]. In practice, the on-chip *RC* time constant may vary from lot to lot by $\pm 25\%$. Thus, in addition the filter must be designed to null over the bandwidth of one channel with $\pm 25\%$ added on as margin.

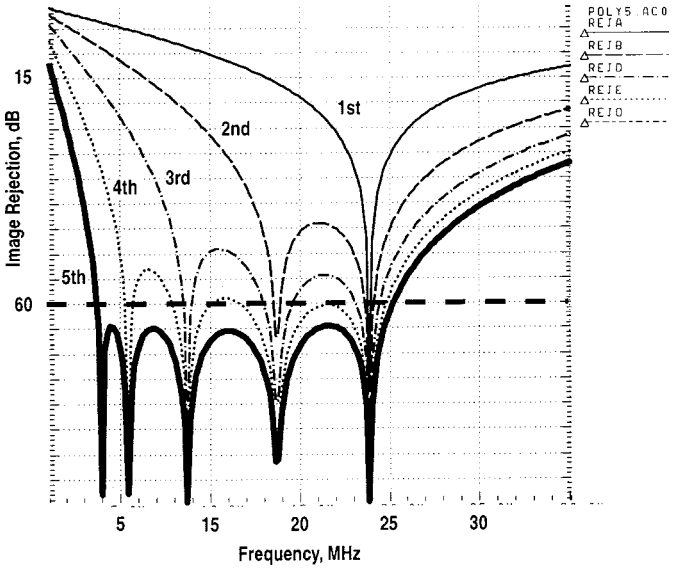

Fig. 8. Cascade response of five-stage stagger-tuned *RC* polyphase filter. Ideally, this delivers better than 60-dB image rejection over the desired frequency band.

B. Component Matching

Mismatch in the transfer function of each branch of the polyphase filter means that the phasors representing the image signal will no longer cancel exactly. The following analysis shows the relation between the mismatch and ultimately achievable image rejection. Consider one *RC* section of the filter [Fig. 10(a)]. With correct component values, the two inputs lying in the image sequence are rotated through this section and cancel exactly at the output. However, if the R and C deviate

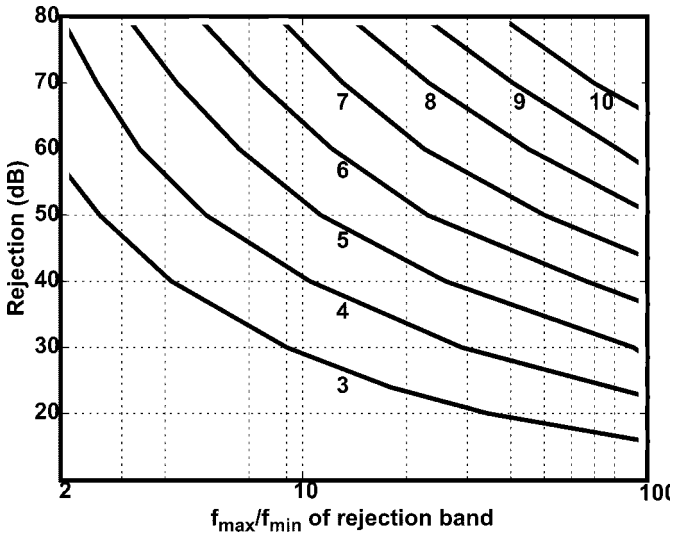

Fig. 9. Image rejection versus the relative bandwidth over which it is sought, with the number of necessary stagger-tuned *RC* stages in cascade as a parameter.

such that $R = R_0(1+\delta_R)$ and $C = C_0(1+\delta_C)$, and the input frequency $\neq 1/(2\pi RC)$, then from the well-known transfer functions of single-pole *RC* and *CR* networks, it follows that the polyphase section still rotates the two signals into antiphase, but their amplitudes are no longer equal [Fig. 10(b), (c)]. This results in nonzero output. Corresponding to a fractional deviation in time constant of δ_τ, the residual voltage is

$$\delta_A = \frac{1-\omega\tau(1+\delta_\tau)}{\sqrt{1+(\omega\tau(1+\delta_\tau))^2}} \simeq \frac{-\delta_\tau}{\sqrt{2}} \text{ around } \omega\tau = 1. \quad (5)$$

Four such uncorrelated signals appear at the polyphase filter outputs due to random mismatches in the four *RC* sections. From (1), they contain a balanced image sequence whose each phasor has an RMS value of

$$\sigma_{im} = \frac{1}{4}\sqrt{1+1+1+1}\,\sigma_A = \frac{\sigma_A}{2} \simeq \frac{A\sigma_\tau}{2\sqrt{2}}. \quad (6)$$

To find the image rejection, compare this with two input phasors of the same amplitude A but in the desired sequence. The output is now $\sqrt{2}A$, and the normalized RMS image leakage due to component mismatch is

$$\frac{\sigma\ (\text{Image Out})}{\text{Desired Out}} = \frac{\sigma_{im}}{\sqrt{2}A} = \frac{\sigma_\tau}{4} = \frac{1}{4}\sqrt{\left(\frac{\sigma_R}{R}\right)^2 + \left(\frac{\sigma_C}{C}\right)^2}. \quad (7)$$

Thus, to reject the image by 60 dB with 3σ yield, the filter resistors and capacitors must match to a σ of 0.094% assuming Gaussian distribution. It is known from experimental studies [4] that the variance of adjacent on-chip resistors and capacitors is proportional to the inverse of their surface area. Deep image rejection therefore requires elements with large area in the polyphase filter.

C. Resistor Cut-Off Frequency

Large area resistors suffer from distributed capacitance to the substrate [Fig. 11(a)]. Associated with the resistor is a cutoff frequency

$$f_R = \frac{1}{2\pi L^2 \rho C'_{\text{ox}}} \quad (8)$$

where

ρ sheet resistance;
L resistor length;
C'_{ox} capacitance per unit area to the substrate.

As a result a high frequency signal shifts in phase within the resistor. This disturbs the intended phase shift through the polyphase filter branches, and the image is no longer nulled. Fig. 11(b) shows the minimum ratio between the cut-off frequency to the highest pole frequency and the corresponding bandwidth for two to five stages of polyphase filters, with image rejection as a parameter. From (2), the required cut-off frequency sets the maximum resistor length. Fig. 11(b) is the same as Fig. 9, now taking into account resistor self-cutoff frequency. Compared to the ideal case, Fig. 9(c) shows that the rejection bandwidth is now lower.

D. Polyphase Voltage Gain and Loss and Frequency Response

Depending on the loading of the following stage, the desired signal traversing the polyphase experiences either gain or loss. As Fig. 12 shows, in the absence of loading equal input sinewaves at the *RC* pole frequency reach each output node in-phase and add together in voltage (6-dB gain). However, within each branch the input signal is attenuated by 3 dB through the *RC* or *CR* series combination, which results in a net voltage gain of 3 dB from each input node to the corresponding output node. When an identical stage loads the output without buffering, the resulting voltage division by 2 lowers the 3 dB of gain into a loss of 3 dB. The lower the load impedance, the higher the loss the desired signal suffers in each stage.

On the other hand, the relative suppression of the image is independent of this load, as long as the load is equal at all four outputs. This can be simply deduced from the fact that the null in the image sequence arises from a transmission zero which is unaffected by the grounded load.

If there are no grounded loads at the polyphase filter outputs, then at dc and very high frequencies either the resistors or the capacitors, respectively, transmit the input to the output with 0-dB voltage gain. In practice, some other circuit must follow a polyphase filter stage. If this is another stagger-tuned stage of the polyphase filter, the bottom plate parasitic associated with its capacitors loads the previous stage. If it is a differential pair, it is the differential input capacitance. In either case, as there is no resistive path to ground, the dc voltage gain through the stage in question remains 0 dB. However, voltage division between the polyphase filter capacitor and the grounded load capacitor attenuates the signal as frequency rises, and may be substantial at the desired signal frequency.

In a multistage polyphase filter, the cascade loss must be limited at the desired signal frequency, otherwise its noise figure will rise unacceptably. To control the total loss, the impedance

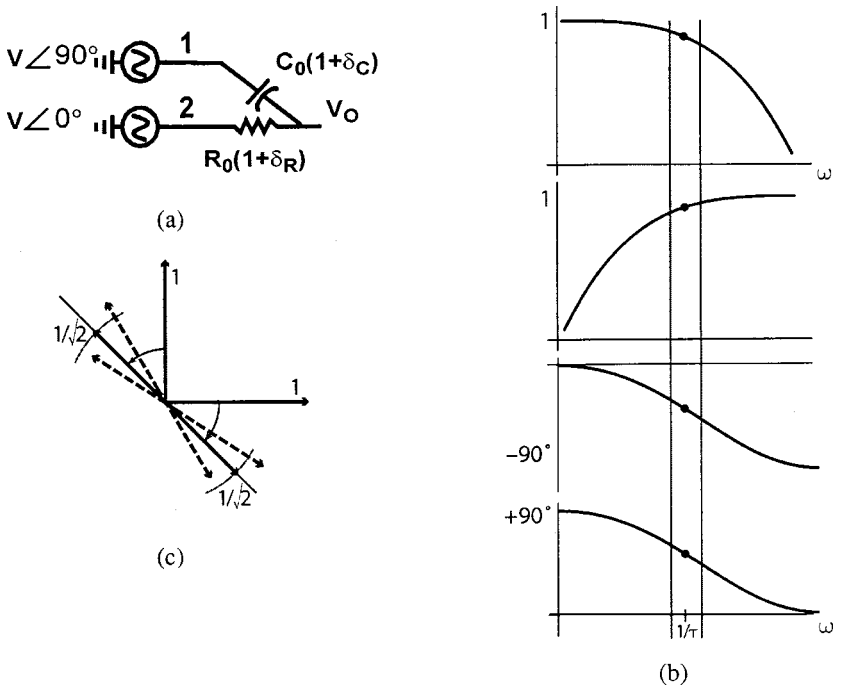

Fig. 10. (a) One signal-cancelling section of polyphase filter with deviated components. (b) Resulting ranges of magnitude and phase response in each branch. (c) Noncancelled residue signal.

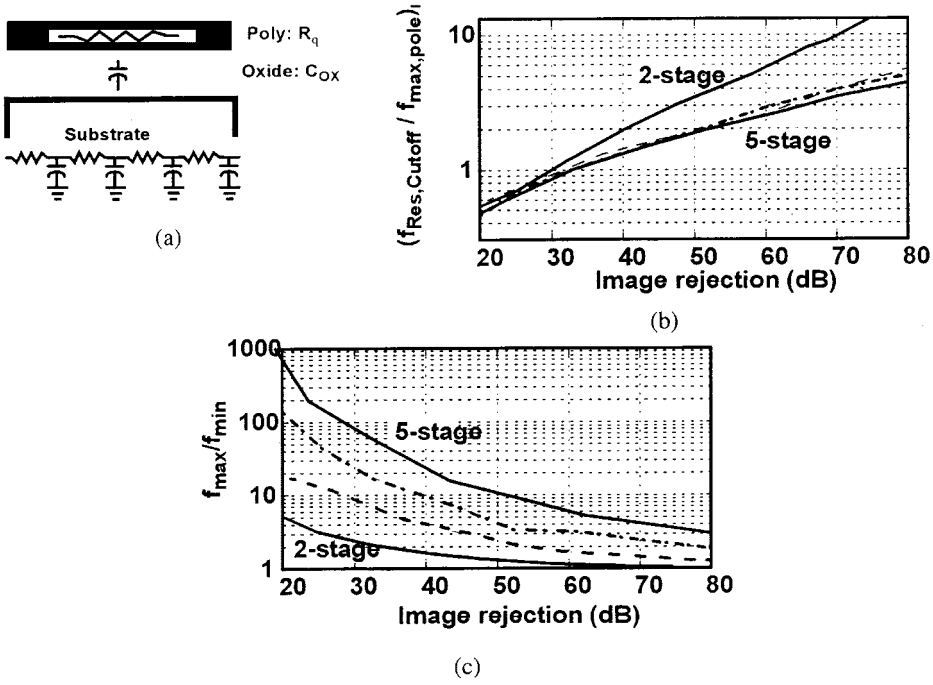

Fig. 11. (a) Parasitic capacitance to substrate associated with resistor. (b) Resistor cutoff frequency (as defined in text) versus signal frequency for a given image rejection. (c) Rejection bandwidth for various numbers of stages, if resistor cutoff is marginal.

of each successive stage is made larger so that it lightly loads the previous stage [Fig. 12(b)]. The stages use progressively larger resistors, with the largest value in the last stage; the stage capacitors are chosen to give the right pole frequency. Parasitic capacitance to substrate limits the highest usable resistance in the last stage, with the consequence that in a long cascade, the low resistance of the first stage may heavily load the circuit that drives the polyphase filter.

E. Polyphase Filter Input Impedance

The input impedance of a polyphase filter is strongly frequency dependent. This poses a problem when the input source resistance is nonzero.

In a multistage polyphase filter loaded at the output with capacitance only, there is no resistive path to ground, which implies very high input impedance at dc. At the pole frequency of the first stage, the input impedance falls to $R||(1/j\omega C)$. At

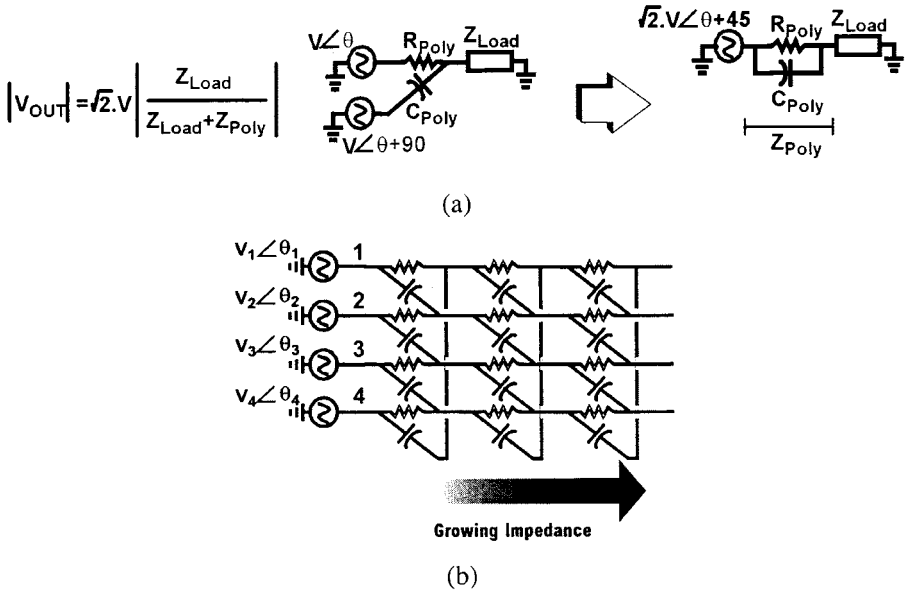

Fig. 12. (a) Signal summation at output node of a polyphase filter, and the effect of a grounded load at the output. (b) Tapering impedance in multistage filter to lower attenuation of desired signal.

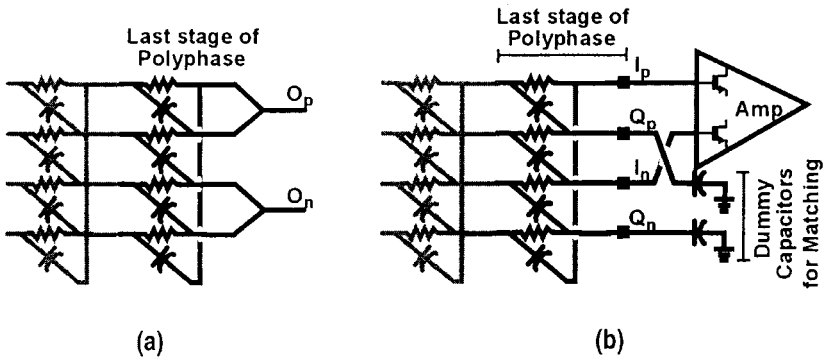

Fig. 13. Two possible ways to terminate a polyphase filter cascade to obtain a differential output. (a) Shorted pairwise outputs. (b) One output pair terminated in dummies.

very high frequencies, the input impedance is lower still, consisting of the load capacitance to ground in series with the filter capacitors. Thus, the input impedance transitions from infinite, through $R/(1+j)$, to mainly capacitive. When a transconductance stage such as a Gilbert mixer drives the filter with a wideband input, the voltage gain to low frequency signals will be much larger than the gain to the desired signal at the pole frequency. Strong adjacent channels might downconvert in a low-IF RX to lower than the pole frequency. Subject to the large gain in the polyphase filter, these interferers may saturate the receiver. Therefore, the polyphase filter must be driven by low source impedance, such as a voltage follower after a transconductance type mixer, to obtain a relatively uniform gain that does not disproportionately boost low frequencies.

F. Polyphase Filter Noise

All resistors in a multistage polyphase filter contribute noise. However, like the desired signal, noise originating in the first few stages is attenuated as it traverses the filter. If all stages use equal resistors but different capacitors for stagger tuning, the last stage's voltage noise spectral density $4kTR$ dominates at the output. Therefore, the last stage's resistance must be lower than some noise-determined upper limit. It follows that to avoid signal loss through the filter, the resistance in previous stages must taper down, possibly leading to a very low resistance in the first stage. The input source resistance must be capable of driving this resistance.

G. Polyphase Filter Output

The output of every stage in a polyphase filter exists in differential quadrature phases (I_0, Q_0, I_0', Q_0'). In practice, the circuit following the polyphase filter, usually an amplifier, is differential. A differential output can be tapped from the polyphase filter in two possible ways, shown in Fig. 13. In the first method I_0 is shorted to Q_0 and I_0' to Q_0'. In the second method, the output signal is taken from I_0 and I_0', or Q_0 and Q_0'. In the first method, quadrature phases of the same signal propagating in the I and Q branches add together (3-dB voltage gain), but each branch also loads the other branch shorted to it (6-dB voltage loss). Compared to open circuit output, the voltage gain to the desired signal in this filter stage is 3 dB lower, that is, net 0 dB. The second method, by contrast, gives the 3-dB net gain of a

polyphase filter terminated in an open circuit. However, the two unused outputs must be loaded by dummy capacitors, otherwise the unbalanced termination of the polyphase filter will degrade image rejection. It is difficult to exactly match dummy grounded capacitors to the input capacitance of a differential pair.

The limit to image rejection when the polyphase filter loads are mismatched depends on the ratio of the load to the filter capacitance. If the load capacitance is smaller, the spread in ratio of the load capacitance and the polyphase capacitance must obey (6). If the load capacitance is comparable or larger, the fractional spread of the load capacitors alone should obey (6). In general, the first method is less sensitive to load capacitance mismatch than the second method.

IV. Polyphase Filter Design Guide

The foregoing considerations may be summed up as a series of steps to design a practical polyphase filter that meets certain specifications.

- Step 1) Calculate the number of stagger-tuned stages required in the polyphase filter from the target image rejection and the fractional bandwidth over which this rejection is required.
- Step 2) As an initial guess, place the two lowest and highest poles at the boundaries of the rejection band. Space the remaining poles equally on the logarithmic frequency axis. The actual pole locations are fine-tuned by simulations.
- Step 3) Specify the matching between the resistors and between the capacitors based on the desired image rejection. This determines the physical area of the filter.
- Step 4) Large resistors will lower the power consumption of the amplifier driving the polyphase filter input. Use the largest filter resistance, limited either by the maximum noise at the output or by the cut-off frequency. In low-noise or low-frequency circuits, the first is the limiting factor, while in high-frequency polyphase filters it is the second.
- Step 5) To lower cascaded loss, taper down the resistance of the polyphase filter stages toward the input. The resulting impedance of the input stage of the polyphase filter will determine the drive requirements on the amplifier prior to the filter.
- Step 6) Design the driving amplifier. If the cascade filter loss is still too large, insert interstage amplifiers to preserve signal dynamic range within the polyphase filter.

V. Quadrature LO Generation

As explained in Section II, the structure in Fig. 6 generates balanced quadrature signals from differential inputs. Any common-mode signal at the input generates a collinear common-mode component at the output. The input common-mode signal may arise from imperfect balance at the input, or from the even-order nonlinearity in the previous stage. When a single-ended nonlinear circuit such as a limiter follows the filter, the collinear common-mode signal at each output shifts the zero crossings and corrupts the final phase relationship among the outputs. Thus, the outputs must be sensed using linear differential circuits that reject the common mode (Fig. 6).

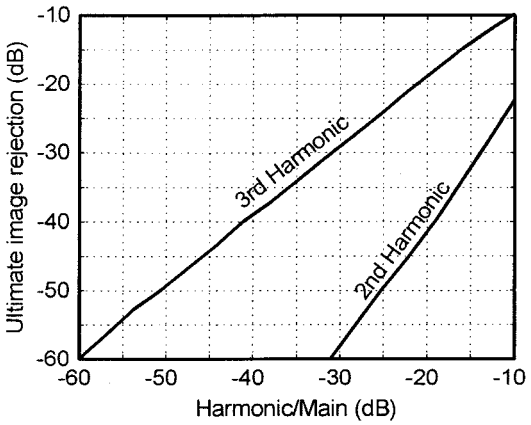

Fig. 14. Harmonics at input of polyphase filter upset the quadrature phase and duty cycle at output, and limit achievable image rejection after mixing.

A nonsinusoidal input waveform contains differential harmonics. These generate noncollinear components at the output that cannot be rejected as common-mode. The polyphase filter passes harmonics with an entirely different gain and phase than the fundamental, which upsets the duty cycle of the output waveform.

Fig. 14 shows the resulting ultimate limit on the image-rejection using single-quadrature downconversion followed by a two-stage polyphase filter to generate quadrature phases. The fundamental coincides in frequency with the first null of the polyphase filter. The error depends on the relative harmonic amplitude. The third harmonic shifts the zero-crossing positions, while the second harmonic shifts the zero crossing position and upsets duty cycle matching. This shows that only very small differential harmonic levels are tolerable for strong rejection of the image.

VI. Quadrature Upconversion

Quadrature mixers are used for single-sideband upconversion (SSUC). In this section, we describe the effect of imperfections on the final sideband suppression. The reader is asked to bear in mind the difference between upper and lower sidebands, each of which can appear in quadrature as one of two sequences (clockwise or counterclockwise).

A. Single-Quadrature Upconversion (SQUC) with Ideal Mixers

Consider upconversion with two mixers (Fig. 15) implemented by the relation $I_{\mathrm{RF}} = I_{\mathrm{LO}} \cdot I_{\mathrm{in}} + Q_{\mathrm{LO}} \cdot Q_{\mathrm{in}}$. With perfect quadrature sequences at the baseband (BB) and LO inputs, and matched mixers, only one sideband appears at the output; in this example, it is the lower sideband (LSB).

$$\cos\omega_{\mathrm{LO}}t \cdot \cos\omega_{\mathrm{in}}t + \sin\omega_{\mathrm{LO}}t \sin\omega_{\mathrm{in}}t = \cos(\omega_{\mathrm{LO}} - \omega_{\mathrm{in}})t. \tag{9}$$

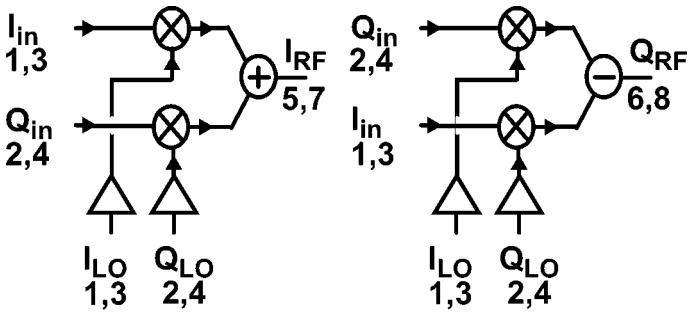

Fig. 15. Two possible arrangements for single-quadrature upconversion. Each signal is actually differential.

Reversing the sequence of either the input or the LO, which is equivalent to multiplying Q and Q' by -1, results in $I_{\rm RF} = I_{\rm LO} \cdot I_{\rm in} - Q_{\rm LO} \cdot Q_{\rm in}$. Now the upper sideband (USB) appears at the output.

$$\cos\omega_{\rm LO}t \cdot \cos\omega_{\rm in}t - \sin\omega_{\rm LO}t \sin\omega_{\rm in}t = \cos(\omega_{\rm LO} + \omega_{\rm in})t. \tag{10}$$

The other option is to implement the upconversion as $I_{\rm LO} \cdot Q_{\rm in} - Q_{\rm LO} \cdot I_{\rm in}$ (Fig. 15)

$$\cos\omega_{\rm LO}t \cdot \sin\omega_{\rm in}t - \sin\omega_{\rm LO}t \cos\omega_{\rm in}t = -\sin(\omega_{\rm LO} - \omega_{\rm in})t = \cos\left[(\omega_{\rm LO} - \omega_{\rm in})t + \frac{3\pi}{2}\right]. \tag{11}$$

It is important to note that the outputs of this mixer arrangement are rotated 90° relative to the previous arrangement, and therefore the output is notated as $Q_{\rm RF}$, as opposed to $I_{\rm RF}$. Again, reversing the sequence of either the input or the LO selects the upper sideband after upconversion but in opposite polarities, respectively, as $Q_{\rm RF} = -I_{\rm LO} \cdot Q_{\rm in} - Q_{\rm LO} \cdot I_{\rm in}$ and $Q_{\rm RF} = +I_{\rm LO} \cdot Q_{\rm in} + Q_{\rm LO} \cdot I_{\rm in}$ (Fig. 15). This fact is important for double-quadrature upconversion (DQUC), explained later.

Any unbalanced or nonquadrature sequence can be decomposed into a weighted sum of the ideal balanced quadrature sequence and the opposite error sequence (Fig. 16). Gain mismatch in the two mixers may be modeled as an unbalanced input applied to two matched mixers. Following the above argument, the opposite error sequence generates the unwanted sideband at the output. Since the phases of the error sequences in the input and LO are random and uncorrelated, the resulting unwanted sideband signal that each error produces could add or subtract. Thus, the relative size of the unwanted sideband is bracketed as follows:

$$\left|\frac{\rm LO_{er}}{\rm LO_{id}} - \frac{\rm IN_{er}}{\rm IN_{id}}\right| \le \frac{\text{Unwanted Sideband}}{\text{Desired Sideband}} \le \left|\frac{\rm LO_{er}}{\rm LO_{id}} + \frac{\rm IN_{er}}{\rm IN_{id}}\right|. \tag{12}$$

B. Double-Quadrature Upconversion (Ideal Mixers)

The double-quadrature upconversion (DQUC) topology [1] is merely the combination of the two SQUC circuits above (Fig. 17). Since both SQUCs share the same input sequences at the input, the signal phase at the output of one SQUC [see (9) and (10)] is in quadrature with the output of the other. In this way, the DQUC constructs a quadrature output sequence in response to an input quadrature sequence.

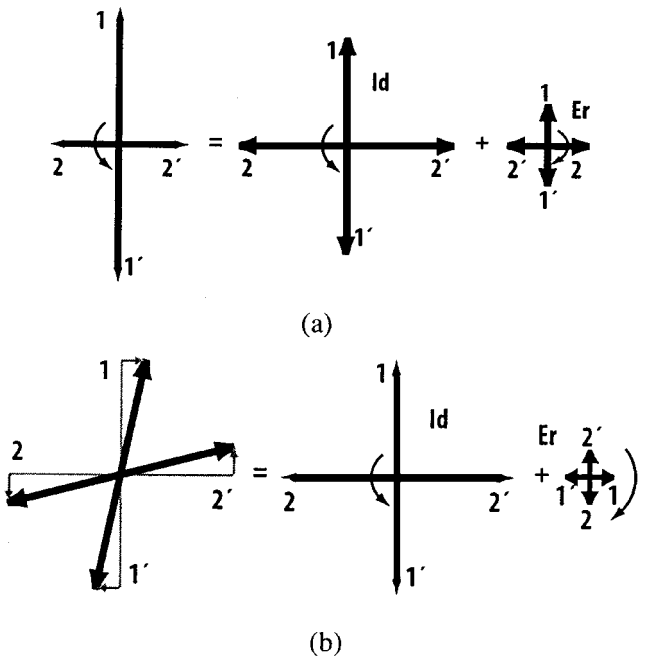

Fig. 16. Unbalanced quadrature sequences may be resolved into linear combinations of balanced sequences of both possible orientations. (a) Amplitude imbalance. (b) Quadrature imbalance.

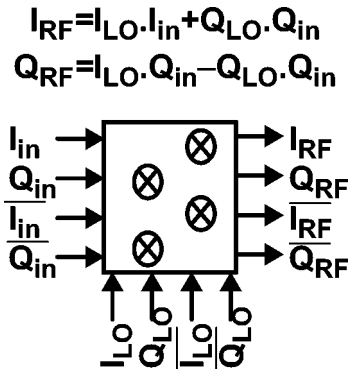

Fig. 17. Double-quadrature upconversion arrangement uses two single-quadrature mixers, whose mixed outputs are in relative quadrature.

Imperfect input and LO quadrature signals may be decomposed into a linear combination of opposite sequences, representing the ideal and the error. The ideal sequence of the input, after mixing with the ideal sequence of the LO, produces the desired upconverted sideband in what will be referred to as the desired sequence. $\rm In_{Er}$ and $\rm LO_{Id}$ after mixing generate the unwanted sideband, and so do $\rm LO_{Er}$ and $\rm In_{Id}$. Using the above analysis, the unwanted sideband due to input error will have the *same sequence* as the desired sideband. However, the LO error sequence generates an unwanted sideband with the opposite sequence. In upconversion, it is often the case that the input signal is at a much lower frequency than the LO frequency. Thus, after upconversion the upper and lower sidebands are close together in frequency. A polyphase filter tuned to the upconverted frequency will offer essentially the *same gain* to both *sidebands*,

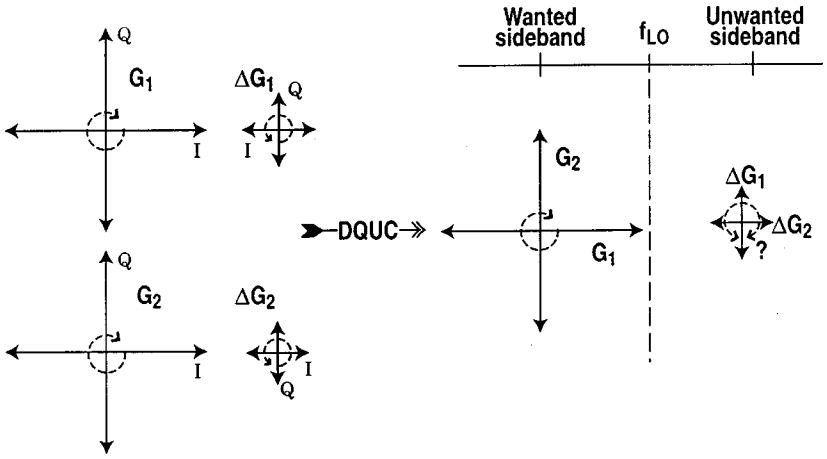

Fig. 18. Graphical analysis of mixer gain errors in the double-quadrature upconversion mixer.

but will *pass only one sequence*. Thus, the polyphase filter will pass the unwanted sideband that lies in the desired sequence. This limits the image rejection as follows:

$$\frac{\text{Unwanted Sideband}}{\text{Wanted Sideband}} \leq \frac{\text{In}_{\text{er}}}{\text{In}_{\text{id}}}. \tag{13}$$

In practice, large devices can improve the matching of the baseband circuits to create the input signal in highly accurate quadrature. This is much more difficult to do at the high frequency of the LO. Thus, the discussed property can significantly improve the unwanted sideband suppression in the DQUP system.

C. Mismatch in the Mixers

In the previous section, we assumed that the mixers are ideally matched. This is not true in practice. To analyze the effect of mismatch, assume balanced quadrature sequences of the LO and input but mismatch in the gain of the mixer pair to the input signal, $G = \Delta G$. The gain mismatch can be reflected back to the quadrature inputs. For SQUP, this may be thought of as an unbalanced quadrature sequence driving ideally matched mixers. From the analysis above, the unbalanced input may be resolved into a balanced sequence ($\propto G$) representing the main input, and another balanced sequence in opposite orientation ($\propto \Delta G$) representing the error; this *error sequence* upconverts into the *unwanted* sideband.

There are four mismatched mixers in the DQUP arrangement. To analyze this simply, notate each *pair* of SQUP mixers with a gain of $G_1 \pm \Delta G_1, G_2 \pm \Delta G_2$, where $\Delta G_{1,2}$ are zero-mean random variables of either polarity, and $G_{1,2}$ are uncorrelated. The mixer gain error is equivalent to unbalanced input sequences applied to matched mixers, much the same as in the SQUP case. The resulting output sequences are best visualized graphically (Fig. 18). They consist of a *wanted sideband* comprising a slightly unbalanced *desired sequence*, and an *unwanted sideband* with an *ambiguous sequence* which depends on the signs and relative sizes of the random variables $\Delta G_{1,2}$. A polyphase filter following the upconverter will pass one sequence and null the other for both wanted and unwanted sideband, which are usually close together in frequency after upconversion. Thus, the unwanted sideband is completely nulled with only 50% probability. To suppress the other 50%-likely case, the mixers must match to a relative value equal to the desired rejection of the unwanted sideband.

VII. Quadrature Downconversion

This section addresses issues of image-reject downconversion, where both the desired signal and the image signal pass through the mixer and are later rejected. Whereas in the upconversion case the image (unwanted sideband) is related to the wanted output, in a receiver the desired and image signals are two different channels, and therefore totally unrelated. Receivers are usually designed with the idea that the image is much larger than the desired signal.

Fig. 19(a) and (b) show two well-known downconversion architectures, labeled single quadrature, and Fig. 20 shows an extension which is termed double quadrature. Multiplying a differential input with a quadrature set of phasors produces another quadrature set at the translated frequency. After downconversion, the desired signal and the image lie in opposite sequences, as shown in Fig. 19. For quadrature LO and differential RF, the output sequence is opposite of (the same as) the input sequence, if the LO is high (low)-side injected. For quadrature RF and differential LO the opposite is the case. Therefore, following the mixer the appropriately configured polyphase filter selects the desired signal and suppresses the image.

Now consider the effect of imperfections. Suppose that either the RF input or the applied LO is not in exact quadrature. As before, the actual (nonquadrature) phases can be decomposed into an exact desired sequence, and a small opposite sequence representing the error. Whether the error is in the LO or in the RF input, after mixing the error sequence in the image will appear in the same sequence as the downconverted desired signal. As a result, this portion of the downconverted image will pass through the polyphase filter with the desired signal. The image rejection is therefore the ratio of the amplitude of the desired sequence to the error sequence. Exactly the same analysis applies if the amplitude of the quadrature input is unbalanced.

At high frequencies, the parasitics and finite resistor cut-off frequency make it difficult to supply the mixer with quadrature accuracy better that 1%, which limits image rejection to 40 dB. While quadrature phases of the LO may be derived in one of

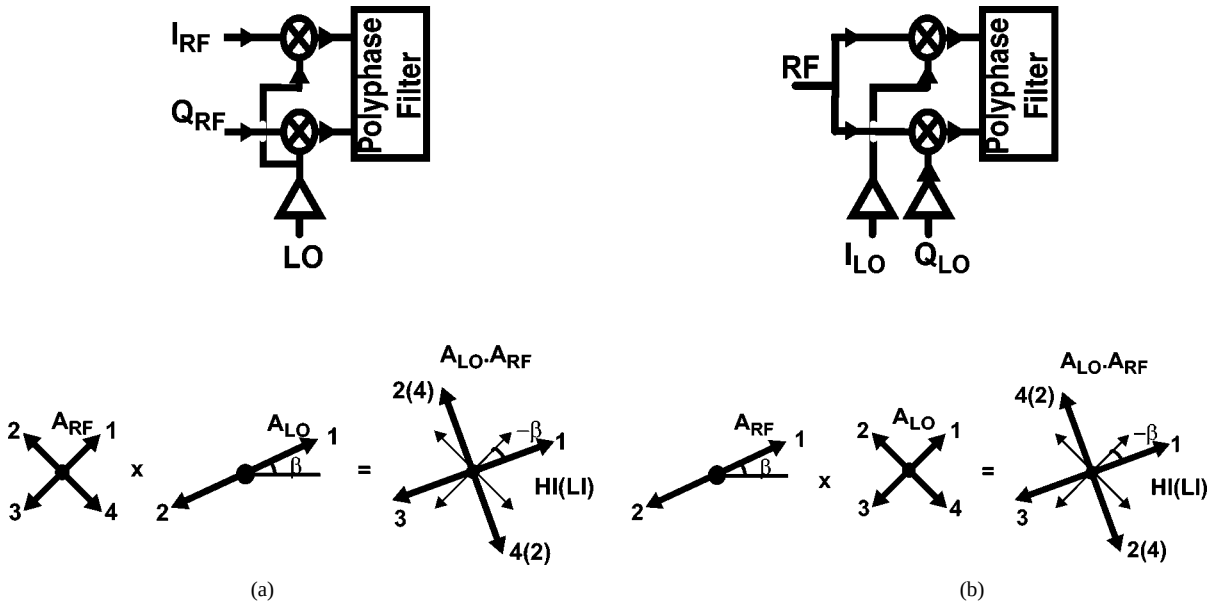

Fig. 19. Two possible single-quadrature downconversion mixers, followed by polyphase filter to null image sequence. The downconverted outputs are shown as phasor sequences. HI and LI refer to high and low LO injection.

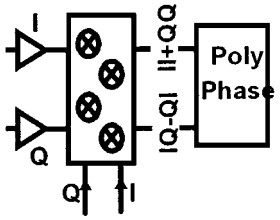

Fig. 20. Double-quadrature downconversion mixer.

many ways, such as *RC–CR* circuits, polyphase filters, quadrature oscillators, or divide-by-2 stages, only the first two are applicable to derive RF quadrature. In all cases, mixer gain mismatch and quadrature inaccuracy, whichever is larger, limits the image rejection.

When a large image rejection is required, the double-quadrature downconversion arrangement is a better choice. This uses four mixers, with both LO and RF inputs applied in quadrature, and the outputs of the mixers are combined as $I_{IF} = I_{RF} \cdot I_{LO} + Q_{RF} \cdot Q_{LO}$ and $Q_{IF} = I_{RF} \cdot Q_{LO} - Q_{RF} \cdot I_{LO}$. These comprise a pair of SQDC mixers. It has been noted before [1], and is proven below, that image rejection depends only to the second order on *quadrature inaccuracy* in the LO and RF. For instance, to reject the image by 60 dB, 3% quadrature accuracy is enough for each of the RF and LO inputs, instead of the 0.1% in single-quadrature downconversion.

The equations describing the four-mixer structure are the same for double-quadrature downconversion (DQDC) and DQUC. The four mixers are grouped into two pairs (Fig. 20). As is shown in Fig. 21, inaccurate RF and LO quadrature signals are decomposed into ideal and error quadrature sequences, RF_{Id}, RF_{Er}, LO_{Id}, and LO_{Er}. Four components appear at the output of the mixer sets, $RF_{Id} \times LO_{Id}$, $RF_{Id} \times LO_{Er}$, $LO_{Er} \times RF_{Id}$, and $RF_{Er} \times LO_{Er}$. The first term is the wanted output, downconverting the desired and image inputs to the same frequency but in opposite sequences. In the second and third terms, the sequence of one of the components is reversed. Now, recall the argument applied to the SQUC blocks. If either the RF or LO sequence is reversed, the mixer output will select the other sideband, here from the difference frequency (= IF) to the sum frequency. This means that the first-order error terms, $RF_{Id} \times LO_{Er}$ or $LO_{Er} \times RF_{Id}$, do not create any output at IF, but lie at the far-away sum frequency where they are easily removed by a lowpass filter. However, the fourth term, $RF_{Er} \times LO_{Er}$, generates output at IF with the same sequence of the desired signal. Thus the image downconverted due to the product of the errors, which is a second-order quantity, passes the polyphase filter.

So far it was assumed that the four mixers match perfectly. Gain (or delay) mismatch in the mixers unbalances the *output* (IF) sequence, which too can be decomposed into ideal and error sequences. The resulting IF sequence unbalance, which is proportional to the mismatch in the mixers, causes part of the image signal to fall into the same sequence as the desired signal. Therefore, the mixer mismatch limits the image rejection to the first order in DQDC.

VIII. Mixer Blocks

The choice of mixer circuit depends on the required image rejection and the input signal frequency. At high RF, differential pairs in a Gilbert-type mixer must use wide FETs of minimum channel length for good matching [5], and this raises the power consumption. In this respect, passive MOS switch mixers are superior. The ON-resistance of the switch must be lower than the polyphase filter resistor in series with it. This means that when the switches are ON, the *series resistors* determine mixer gain matching. However, the switch resistance dominates in the transition from OFF to ON. Now random or systematic spreads in threshold voltage and switch channel resistance will contribute mismatch in the time-averaged mixer conversion gain. An LO waveform with sharp edges alleviates this problem because the mismatches are apparent over a smaller fraction of the clock cycle. At low LO frequencies, this is readily obtained by

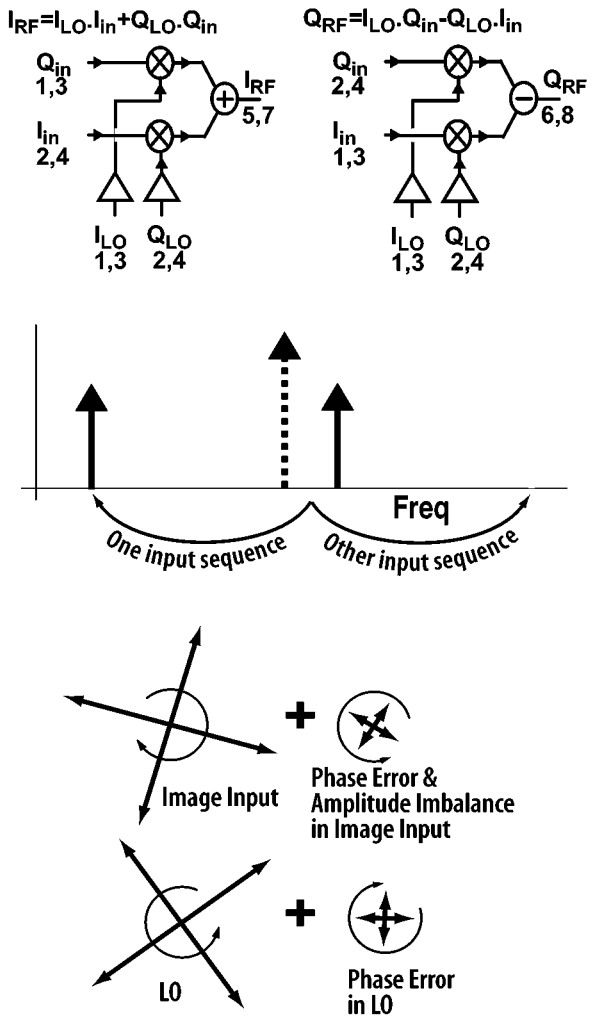

Fig. 21. Graphical analysis of errors in double-quadrature downconversion mixer, based on decomposition into two single-quadrature single-sideband select mixers.

switching the mixers with the rail-to-rail output of fast CMOS inverters.

A FET switch is nonunilateral. This has an important practical consequence in the double-quadrature mixer. Assuming a square-wave LO, at any time two among $\mathrm{LO_I}$, $\mathrm{LO_Q}$, $\mathrm{LO'_I}$, and $\mathrm{LO'_Q}$ are high. Without loss of generality, consider $\mathrm{LO_I}$, $\mathrm{LO_Q}$ both high as in Fig. 22. Then the two differential inputs, $\mathrm{RF_I}$ and $\mathrm{RF'_I}$ are shorted through four switches. This means that each input source is differentially shunted by $2r_{\mathrm{ON}}$, which will deeply attenuate the signal. This problem can be solved in two ways. First, isolating resistors can be inserted in series with the passive mixers (Fig. 23) increasing the effective r_{ON} of the mixer switches. Well-matched linear isolating resistors also improve gain matching among the mixers. However, the series isolating resistors induce signal loss. The second way to overcome this problem is to separately connect the four mixer outputs to a polyphase filter divided into two identical halves on a common centroid. The outputs of the two half circuits are finally connected together after the last polyphase filter section (Fig. 24). In this way, the input differential nodes of the ON mixers connect through all the polyphase filter stages in series, which lowers the loading on the driving stage.

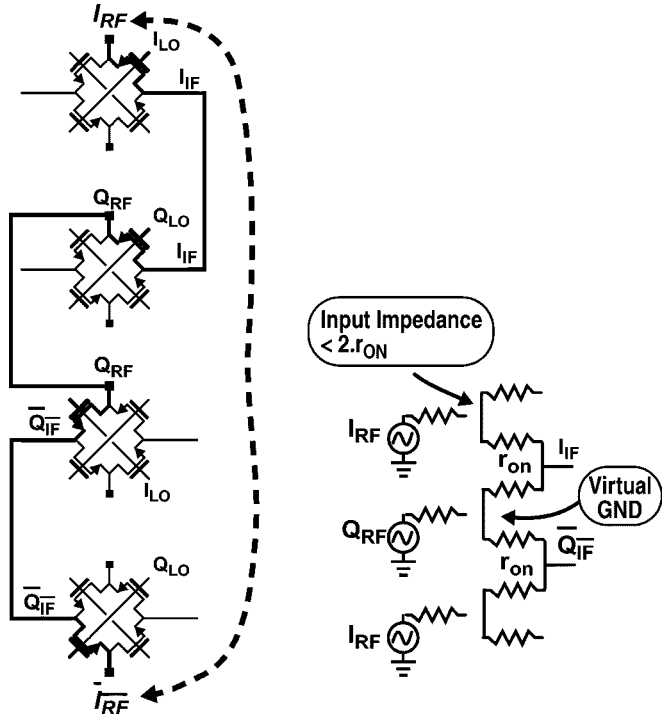

Fig. 22. Passive FET mixers connected in double-quadrature arrangement load-driving circuits with their ON resistance.

IX. Amplification Within Polyphase Filter

In a wideband multistage polyphase filter, the cascade loss may accumulate to the point that interstage amplifiers must boost the signal if it is not to be overcome by noise. To fulfill the specification on image rejection, the amplifiers in each branch must match as accurately as the polyphase filter components. This requires careful layout and use of large area MOSFETs which match well in V_t. The gate area of FETs in low frequency amplifiers may be enlarged by using wide and long channels, while holding the ratio W/L at a reasonable value. Now only the required dynamic range, not area, determines power consumption. However, in high-frequency amplifiers the minimum f_T required for successful operation may constrain L to some upper limit, and FET area can only be enlarged by increasing W/L leading to higher bias current.

The interstage amplifier must have large dynamic range in order not to limit overall receiver dynamic range. Furthermore, as explained in Section III, the polyphase input impedance is strongly dependent on frequency. To maintain a relatively flat overall gain versus frequency, the interstage amplifier's output impedance must be much lower. This requires a two-stage amplifier, in which the first stage provides gain and the second stage provides the low output impedance. Output impedance may be lowered with a source follower, or with voltage sampling feedback.

The cascade loss is high through a passive downconverter followed by a multistage polyphase filter. The optimum point for inserting the amplifier to maximize the dynamic range is where it divides the total cascade loss into two equal parts. Section XI illustrates this in an image-reject downconversion circuit.

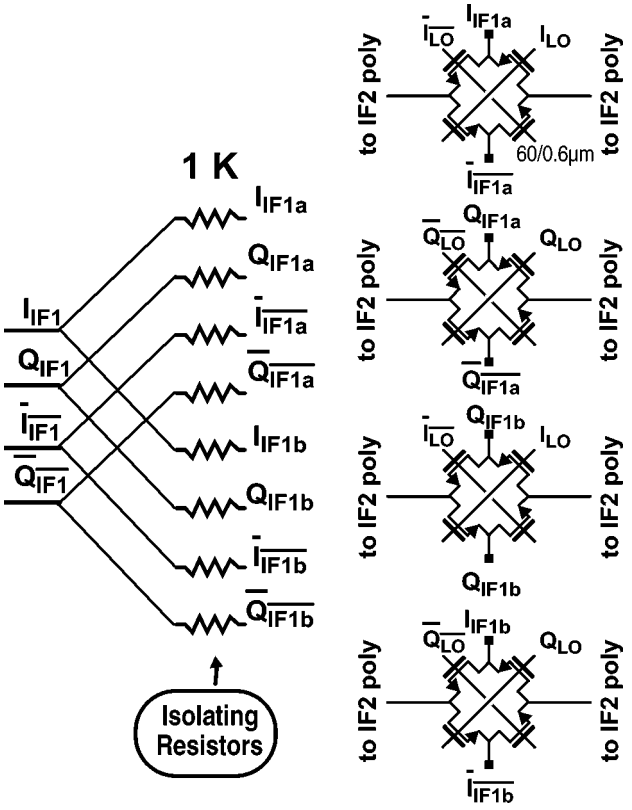

Fig. 23. Isolation resistors in series with mixers lower the input source loading, and improve matching of gains in the multiple branches when mixer switches are ON.

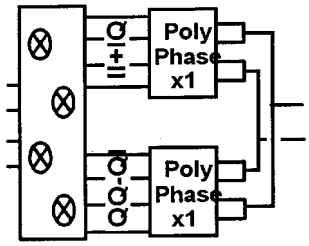

Fig. 24. As an alternative to shorting the mixer outputs pairwise and driving the polyphase filter, the signals are kept separate and shorted at the output of two identical polyphase filters in parallel. This significantly lowers loading on input source.

X. Layout Considerations

Careful layout is very important to match the polyphase filter elements to the required degree. Physical area defines the matching among the adjacent resistors and the capacitors. All the *R*'s and *C*'s in one stage are laid out in the same orientation. Dummy resistors and capacitors covering at least a 50-μm distance are placed at the edges of the polyphase filter (Fig. 25) to shield against lithography edge effects during fabrication. Good matching for large image rejection mandates use of physically large resistors and capacitors, which widens the layout of the entire polyphase filter. This block can now suffer from processing gradients. To overcome linear gradients, the polyphase filters are laid out in common centroid, which however makes the interconnections complicated and long, with many lines crossing each other. In general, the interconnect lines are of different length, and cross each other

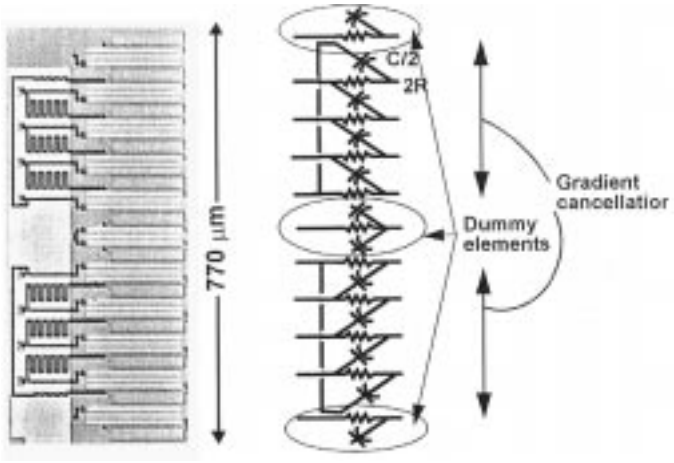

Fig. 25. Layout of one stage in the cascade, showing common centroid and dummy elements.

asymmetrically. To balance the parasitic interconnect resistance in each branch, the interconnect lengths are equalized. As shown in Fig. 26, one solution is to use serpentine shapes as part of all the parallel interconnections. By adjusting the height of the serpentine, the wire length in the branches may be equalized while keeping the same number of corners. Another problem is in the asymmetry in crossover capacitances. If the process has three or more metal layers, a grounded isolating metal plate may be inserted between the signal lines, as shown in Fig. 26. This converts the asymmetric interline capacitance to symmetric line-to-ground capacitance. Two parallel signal lines should be placed far enough apart so that the interline capacitance is negligible.

One gradient-compensated stage of the polyphase filter comprising two half circuits now has eight capacitors and eight resistors. Considering the required distance between the parallel lines, the area occupied by wiring between the two halves may exceed the area of *R*'s and *C*'s. An alternative, more area-efficient approach is to connect two halves of the polyphase filters at the input of the first stage, and then at the output of the last stage. Therefore, the solution shown in Fig. 24 is also area efficient.

XI. Design Example

To verify these concepts, a standalone downconversion prototype (Fig. 27) with an input frequency of 220 MHz and an IF band spanning 3.5–20 MHz has been designed. This is an unusually wide channel bandwidth (16.5 MHz) centered at a low IF (10 MHz) in a wideband wireless LAN receiver. The target image-rejection is 60 dB across the full IF band (Fig. 8). The double-quadrature architecture lowers sensitivity to quadrature errors in the RF and LO mixer inputs. To reject the image by 60 dB, the phase must be accurate to 3%. Quadrature phases are generated in two-stage polyphase filters tuned to 220 MHz. A simple noncommon centroid layout with small area components would have been appropriate for the polyphase filters before downconversion, but as no information was available regarding on-chip process gradients, a common-centroid layout was used here as well.

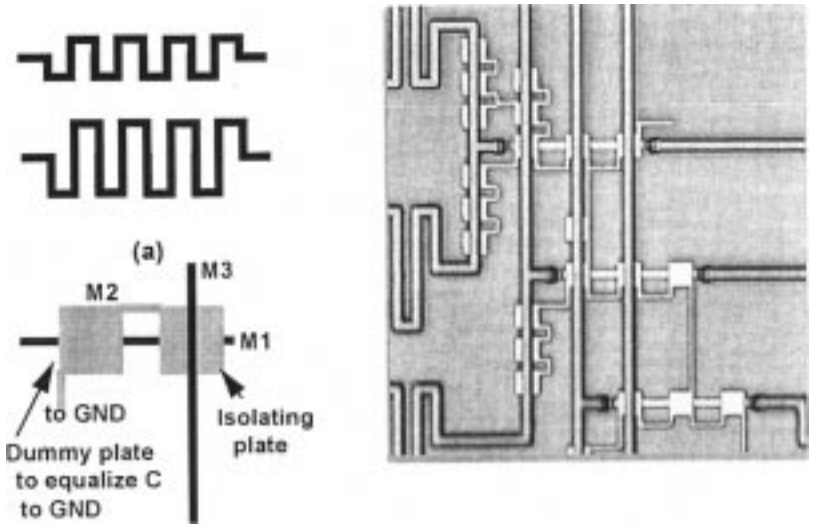

Fig. 26. Illustrating considerations of interconnect to balance resistance and capacitance in every branch of polyphase filter.

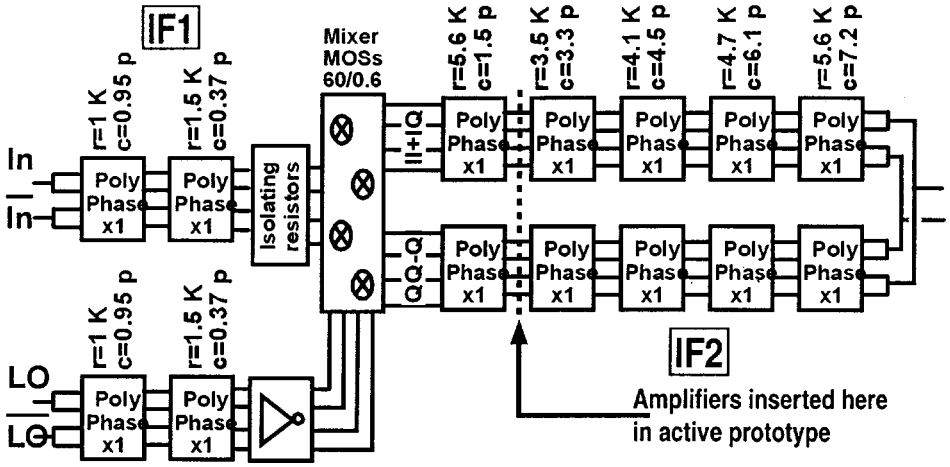

Fig. 27. Passive prototype of high-image-rejection double-quadrature downconverter. IF1 $=$ 270 MHz, IF2 $=$ 10 MHz. Interstage amplifiers were inserted in a second active prototype.

The downconversion mixer FETs of 60/0.6 μm and the IF polyphase filter R's and C's must match to 0.1%. The passive 4-FET mixers are padded with 1-kΩ polysilicon resistors. When the mixer FETs are hard-switched with very short transition times, series resistors determine gain matching in the various branches. Fast CMOS inverters with small rise and fall time used as LO buffers guarantee sharp transitions.

Using the guidelines presented earlier in this paper, a five-stage stagger-tuned polyphase filter is designed to obtain the desired image rejection across the 10-MHz channel bandwidth (actually the image is rejected across 3.5–20 MHz to allow for 25% spreads in resistance and capacitance). Test resistors were first fabricated to measure mismatch statistics, and it was found that the resistor area must be 2400 μm^2 to match to 0.1%. The capacitors must be at least 0.5 pF to match to the same accuracy.

The desired signal is attenuated by 25 dB as it traverses the cascade of lossy blocks of the passive RF polyphase filter, the padded passive mixers, and the passive IF polyphase filter. As the object of fabricating this standalone prototype is to determine the ultimately achievable image rejection, it contains no interstage amplification.

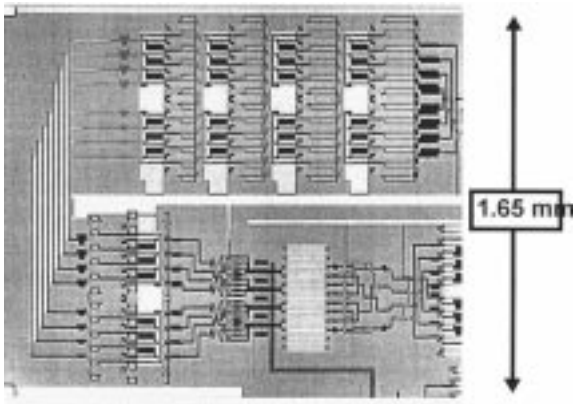

Fig. 28. Microphotograph of active prototype.

The final chip micrograph is shown in Fig. 28. Fig. 29 plots the image-rejection measurement results for various samples of the passive prototype. It is notable that the image rejection is

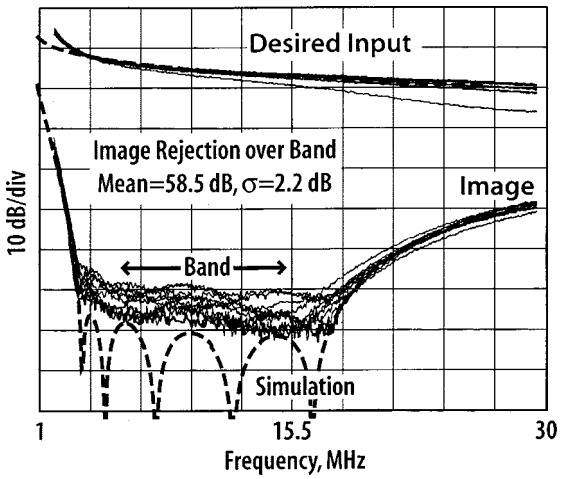

Fig. 29. Measured image rejection on twelve test chips, compared with simulated image rejection with perfectly matched elements.

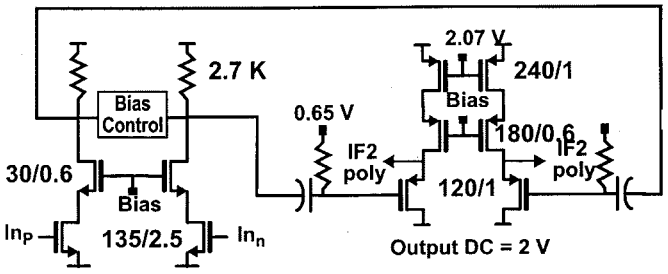

Fig. 30. 10-MHz interstage amplifier. Topology and FET sizes are chosen for 0.1% mismatch on two differential paths in polyphase filter.

very close to the simulated response. The average image rejection is 58.5 dB. Due to the large loss, this block cannot be used as is in a receiver.

An active version of the image reject downconverter containing interstage amplifiers was embedded in a full receiver [6]. Fig. 30 shows the interstage amplifiers, which are inserted after the first stage of the five-stage IF polyphase filter (Fig. 27). In this way, the total loss in the cascade is divided into two 10-dB sections, interpolated by the amplifiers. This arrangement gives the maximum dynamic range. The input to the common-source (CS) amplifier is biased through the polyphase stages and the passive mixer by the output voltage of the amplifier driving the IF1 signal. The source-follower (SF) output stage is ac coupled to the CS stage. Large-area FETs limit the gain mismatch between the two differential amplifiers in I and Q paths to less than 0.1% RMS. As the amplifier operates in the 10-MHz (IF2) band, long channel FETs are used without adverse impact of the lower f_T. Each IF2 amplifier drains 9.5 mA. The coupling capacitor between the two stages creates a highpass pole at about 5 MHz. To some extent, the highpass transition band compensates the droop in the polyphase filter's frequency response. The amplifier followed by four stages of polyphase has input-referred differential noise of 6.4 nV/$\sqrt{\text{Hz}}$, and IIP3 of $+15$ dBm referred to 100 Ω. The total loss from the input of the IF2 amplifier to the end of the IF2 polyphase filter is about 1 dB. Fig. 31 shows the

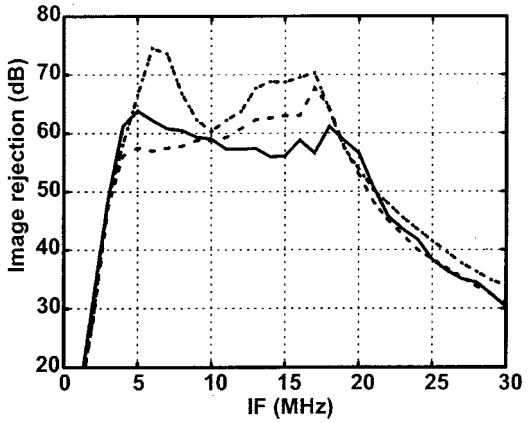

Fig. 31. Measured image rejection in three samples of polyphase filters, including interstage amplifiers.

image rejection from three samples of the final receiver to be on average about 60 dB, which is comparable with the performance of the passive chain. It may be deduced that interstage amplifiers appropriately designed for the required frequency band and matching do not degrade the image rejection performance, but in fact yield very good dynamic range at reasonable power consumption.

XII. Conclusion

The operation of passive analog polyphase filters and downconversion mixers has been described in easy-to-understand terms as phasor sequences. The preferred downconversion mixer architecture has been identified, and the practical limitations to the image rejection in the combination of the polyphase filter and mixer are explained. The fundamentals are put to test in a 0.6-μm prototype wideband image-reject mixer, which is able to repeatedly achieve an unprecedented 58-dB image rejection across a 10-MHz-wide bandwidth centered at an IF of 10 MHz. Carefully designed interstage amplifiers are required to limit the cascade loss of the system, yet maintain image rejection.

References

[1] J. Crols and M. Steyaert, "A single-chip 900-MHz CMOS receiver front-end with a high-performance low-IF topology," *IEEE J. Solid-State Circuits*, vol. 30, pp. 1483–1492, Dec. 1995.

[2] M. J. Gingell, "Single-sideband modulation using sequence asymmetric polyphase networks," *Electric. Commun.*, vol. 48, no. 1–2, pp. 21–25, 1973.

[3] R. C. V. Macario and I. D. Mejallie, "The phasing method for sideband selection in broadcast receivers," *EBU Rev. (Technical Part)*, no. 181, pp. 119–125, 1980.

[4] M. J. McNutt, S. LeMarquis, and J. L. Dunkley, "Systematic capacitance matching errors and corrective layout procedures," *IEEE J. Solid-State Circuits*, vol. 29, pp. 611–616, May 1994.

[5] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, "Matching properties of MOS transistors," *IEEE J. Solid-State Circuits*, vol. 24, pp. 1433–1440, May 1989.

[6] F. Behbahani, J. C. Leete, Y. Kishigami, A. Rothmeier, K. Hoshino, and A. A. Abidi, "A 2.4-GHz Low-IF receiver for wideband WLAN in 0.6-μ m CMOS—Architecture and front-end," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1908–1916, Dec. 2000.

Farbod Behbahani (M'99) was born in Tehran, Iran, in 1967. He received the B.S. and M.S. degrees (with honors) in electrical engineering from Sharif University of Technology, Tehran, Iran, in 1990 and 1993, respectively, and the Ph.D. degree from the University of California, Los Angeles (UCLA), in 1999.

From 1992 to 1995, he worked for Philips Semiconductors as an RF and Analog Integrated Circuit Designer. From 1995 to 1999, he was a Research Assistant at UCLA. Since 1999, he has been with Valence Semiconductor Inc., Irvine, CA, where he is the Director of Engineering, RF and Wireless. His research interests include RF CMOS and adaptive architecture for wireless radio. He has received four U.S. patents and is an author or co-author of more than 25 technical papers in the area of integrated circuit design and communication systems.

Dr. Behbahani was a corecipient of the second prize in the annual Iranian national research contest in 1996 and the IEEE Solid-State Circuits Society Pre-Doctoral Fellowship in 1997. He received the Young Scientist Award from the Association of Professors and Scholars of Iranian Heritage in California in 1999. He was also recognized as the outstanding Ph.D. in electrical engineering from UCLA in 2000.

Yoji Kishigami was born in Tokushima, Japan, in 1967. He received the B.S. and M.S. degrees in physics from Kyoto University, Kyoto, Japan, in 1991 and 1993, respectively.

He joined Asahi Kasei Corporation, Japan, in 1993, where he has been engaged in the research and development of RF ICs. From 1998 to 1999, he was a research scholar in the Electrical Engineering Department, University of California, Los Angeles, where he worked on the design of CMOS RF circuits.

John Leete (M'99) received the B.S. degree in electrical engineering from North Carolina State University, Raleigh, NC, in 1995 and the M.S. degree in electrical engineering from the University of California at Los Angeles in 1999.

He is currently with Broadcom Corporation, El Segundo, CA. His current interests include RF IC design for wireless communications and ESD protection strategies for RF circuits and systems. He is a member of Phi Kappa Phi and Eta Kappa Nu.

Asad A. Abidi (S'75–M'80–SM'95–F'96) received the B.Sc. (Hons.) degree from Imperial College, London, U.K., in 1976 and the M.S. and Ph.D. degrees in electrical engineering from the University of California, Berkeley, in 1978 and 1981.

He was with Bell Laboratories, Murray Hill, NJ, from 1981 to 1984 as a Member of Technical Staff in the Advanced LSI Development Laboratory. Since 1985, he has been with the Electrical Engineering Department of the University of California, Los Angeles, where he is a Professor. He was a Visiting Faculty Researcher at Hewlett-Packard Laboratories during 1989. His research interests are in CMOS RF design, high-speed analog integrated circuit design, data conversion, and other techniques of analog signal processing.

Dr. Abidi was the Program Secretary for the International Solid-State Circuits Conference from 1984 to 1990 and General Chairman of the Symposium on VLSI Circuits in 1992. He was Secretary of the IEEE Solid-State Circuits Council from 1990 to 1991. From 1992 to 1995, he was Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS. He has received the 1988 TRW Award for Innovative Teaching and the 1997 IEEE Donald G. Fink Award. He was a corecipient of the Best Paper Award at the 1995 European Solid-State Circuits Conference, the Jack Kilby Best Student Paper Award at the 1996 International Solid-State Circuits Conference (ISSCC), the Jack Raper Award for Outstanding Technology Directions Paper at the 1997 ISSCC, and the Design Contest Award at the 1998 Design Automation Conference.