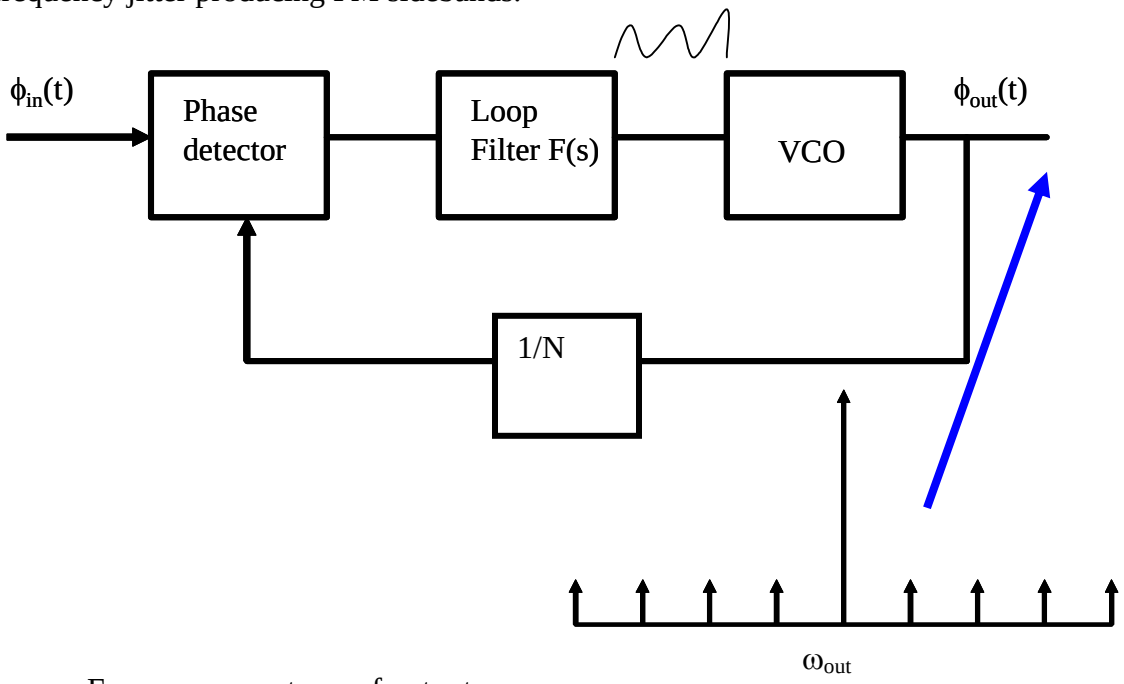
## Third-order PLL

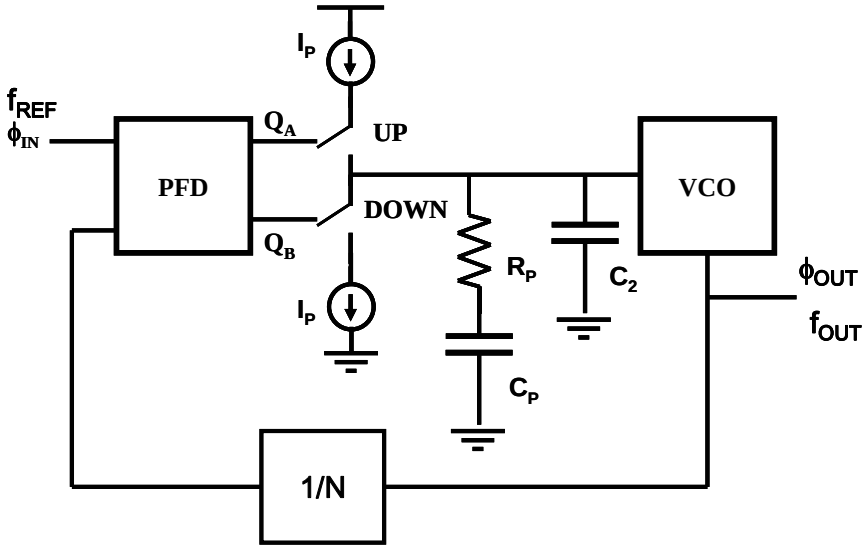
There is still one residual problem that we have overlooked. The phase detector produces pulses of variable width that activate the switches to either charge or discharge the capacitor $C_P$ in the case of the charge pump PFD-CP combination. Now that we have added the resistor $R_P$, which is absolutely necessary for stability, we find that the control voltage coming out of the charge pump will jump up or down before settling to its steady state value. This occurs because you cannot change the voltage across a capacitor instantaneously, so the initial voltage drop occurs across $R_P$, which then charges $C_P$ exponentially. This jumpy control voltage frequency modulates the VCO at the reference frequency, creating reference spurs. This is not such a big problem if N = 1 because the jump will be at the same frequency as the VCO. But, at larger N values, it creates low frequency jitter producing FM sidebands.



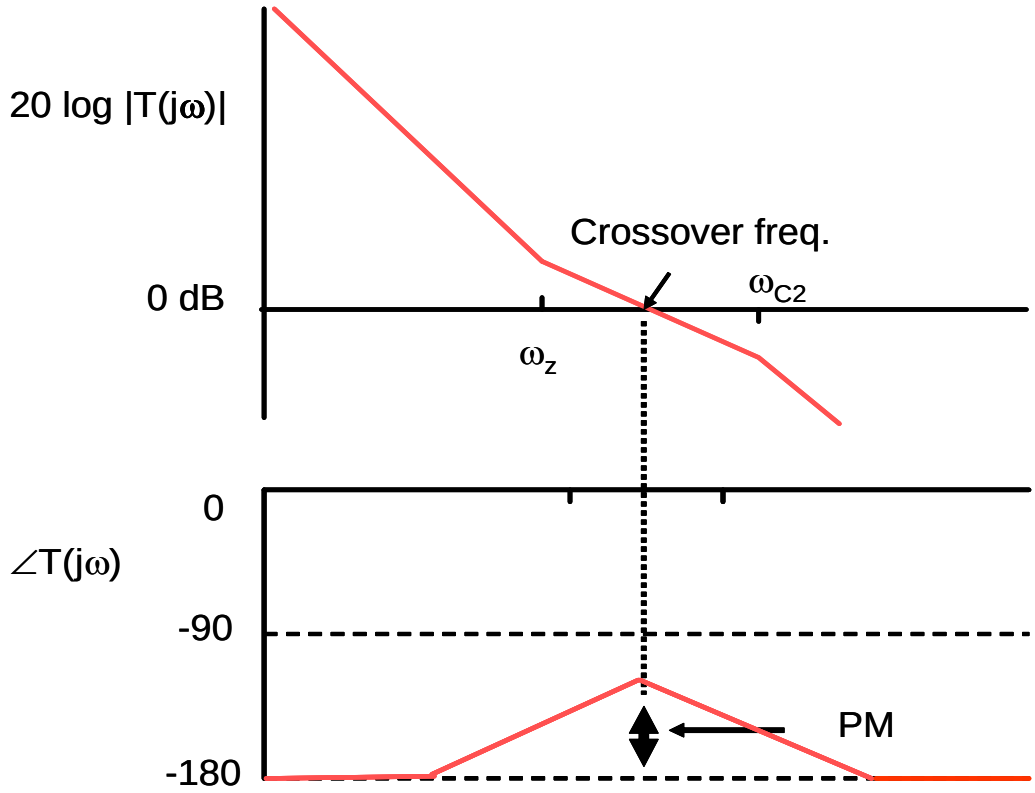

Frequency spectrum of output.
Reference spur sidebands are spaced at intervals of $\omega_{in}$.

So, we need to fix this by adding a second capacitor, $C_2$, whose function is to filter out the jumpy response of the series RC network. The magnitude of the reference spur sidebands is reduced. Unfortunately, however, $C_2$ adds a third pole of finite frequency that will reduce the stability of the PLL. Now, the handy tools we have been using for predicting performance of the second-order PLL no longer are accurate.

A look at the Bode plot verifies this.

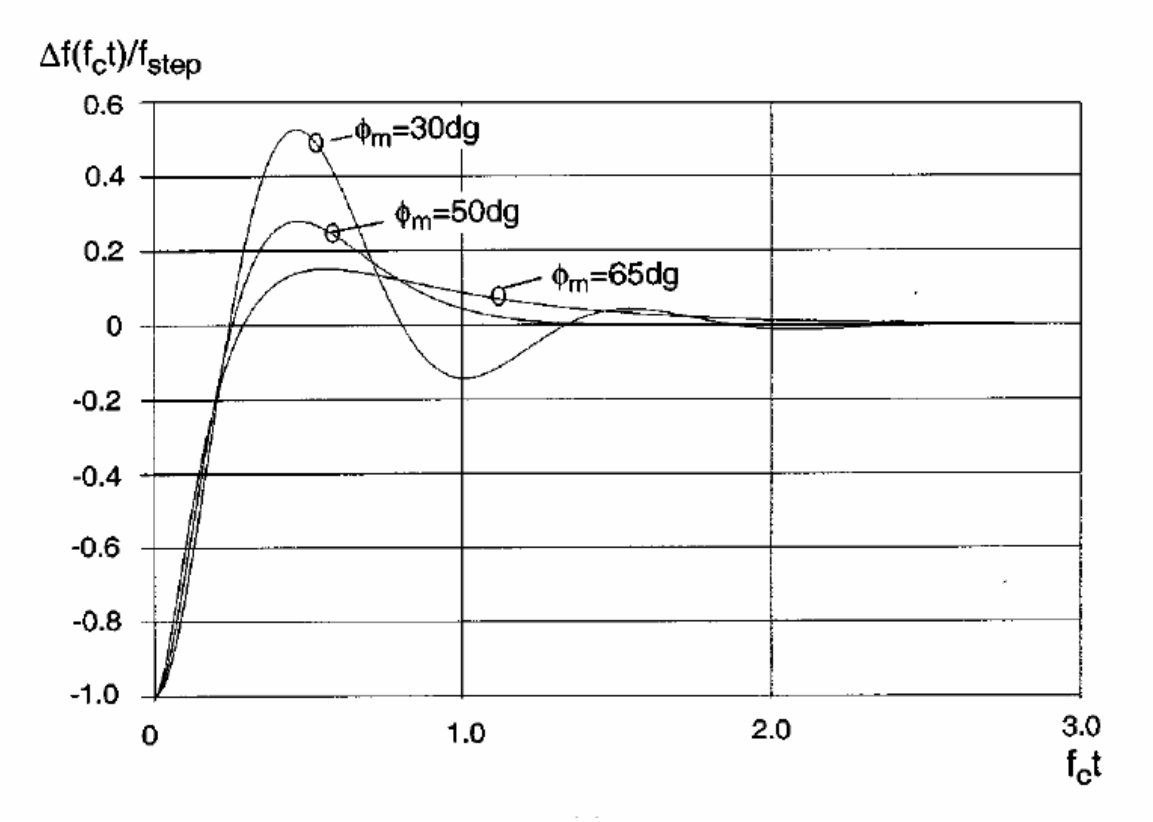



$$\omega_z = \frac{1}{R_P C_P} \qquad \omega_{p3} = \frac{C_P + C_2}{R_P C_P C_2}$$



The pole frequency is given by $R_P$ in parallel with the series combination of $C_P$ and $C_2$. Thus, the pole is always higher in frequency than the zero. We can see that the added pole reduces the phase margin. In fact, now when the loop gain is increased, phase margin is reduced.

Since the second order model using $\omega_n$ and $\zeta$ are no longer valid for predicting settling behavior, a different way is needed to relate crossover frequency and phase margin to settling time. The figure below, from Vaucher[1] provides this link. A frequency step response is plotted. In this figure, the frequency error, $\Delta f$, is normalized to a frequency step, fstep, and is plotted against a normalized time axis, $f_C t$. Here, $f_C$ is the crossover frequency. $\phi_m$ is the phase margin.

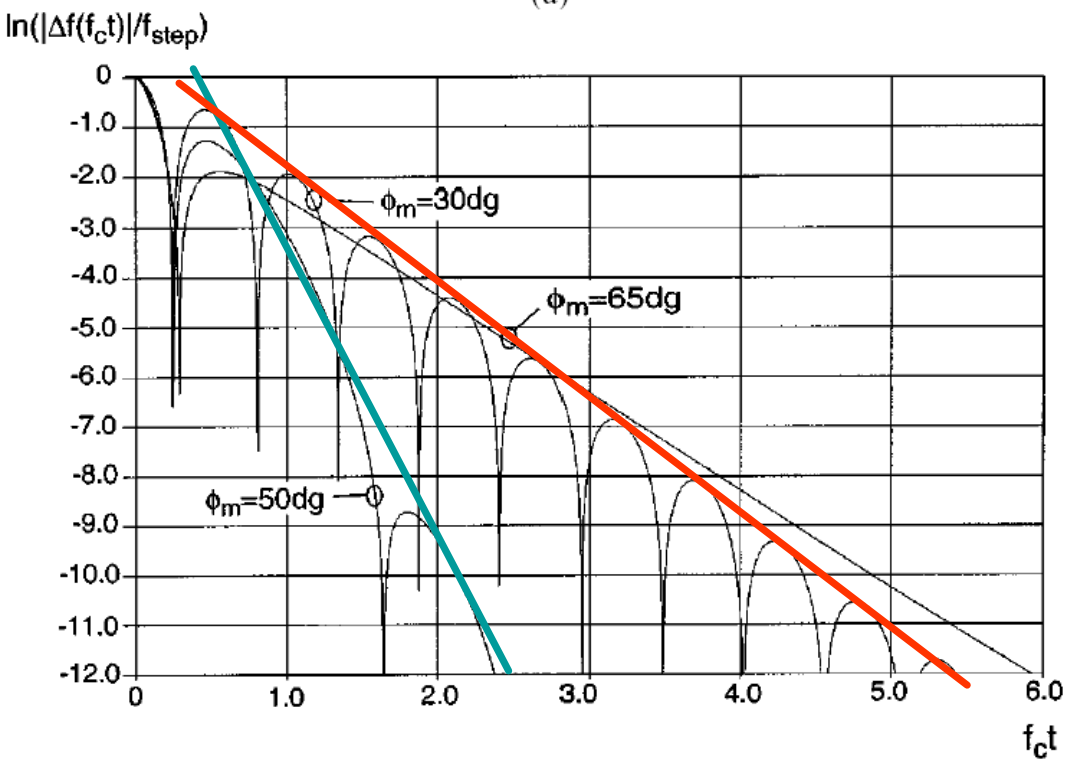



According to the plot, a PM of 50 degrees produces more overshoot, but settles faster than 65 degrees. If the higher overshoot can be tolerated, this would be a better choice. If less overshoot is required, then the 65 degree PM is best. A higher $f_C$ will be required, however, to meet the same settling time spec. The 30 degree case seems to have no benefits.

[1] C. S. Vaucher, "An adaptive PLL tuning system architecture combining high spectral purity and fast settling time, IEEE J. Solid State Cir., Vol. 35, #4, pp. 490 – 502, April 2000.

The next plot shows the settling transient for different PM values expanded on a log scale [1]. The vertical axis plots $\ln(|\Delta f(f_c t)|/f_{step})$. This gives the remaining frequency error $\Delta f$ in response to a step in frequency $f_{step}$ plotted against a normalized time axis $f_C t$.

(a)




(b)

Fig. 3(b). The red and green lines trace the envelope for the 30 and 50 degree cases. For example, at $t_{lock} = 2f_C t$ and $\phi_m = 50$ degrees, the frequency has settled to within $e^{-9} = 1.23 \times 10^{-4}$ of its final value. (ref. C. Vaucher, op. cit.)

This plot can be used to determine the crossover frequency required for a particular settling time, $t_{lock}$.

**Ex.** Suppose we want to achieve settling to within 0.1 % in 2 ms.

$\ln(0.001) = -6.9$.

If we choose the 50 degree PM, $f_C\, t_{lock} = 1.7$

So, $f_C = 1.7/0.002 = 850$ Hz.

Because some applications require a smaller residual settling error, Vaucher [1] also provides a plot showing settling time to $e^{-10}$ ($4.5 \times 10^{-5}$) vs. phase margin.

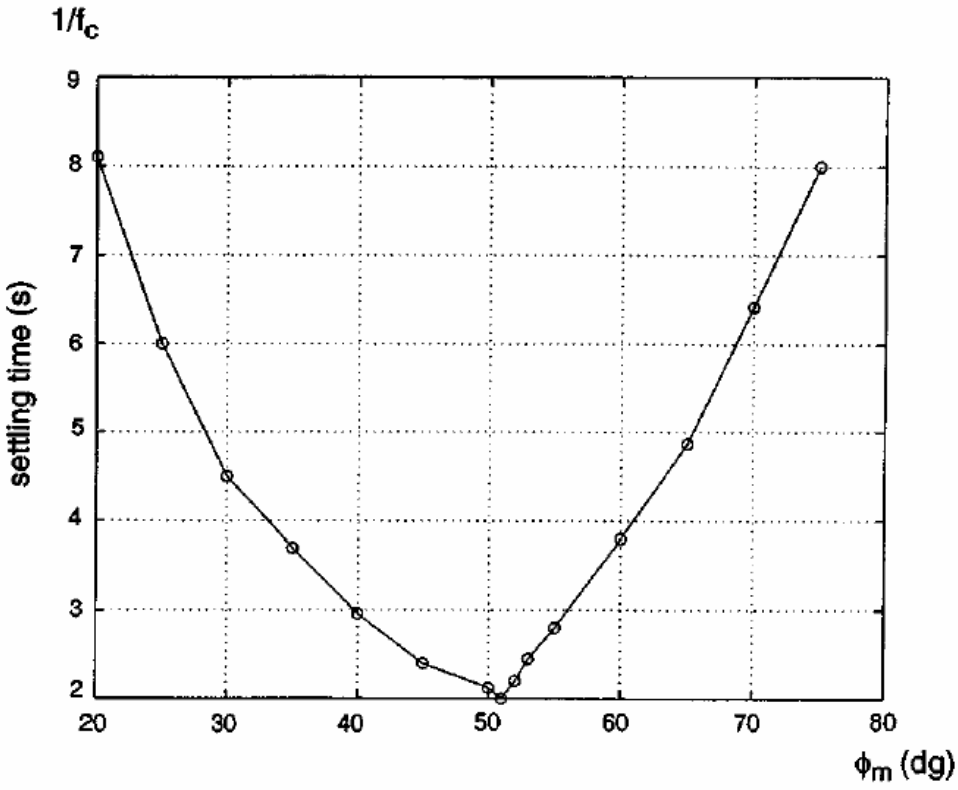



Fig. 4. Setting time as function of the phase margin for $f_{error}/f_{step} = e^{-10}$.

(ref. C. Vaucher, op. cit.)

The settling time reaches a sharp minimum at about 51 degree PM. This is the phase margin just below the point at which the closed loop poles are coincident at $-f_C$. [1] Thus, the design of critically damped loops, a PM of about 70 degrees, does not lead to the fastest settling time for third order CP PLLs.

**Alternatively:**
Recall that the rate at which a second-order low pass system responds to a step in phase or frequency is given by $e^{-\omega_n \zeta t}$, the envelope of the damped ringing. Vaucher hypothesizes that an effective damping factor, $\zeta_e(\phi_m)$, can be defined from the envelope of the responses in fig. 3(b). Then,

$$\bar{\zeta}_e(\phi_m) = \frac{-\Delta(env(ln(\Delta f(f_c t)/f_{step})))}{\Delta(f_c t)}$$

$$f_C = \frac{1}{t_{lock}\zeta_e(\phi_m)} ln\left(f_{step}/f_{error}\right)$$

$f_{step}$ is the amplitude of the frequency jump
$f_{error}$ is the maximum frequency error at $t_{lock}$

Figure 6 is extracted from Fig. 4. It shows the effective damping factor vs phase margin for $\ln(f_{step}/f_{error}) = -10$.

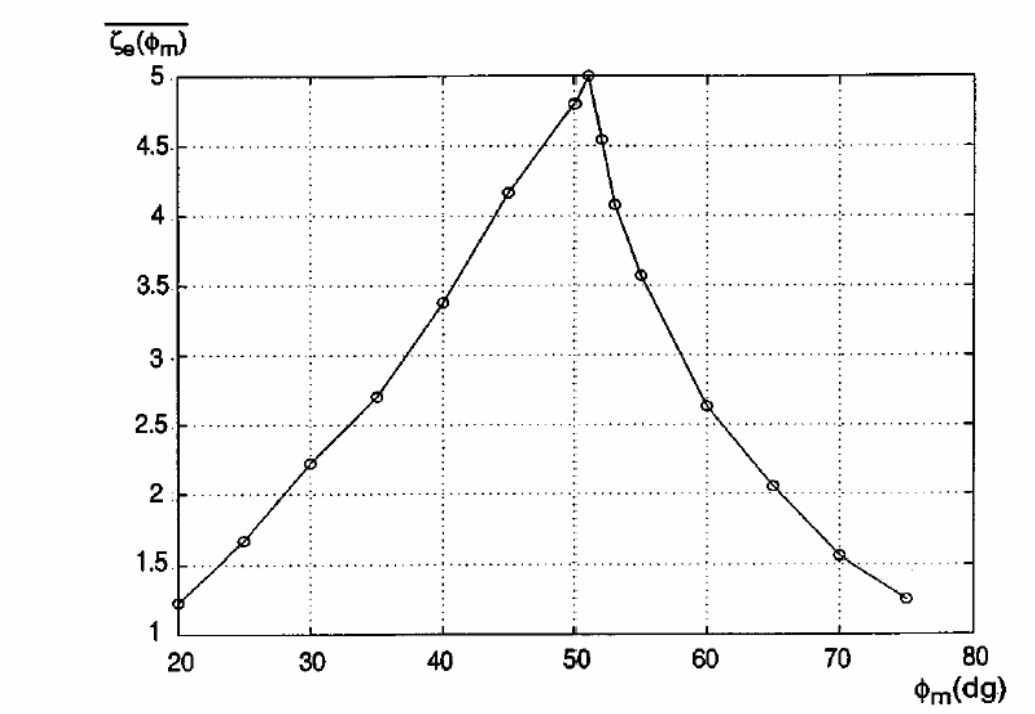



Fig. 6. Average values of $\zeta_e(\phi_m)$ for a $\Delta(\ln(\cdot))$ of ten.

**Design of charge pump PLL.** The equation for loop gain T(s) can be used with the Bode plot to set the crossover frequency and determine k to obtain a particular phase margin. $f_C$ and $\phi_m$ can be determined from the above plots to match a particular settling time specification.

The phase frequency detector (PFD) with single capacitor $C_P$ has

$$\frac{V_{out}(s)}{\Delta\phi} = \frac{I_P}{2\pi C_P s}$$

To find the frequency response of the input current, we note that,

$$I(s) = Vout(s)/Z(s) = Vout(s)/(1/sC_P)$$

where Z(s) is the complex impedance. So, the current source can be modeled as:

$$\frac{I(s)}{\Delta\phi} = \frac{I_P}{2\pi} \quad .$$

Now, let's use this to modify the PFD-CP combination for the third-order loop filter. Multiply the current by the new Z(s):

$$Z(s) = \frac{1}{sC_2} \| \left( R_P + \frac{1}{sC_P} \right) = \frac{1}{C_P + C_2} \frac{(1+s/\omega_z)}{s(1+s/\omega_{p3})}$$

So, the loop gain, T(s),

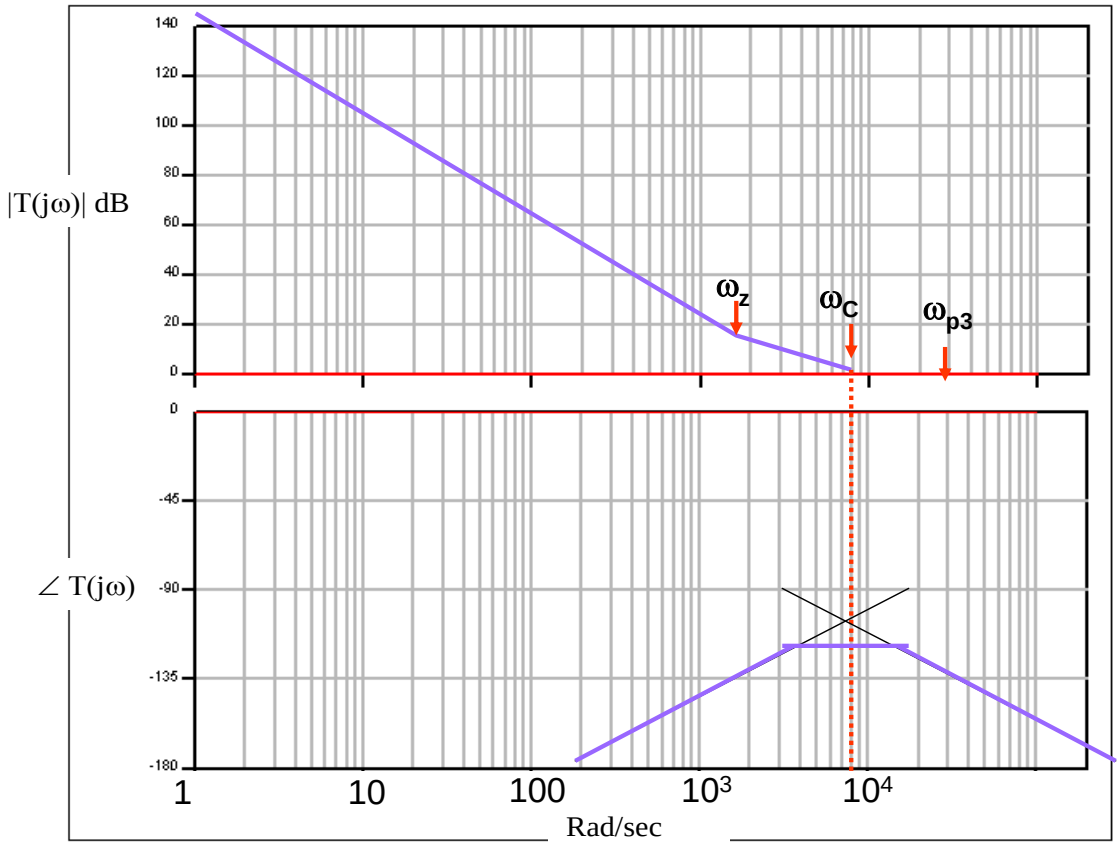
$$T(s) = \frac{I_P K_O}{2\pi N (C_P + C_2) s^2} \frac{(1+s/\omega_z)}{(1+s/\omega_{p3})}$$

Where $\omega_z = 1/R_P C_P$ and $\omega_{p3} = (C_P + C_2)/(R_P C_P C_2)$.

The next step is to determine the zero and third pole frequencies needed to obtain the desired phase margin. One strategy is to choose these frequencies centered around the crossover frequency. The Bode plot can be used to estimate this. We want to choose k such that

$$\omega_z = \omega_c / k$$

$$\omega_{p3} = \omega_c \cdot k$$




Here we see a solution sketched out for k = 4. The factor k can be estimated by[2]

$$k = \left[\frac{1+\sin(\phi_m)}{1-\sin(\phi_m)}\right]^{1/2}$$

[2] D. Shaeffer, Design Criteria for Frequency Synthesis in Wireless Systems, Session F1, Girafe Design Forum, ISSCC 2005.

## Design process:

1. $f_C$ and $\phi_m$ are determined by settling time using the plots from [1].
2. k is derived from $\phi_m$. So, $\omega_z$ and $\omega_{p3}$ are known.
3..At this stage, you can estimate the loop filter components. Here are three ways that give reasonably accurate results. You can later use ADS to optimize from these initial results if they are not sufficiently accurate for your design.

a. First method does not make any assumptions. Start from loop gain.

$$T(s) = \frac{I_P K_O}{2\pi N(C_P + C_2)s^2} \frac{(1 + s/\omega_z)}{(1 + s/\omega_{p3})}$$

Evaluate the magnitude at the crossover frequency. We see that the frequency ratios at crossover are just defined by k. And, at crossover, $|T(j\omega_C)| = 1$

$$|T(j\omega_c)| = \frac{I_P K_O}{2\pi N(C_2 + C_P)\omega_c^2} \frac{\sqrt{1 + (\omega_c/\omega_z)^2}}{\sqrt{1 + (\omega_c/\omega_{p3})^2}} = \frac{I_P K_O}{2\pi N(C_2 + C_P)\omega_c^2} \frac{\sqrt{1 + (k)^2}}{\sqrt{1 + (1/k)^2}} = 1$$

Thus, $C_T = C_2 + C_P$ can be determined. Then,

$$\frac{\omega_{p3}}{\omega_z} = k^2 = \frac{C_2 + C_P}{R_P C_P C_2} \bullet R_P C_P = \frac{C_2 + C_P}{C_2}$$

so,

$$C_2 = \frac{C_2 + C_P}{k^2}$$

and

$$C_P = C_T - C_2$$

and

$$R_P = \frac{1}{\omega_z C_P}$$

b. Another method makes the assumptions that $\omega_z << \omega_C$, $\omega_C << \omega_{p3}$ and $C_P + C_2 \approx C_P$

Start with the magnitude of T(jω).

$$|T(j\omega)| = \frac{I_P K_O}{2\pi N(C_P + C_2)\omega^2} \frac{\sqrt{1+(\omega R_P C_P)^2}}{\sqrt{1+(\omega/\omega_{p3})^2}}$$

Then at crossover, $|T(j\omega_C)| = 1$, so solve for $R_P$.

$$|T(j\omega_C)| \approx \frac{I_P K_O}{2\pi N C_P} \frac{\sqrt{(\omega_C R_P C_P)^2}}{\omega_C^2} \approx \frac{I_P K_O}{2\pi N} \frac{R_P}{\omega_C} = 1$$

Once $R_P$ is known, then $C_P$ and $C_2$ follow from $\omega_z$ and $\omega_{p3}$.

$$\omega_{p3} = \frac{C_P + C_2}{R_P C_P C_2}$$

$$\omega_z = \frac{1}{R_P C_P}$$

$$C_2 = \frac{C_P}{(\omega_{P3}/\omega_z - 1)} = \frac{C_P}{k^2 - 1}$$

OR:

c. Calculate the loop gain at a low enough frequency that both zero and third pole contribution to the magnitude can be ignored. Suppose you set $\omega$ = 1 rad/s. The loop gain can be determined by a Bode plot method, either on the graph or using:

$$\text{dB of } |T(j1)| = 20\log\left(\frac{\omega_C}{\omega_z}\right) + 40\log(\omega_z). \text{ (dB)}$$

Then, convert from dB to a ratio:

$$|T(j1)| = \frac{I_P K_O}{2\pi N(C_P + C_2)}$$

so, $C_P + C_2$ can be determined. Let's call this $C_T$. Then, using, $\omega_z$ and $\omega_{P3}$, then using the equations in part a., $R_P$ and $C_P$ can be found from $\omega_z$ and $C_2$:

$$R_P = \frac{1}{\omega_z (C_T - C_2)}$$

$$C_P = \frac{1}{\omega_z R_P}$$

Implicit in all of this is that you have a specific divide ratio N that you are designing for. In all cases, however, N will vary over some range so that the synthesizer frequency can be tuned. And, over this frequency range, $K_O$ is not constant either. Both of these variations will affect the phase margin and settling time since the loop gain depends on both of these factors.

Your job, then, is to figure out ahead of time which extreme represents the worst case in terms of whatever parameter you are trying to specify: overshoot, spur rejection or settling time. Design for the worst case, and the other extreme will most likely exceed specs.

In the case of the second order loop, the end with the lowest $K_V$ and highest N generally produces the lowest phase margin. Phase margin increases as the crossover frequency increases. $\omega n$ increases, but $\zeta$ also increases. Thus, the settling time must be estimated at both ends and depends on the specific design details. Spur rejection gets worse for higher crossover.

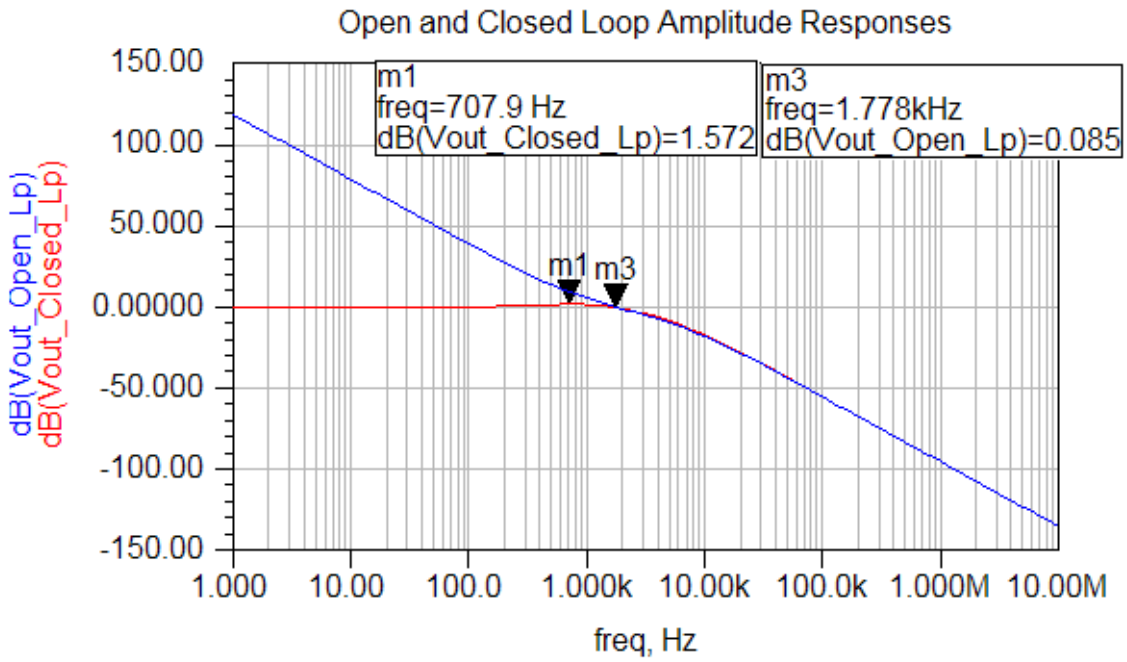
You can estimate the settling time from the exponential behavior of the transient response:

$$e^{-\omega_n \zeta t_S} = \frac{\Delta f}{f_{final}} = fractional\ freq error$$

$$t_s = \frac{-\ln(\Delta f / f_{final})}{\omega_n \zeta}$$

For the third-order PLL, the opposite is true. Phase margin, overshoot and spur rejection get worse as the crossover frequency increases. Analysis is more difficult, but a Bode plot can be used to estimate the crossover frequency and phase margin. Settling response can be estimated from the normalized curves. ADS or MATLAB simulation should be used to verify the results.

**Reference spur rejection.** Refer to the magnitude Bode plot below.




The slope approaching and leaving the crossover region is – 40 dB/decade because:

1. Type 2 loop gain function has a factor of $1/s^2$. However,
2. The zero reduces slope to – 20 dB/decade in the crossover region, but because the reference frequency must be at least 10 times $f_C$, the slope again approaches -40 dB when the third pole kicks in.

So, depending on the relationship between the reference and crossover frequencies, we can predict the spur rejection based upon either a – 20 or -40 dB/decade extrapolation. From the Bode plot, you can see that the closed loop gain is the same as open loop gain after crossover. The gain at crossover is 0 dB, so anything beyond that frequency will be attenuated as shown.

**Example:** suppose the reference frequency is 100 KHz. Crossover is about 2 kHz in this example. We can see that the graph predicts – 60 dB of attenuation for 100 kHz signals.

Or, estimate from the equation below:

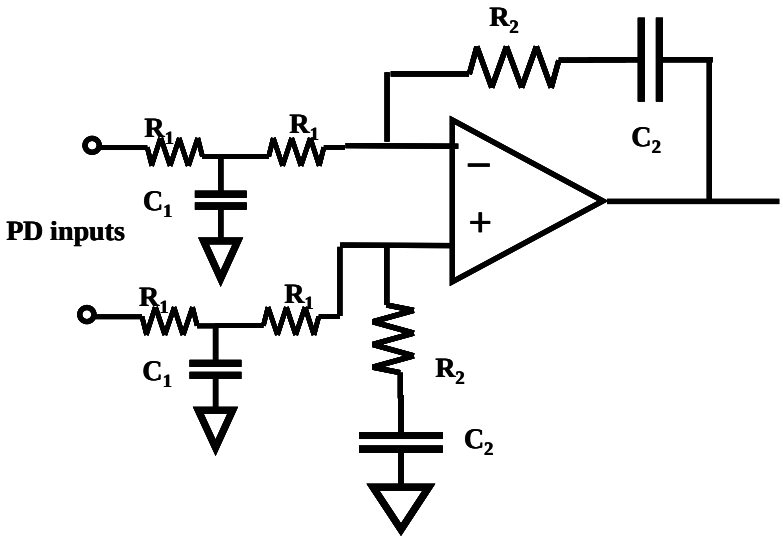
$$SR \cong 20\log\left(\frac{f_{P3}}{f_C}\right) + 40\log\left(\frac{f_{ref}}{f_{P3}}\right)$$

## OpAmp Loop Filter Version

The charge pump solution, although quite popular, is not the only possibility. You can also produce the Type 2, third-order loop gain function using the opamp style loop filter shown below. Capacitor $C_1$ gives the third pole in this case.

$$\omega_Z = \frac{1}{R_2 C_2}$$

$$\omega_{p3} = \frac{2}{R_1 C_1}$$



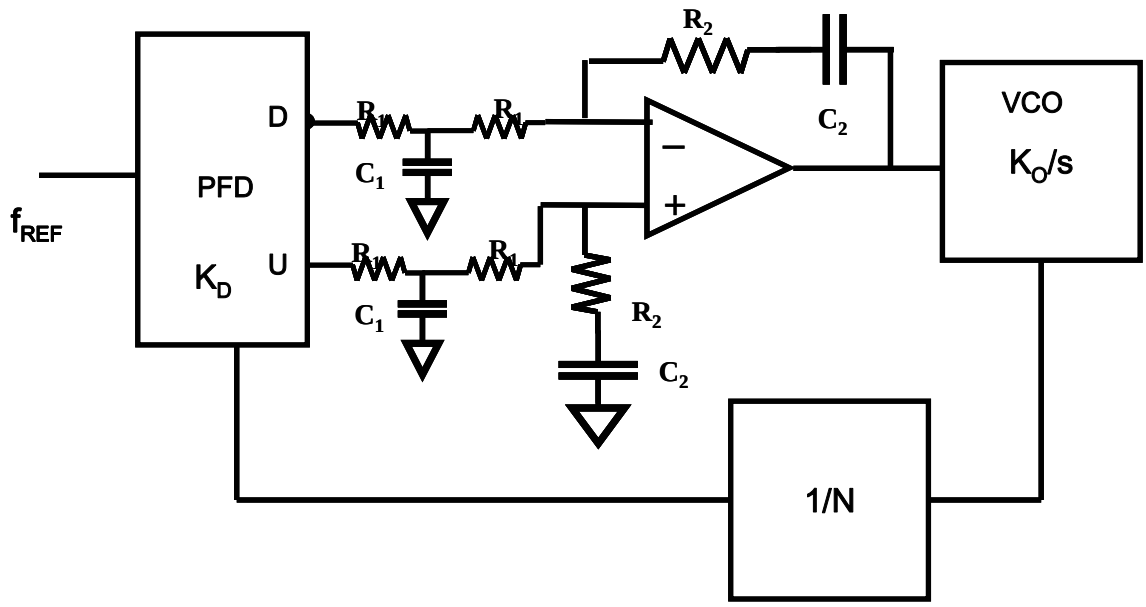

Because the phase-frequency detector has limited current output capability, you need to make sure that R1 is sufficiently large so that this current is not exceeded, otherwise the filter will not work correctly. In deriving the transfer function, F(s), you should note that only one input at a time is being driven. The PFD output gives either UP or DOWN pulses (neglecting the very narrow pulses produced at both outputs when the loop is locked) if the phase is lagging or leading respectively.

$$F(s) = \frac{(1 + s/\omega_z)}{2sC_2R_1(1 + s/\omega_{P3})}$$

The block diagram of the PLL with opamp filter is shown below. From the diagram, T(s) can be seen to be:

$$T(s) = \frac{K_D K_O}{2NC_2R_1s^2} \frac{(1 + s/\omega_z)}{(1 + s/\omega_{P3})}$$

Then the design can proceed in a similar manner as with the charge pump if phase margin and settling time are known.




$$|T(j\omega_c)| = \frac{I_P K_O}{2NC_2R_1\omega_c^2}\frac{\sqrt{1+(\omega_c/\omega_z)^2}}{\sqrt{1+(\omega_{p3}/\omega_c)^2}} = \frac{I_P K_O}{2NC_2R_1\omega_c^2}\frac{\sqrt{1+(k)^2}}{\sqrt{1+(1/k)^2}} = 1$$

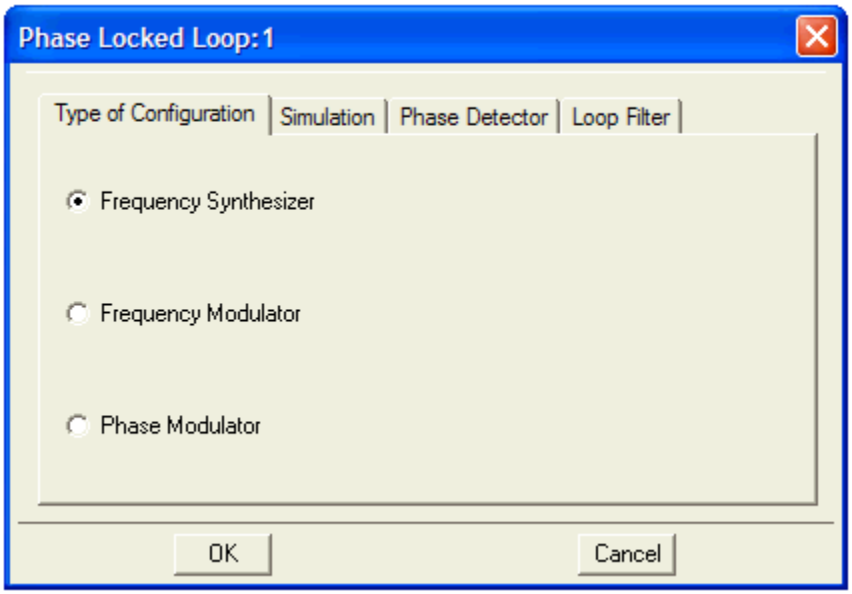
R1 is known from the phase frequency detector maximum current limitation.

So, solve for $C_2$. Then,

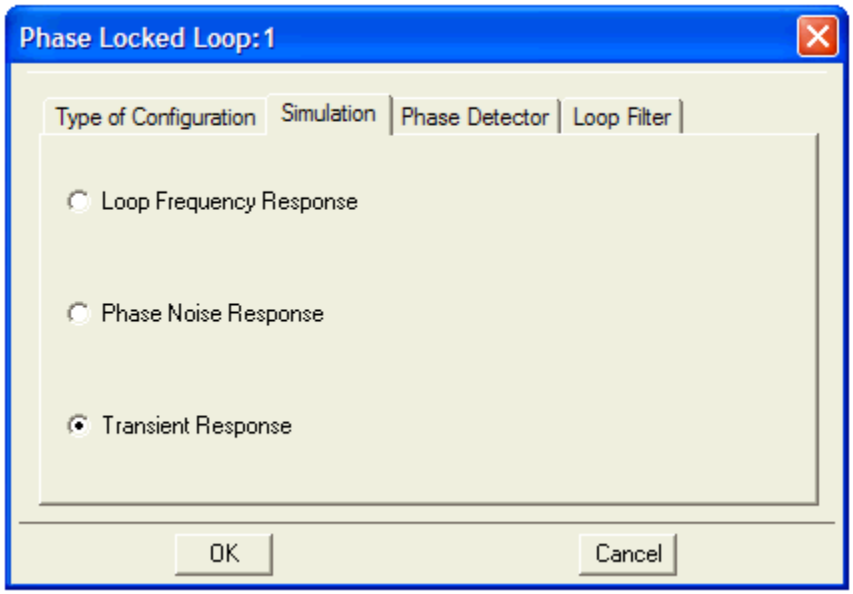
$$R_2 = \frac{1}{\omega_z C_2}$$

$$C_1 = \frac{2}{\omega_{p3} R_1}$$

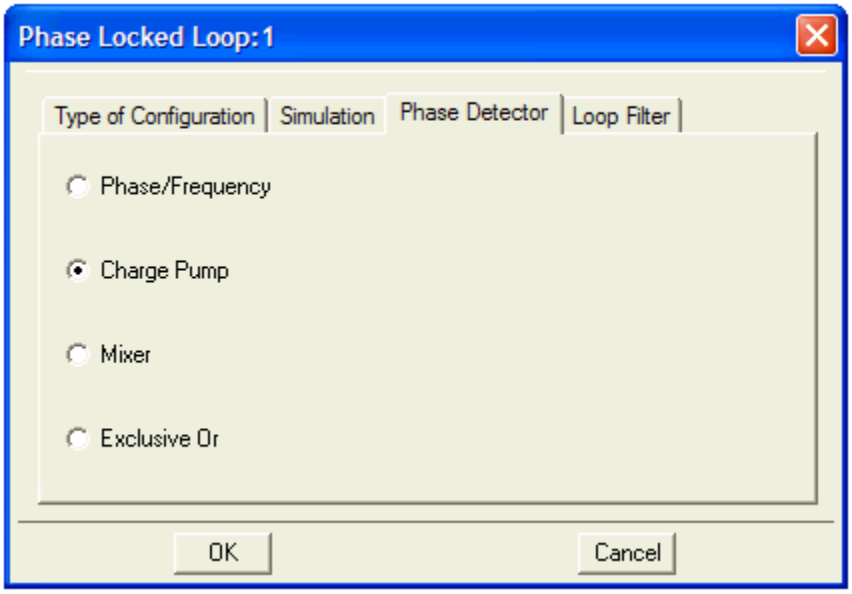
**Simulation tool:** You can verify your design using the ADS PLL design guide.



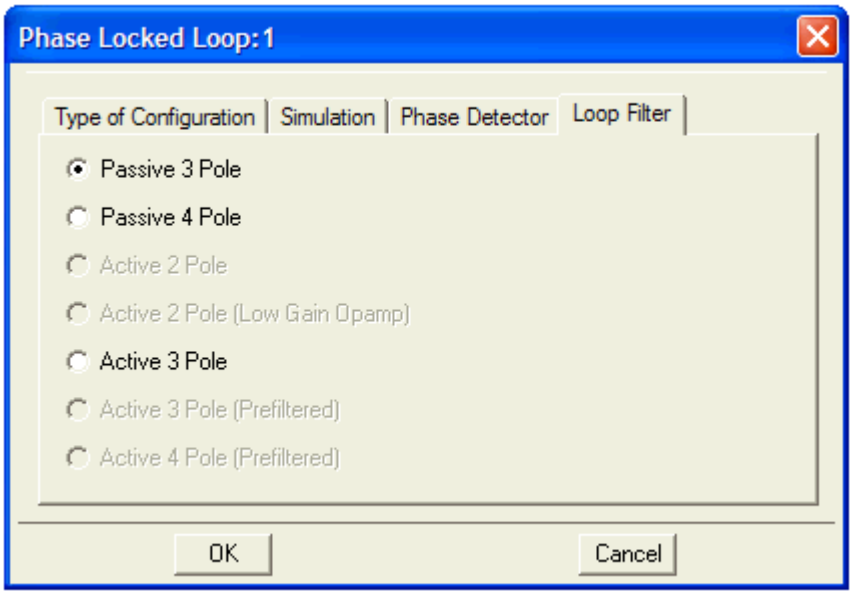

1. The first step is to select the PLL design guide from the DesignGuide menu. Then select the application, in this example, Frequency Synthesizer.




2. Next, specify which type of simulation you wish to perform.



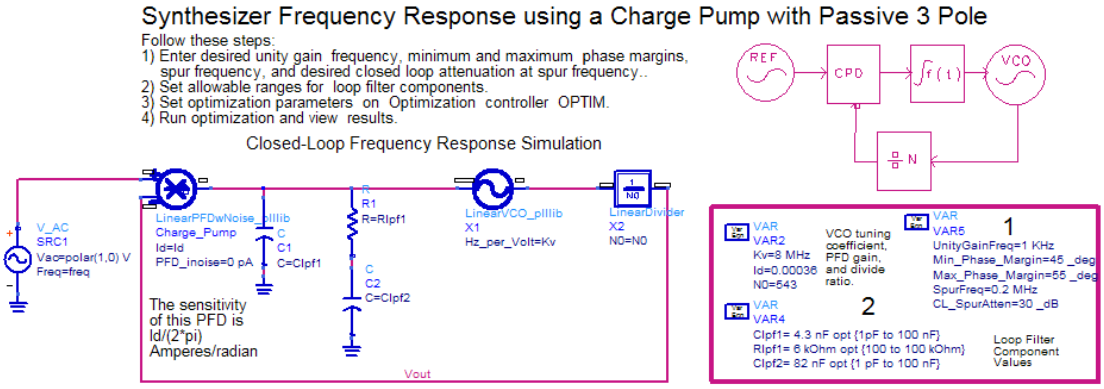

3. The type of phase detector being used must be selected.

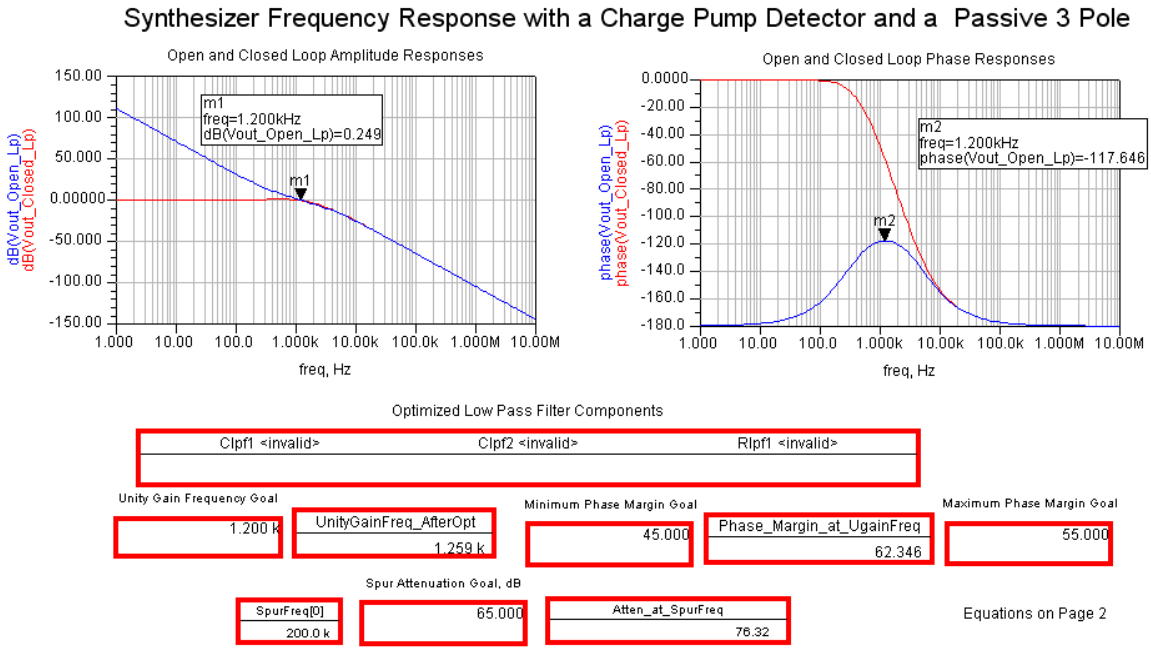



4. Finally, select the filter type. The $R_P C_P C_2$ combination is a passive 3 pole, of course.

The frequency response simulation mode uses the AC analysis method. It plots a Bode plot of the open and closed loop gain. Component values can be optimized.

You will need to specify your reference frequency, charge pump current, the divide ratio, and your VCO tuning coefficient. Enter the corresponding filter component values. To evaluate your calculated component values, you should disable the optimization controller. Then, the Bode plot that is produced will reflect your choice of components. You can refine the solution later by using the optimization feature.

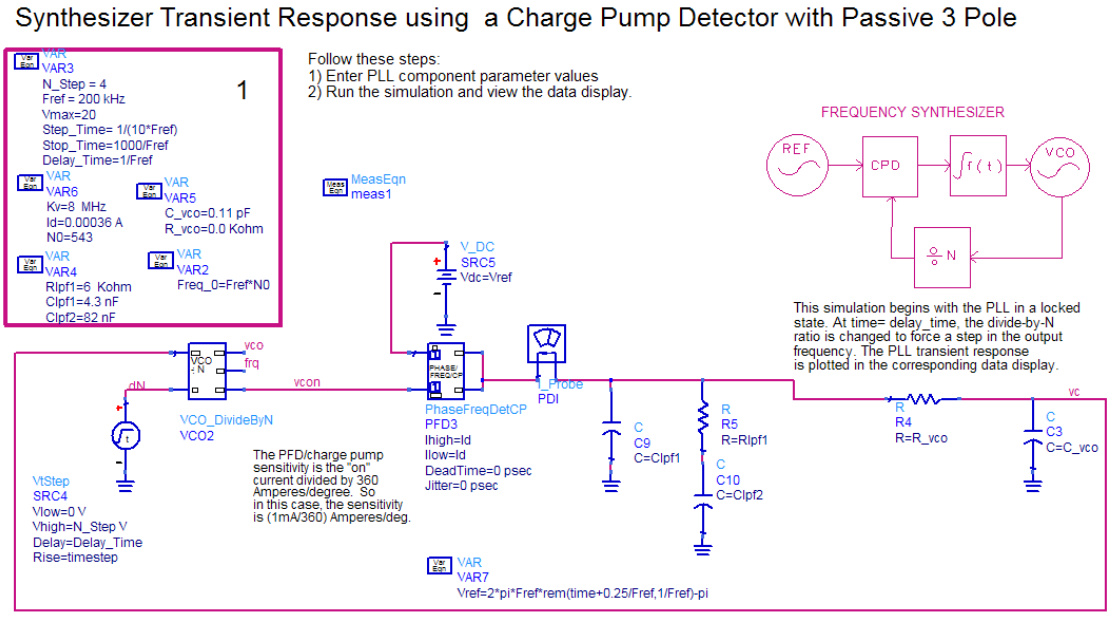


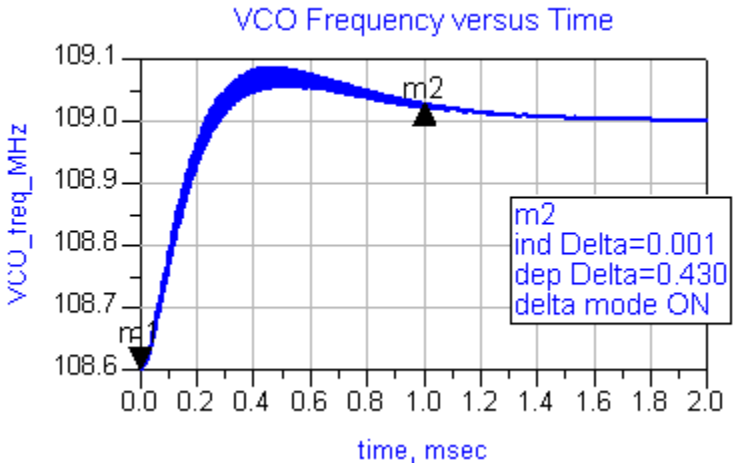




With optimization disabled, the lowpass filter component values are not displayed, but crossover frequency, phase margin and spur attenuation are calculated.

When you optimize, then specify the desired crossover frequency and phase margin. But, start from the component values you have already selected to obtain a solution that is closer to optimum. The optimizer does not generate a unique solution, and the closer the initial values are to your goal, the more useful the result.

A transient simulation can also be used to verify settling time.




Note the components on the far right, R4 and C3. These model the input to your VCO. If C3 is large, it will produce a 4$^{th}$ pole that could badly affect your step response. Be sure that the VCO does not have any large filtering capacitors at the tuning port.