A 2.4GHz SiGe Low Phase-Noise VCO Using On Chip Tapped inductor

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Abstract:

An on-chip tapped inductor technique is shown to be an efficient method for reducing oscillator phase noise. Higher signal amplitude can be achieved while avoiding breakdown and without penalty in area or tuning range. A commercial SiGe BJT process was used to fabricate the 2.4GHz VCO. The measured phase noise at 1MHz offset frequency is -128 dBc/Hz with 23% tuning range. The VCO dissipates 16.5mA at a 2.5V supply voltage.

1. Introduction

The requirement of phase noise in integrated oscillators has been driven by wireless applications. In addition, cost concerns require that the chip area should be as small as possible. In order to achieve the phase noise requirement and smaller chip area, the signal amplitude has to be maximized.

In a recent paper, it [1] states that Lesson's hypothesized equation

$$L(\omega_m) = \frac{4FkTR_p}{V^2{}_{rms}}\left(\frac{\omega_o}{2Q\omega_m}\right)^2 \qquad (1)$$

holds and the oscillator's noise factor F of a current-biased differential LC oscillator as shown in Fig. 1 is

$$F = 1 + \frac{4\gamma I_{bias}R_p}{\pi\sqrt{2}V_{rms}} + \gamma\frac{4}{9}gm_{bias}R_p \qquad (2)$$

where Vrms is the rms oscillation amplitude, I_{bias} is the bias current, γ is the FET noise factor (2/3 for long channels), R_p is the equivalent parallel resistance of the resonator and gmbias is the gm of the FET current source. The first term in (2) is the noise contributed by R_p. The second term is the phase noise induced by differential pair thermal noise and is independent of the specifics of the transistors. The last term is the noise contributed by the current source. Equation (1) and (2) show that the relative contribution of the resonator loss is fixed. In the current-limited regime, where the FET current source remains in saturation, the oscillation amplitude Vrms is proportional to $I_{bias}R_p$, so the differential pair contributes noise proportional to γ. The last term in equation (2) is proportional to gm of the current source. The same equation can be applied to a BJT LC oscillator with a different γ.

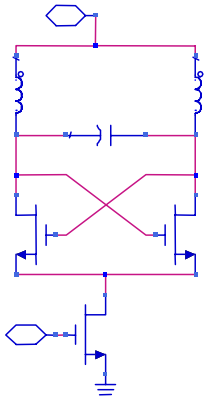

Figure 1. Current-biased differential LC oscillator

Suppose that the current source contribution is removed from equation (2), then the phase noise will be proportional to

$$L(\omega_m) \propto \frac{1}{I_{bias}{}^2 R_p Q^2} \qquad (3)$$

and the oscillator can be designed for least phase noise by increasing $I_{bias,}$ R_p and Q.

However, the signal amplitude $I_{bias}R_p$ is constrained by breakdown mechanisms in the devices and the supply voltage. Equation (3) shows that phase noise can still be reduced if I_{bias} is increased while $I_{bias}R_p$ is kept constant. For example, if Rp is reduced by half, the maximum I_{bias} can be increased 2 times, so $L(w_m)$ will be reduced by 3dB according to equation (3) if Q does not change much. In 2.4GHz frequency range, the major contribution of the resonator loss is from the inductor. A smaller Rp means a smaller inductor. As far as area is concerned, a smaller inductor is preferable. But Rp cannot be too small, since Q will drop. An optimisation procedure is needed to find the optimum inductor for lowest phase noise under the requirement of chip area, voltage supply and tuning range.

If a better phase noise is needed, several identical oscillators can be coupled to each other, the phase noise will be reduced by a factor of 1/(number of oscillators coupled)[3]. But the chip area will be increased. In this paper, a tapped inductor approach is presented which can further reduce the phase noise under the same chip area, breakdown and voltage supply constraint as the normal LC oscillator shown in Fig. 1.

2. Circuit Design

In order to reduce the phase noise of the oscillator, a large output swing of the resonant tank is needed, but the large voltage swing will easily move the transistor into its breakdown region. Therefore, the Vce breakdown voltage will also limit the reduction of phase noise. In order to preserve the resonator voltage swing, an inductor tapping technique is used.

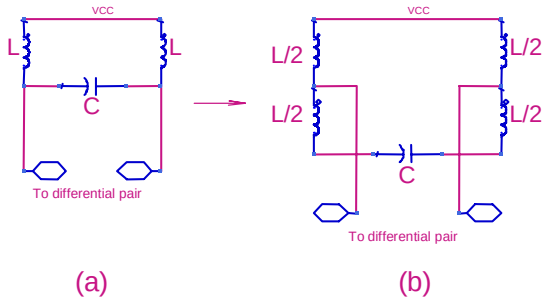

Figure 2(a) LC resonator (b) a tapped inductor capacitor resonator

Fig. 2 shows the LC resonator transformed into a tapped resonator. The same inductor and capacitor are used. Since the dominant loss of the resonator is the inductor, the Q of the resonator will not be changed but the Rp, which is the equivalent input impedance looking from the differential pair, is reduced by 1/(tapping ratio)^2, which is ¼ in Fig. 2. Then four times more current can be drawn into the oscillator to maintain the same output amplitude at the differential pair. The amplitude of the resonator will be double which allow more energy to be stored in the tank, so it reduces phase noise. Moreover from equation (2), the 4 times larger gm noise contribution from the tail current source, if BJT is used, will be scaled 4 times smaller by the smaller (Rp/4). Therefore, the total noise contribution from the tail current source remains the same. The phase noise will be reduced by 6dB using 1 to 1 tapping ratio as estimated from equation (2) and (3). Besides, the inductor tapping can also increase the output impedance of the transistor, so the loading due to the transistor is reduced. Also the tuning range of the tapped inductor VCO is the same as a normal LC VCO, since four times larger current is drawn, four times larger parasitic capacitance is introduced by the four times larger differential pair, but only ¼ of the parasitic capacitor will load the resonator due to the inductor transformer. A comparison of coupled oscillator and tapped oscillator to a basic LC oscillator is given in Table 1.

	LC	Couple	Tapping
Voltage swing at the differential pair	1x	1x	1x
Tuning range	1x	1x	1x
Supply voltage	1x	1x	1x
Current bias	1x	4x	4x
Chip Area	1x	4x	1x
Phase noise	0dB	-6dB	-6dB

Table 1. Comparison of coupling oscillator and tapping oscillator reference to LC oscillator

From equation (2), the tail current source may have a large impact on the generation of phase noise, often being the largest contributor[4]. The effect of the tail current noise can be reduced only by reducing its gm. For mos, this implies an increase of transistor over-drive, and consequently an increase of the minimum drain-source voltage for the tail transistor to act as a current source. For BJT, a resistor is added to the emitter to reduce its gm. Both schemes will limit the maximum voltage amplitude of the oscillations, and cause a net increase of the phase noise. According to [1], the major noise frequency at the current source is the 2nd harmonic to the oscillation frequency, so a capacitor is used to filter the 2nd harmonic noise frequency by connecting it to the collector of the current source. Reference [2] has suggested that an extra filter is needed for the current source to provide high impedance to the even harmonics of the oscillator frequency in order to stop the differential pair FET in triode region from loading the resonator. But it is not applicable to BJT switch pair since when the BJT is driven into saturation, the base collector junction will turn on which will start to load the resonator even when a high impedance current source is present. Therefore, the filter is not implemented. The remedy is not to drive the BJT switch pair to saturation.

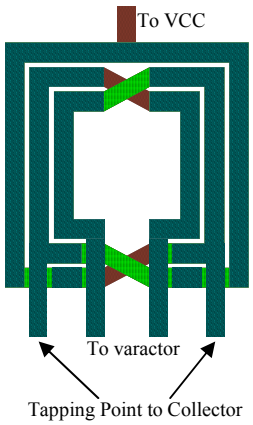

Figure 3. Layout of the tapped inductor

A three turn square center-tapped inductor, as shown in Figure 3, with 2 additional tap points has been designed using the Agilent Momentum EM simulator. The size of the inductor is 250x250 um^2 and the inductance is designed to be 2.3nH. The tapped points are designed to have a voltage divide ratio around 1:1 which is optimised for phase noise and layout. The choice of the 1:1 tapping ratio is a compromise. A larger

ratio would achieve a larger tank voltage, but the ratio cannot be set too large. If it is too large, parasitic oscillation will occur. Besides, if the ratio is too large, it is difficult to layout the inductor. Therefore, a 1 to 1 ratio is used, as determined through simulation.

In order to reduce the phase noise, the voltage swing of the tank should be as large as possible but it is limited by the Vce breakdown of the device. Since the voltage swing of the tank is proportional to I_{bias}, I_{bias} is set to a value for the maximum Vce of the transistor.

Two varactors connected in back-to-back are used for frequency tuning. The varactor diode is an NPN collector-base junction with a hyperabrupt collector doping profile.

One common collector stage is used as buffer. To minimize the loading from the buffer, the capacitor autotransformer is used to increase the input impedance of the buffer. This buffer can directly drive the off-chip 50ohm load. The complete VCO circuit diagram is shown in Figure 4.

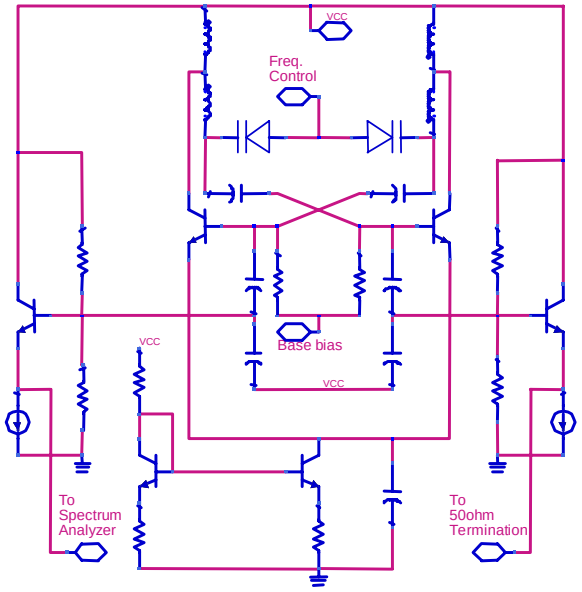

Figure 4. Complete VCO Circuit diagram

3. Measurement Results

The circuit is fabricated in a SiGe process from Maxim Integrated Products. Since the tapped inductor technique is also suitable for low voltage operation, different supply voltages are used to test the circuit. Agilent E4440A with phase noise option is used to measure the phase noise of the oscillator. The phase noise plots are shown in Fig. 5. Measurements give a quality factor for the whole LC-tank of about 7 at 2.4GHz. In Fig. 6 the frequency versus control voltage yielding a tuning range of 23% under 2.5V supply is presented. The variation of phase noise under different supply voltages across the tuning range is shown in Fig. 7. The die photo in Fig. 8 shows that the VCO area is 590um x 350um. A summary of the performance is given in Table 2.

Vcc (V)	2.5	1.8	1.5
Core current bias (mA)	16.5	11	5.5
Tuning range (%)	23	17.3	16
Phase noise @1MHz (dBc/Hz)	-128	-125.5	-121

Table 2 Summary of Measured VCO Performance

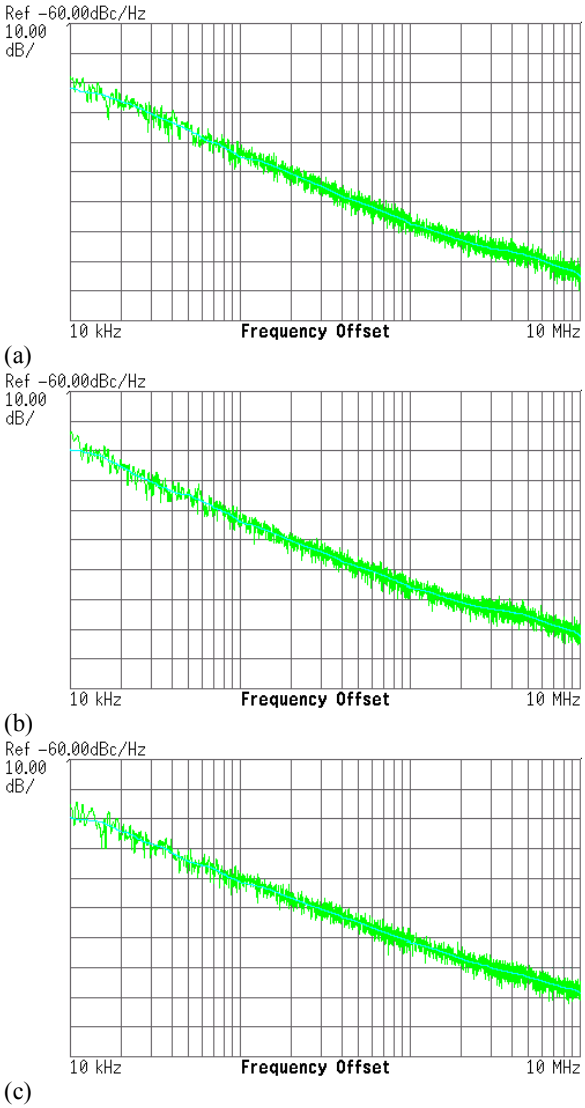

Figure 5. Measured phase noise @1MHz offset at 2.6GHz with different supply voltage (a) 2.5V, (b) 1.8V, and (c) 1.5V

Table 3 compares these oscillators with some other oscillators published in literature. A commonly accepted quantity used for comparing various oscillators is the figure of merit (FOM) that is defined as below

$$FOM = 10\log\left(\frac{f_o}{f_{off}}\right)^2 \frac{1}{P} - L(f_{off})dB \qquad (4)$$

where P is the power dissipation of the oscillator in milliwatts, f_o is the center frequency, f_{off} is the frequency offset from the center, and $L(f_{off})$ is the phase noise measured at f_{off} offset frequency.

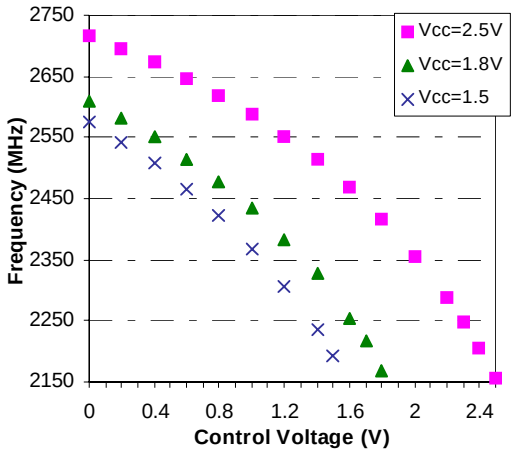

Figure 6. Frequency versus Control voltage

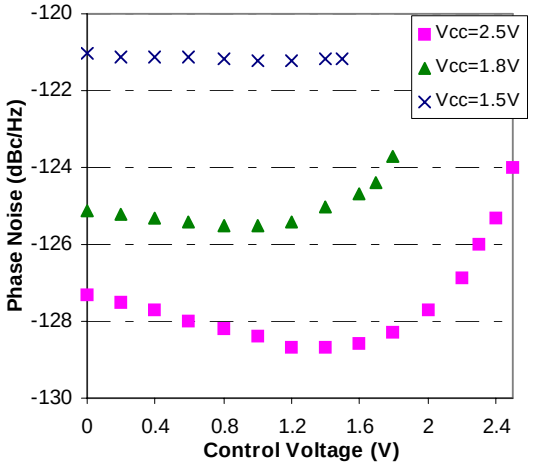

Figure 7. Phase noise @1MHz offset versus Control voltage

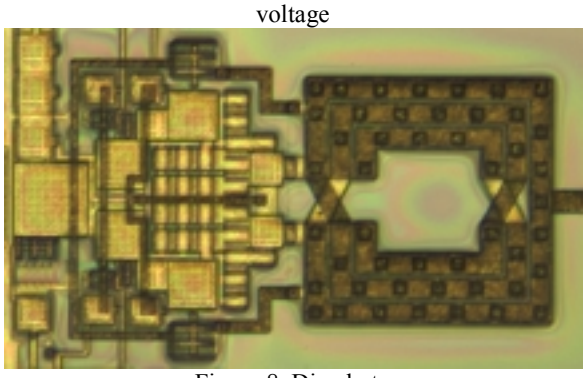

Figure 8. Die photo

It is shown that our oscillators give better phase noise performance than those previously published in literature at 2.4GHz range. Besides, a wide tuning range is also achieved. A better FOM can be achieved if the tuning range is reduced since less noise will be injected from the varactors.

Ref.	Freq GHz	Tun %	PN@ 1MHz	Vcc (V)	Cur. (mA)	FOM
*	2.4	23	-128	2.5	16.5	179.5
*	2.4	17	-125.5	1.8	11	180
*	2.4	16	-121	1.5	5.5	179.4
5	2.4	21	-119	3	6	174
6	2.6	26	-119.4	2.5	4	177.7
7	2.56	20	-124	2	7	181
8	2.4	11	-123	2.5	1.5	185
9	2.4	15	-119	1.8	1	184

Table 3. VCO Performance Comparison
*this work

4. Conclusion

One of the most efficient methods of reducing phase noise is to increase the signal amplitude in the resonator. However, the maximum resonator signal amplitude is limited by breakdown mechanisms in the devices and supply voltage. A tapped inductor technique is introduced to allow a higher swing in the tank in order to reduce the phase noise. This technique uses the same area as the normal LC oscillator.

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