An Adaptive PLL Tuning System Architecture Combining High Spectral Purity and Fast Settling Time

Cicero S. Vaucher, *Member, IEEE*

***Abstract*—An adaptive phase-locked loop (PLL) architecture for high-performance tuning systems is described. The architecture combines contradictory requirements posed by different performance aspects. Adaptation of loop parameters occurs continuously, without switching of loop filter components, and without interaction from outside of the tuning system. The relationship of performance aspects (settling time, phase noise, and spurious signals) to design variables (loop bandwidth, phase margin, and loop filter attenuation at the reference frequency) are presented, and the basic tradeoffs of the new concept are discussed. A circuit implementation of the adaptive PLL, optimized for use in a multiband (global) car-radio tuner IC, is described in detail. The realized tuning system achieved state-of-the-art settling time and spectral purity performance in its class (integer-N PLL's): a signal-to-noise ratio of 65 dB, a 100-kHz spurious reference breakthrough signal under −81 dBc, and a residual settling error of 3 kHz after 1 ms, for a 20-MHz frequency step. It simultaneously fulfills the speed requirements for inaudible frequency hopping and the heavy signal-to-noise ratio specification of 64 dB.**

***Index Terms*—Adaptive systems, FM noise, frequency synthesizers, phase-locked loops.**

I. Introduction

FAST settling time–frequency synthesizers are essential building blocks of modern communication systems. Typical examples are digital cellular mobile systems, which employ a combination of time-division duplex (TDD) and frequency-division duplex (FDD) techniques. In these systems, the downlink frequencies (base station to handsets) are placed in different bands with respect to uplink frequencies. In order to save cost and decrease the size of the handset, it is desirable to use the same frequency synthesizer to generate uplink and downlink frequencies. Requirements are that the synthesizer has to switch between bands and settle to another frequency within a predetermined time (>1.7 ms for GSM and DCS-1800 systems [1]).

Car-radio receivers with optimal radio data system (RDS) performance ask for fast-settling-time tuning systems as well [2]. The RDS network transmits a list of (nationwide) alternative frequencies carrying the same program. The tuner performs a background scanning of these frequencies, so that optimum reception condition is provided when the receiver is displaced within different coverage regions. For the system to be effective, the background scanning has to be performed in a transparent (inaudible) way to the listener. A possible but expensive way to do that is to use two tuners in the receiver, with one of them being used for checking on alternative frequencies only. Single-tuner solutions—which have a much better price/performance ratio—require a tuning system architecture able to do frequency hopping in an inaudible way [2]. In other words, a fast-settling-time architecture is required for these applications.

Communication systems often pose severe requirements on the spectral purity of the tuning system local oscillator (LO) signal. There are two main reasons for this. First, to avoid problems with reciprocal mixing of adjacent channels. Reciprocal mixing decreases the receiver's selectivity and disturbs the reception of weak signals. Second, because the mixing process, which is used for down-conversion of the radio-frequency (RF) signals, superposes the phase noise of the LO on the modulation of the RF signal. Hence, the signal-to-noise ratio (SNR) at the output of the demodulator is a function of LO's phase noise level [3].

This paper describes an adaptive tuning system architecture that combines fast settling time with excellent spectral purity performance. The architecture was optimized to be used in a global car-radio tuner IC with inaudible RDS background scanning. The integer-N frequency synthesizer has an SNR of 65 dB and a 100-kHz spurious reference breakthrough under −81 dBc at the voltage-controlled oscillator (VCO) (−87 dBc at the mixer). Residual settling error for a 20-MHz frequency step is 3 kHz after 1 ms. These results are similar to those of a fractional-N implementation [4]. The complexity of our tuning system, however, is much smaller. The adaptive phase-locked loop (PLL) was integrated in a 5-GHz, 2-μm bipolar technology. The tuning system works with 8.5-V supply voltage for the charge pumps and with 5 V for the logic functions. Total current consumption is 21 mA from the 5-V supply and 12 mA from the 8.5-V supply.

The architecture of the multiband tuner IC is described in Section II. Section III presents relationships of settling time, phase noise, and spurious signals to the design variables, namely loop bandwidth, phase margin, and loop filter attenuation at the reference frequencies. Section IV introduces the adaptive PLL architecture and discusses the advantages and tradeoffs of the concept. Section V describes the circuit implementation, and Section VI presents a summary of measured results.

Manuscript received July 23, 1999; revised November 29, 1999.

The author is with Philips Research Laboratories, Eindhoven 5656 AA The Netherlands (e-mail: Cicero.Vaucher@philips.com).

Publisher Item Identifier S 0018-9200(00)02861-4.

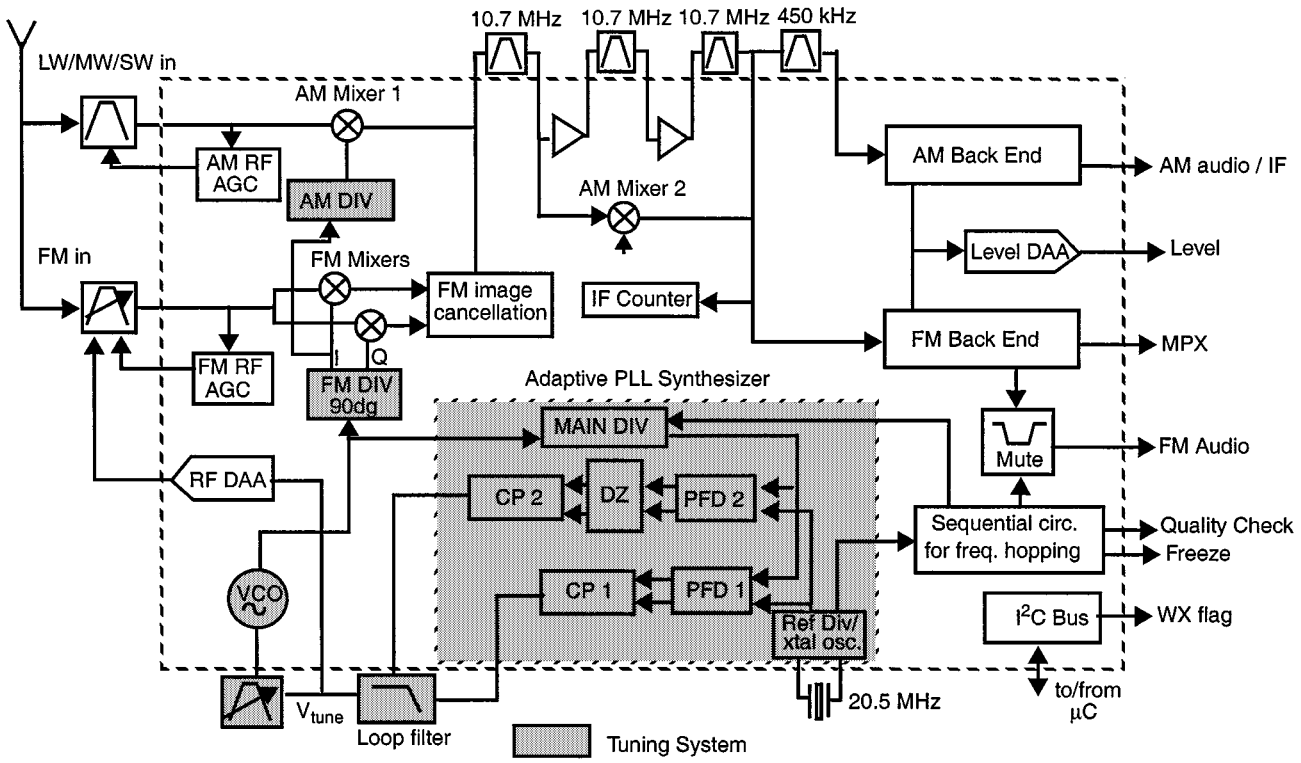


Fig. 1. Simplified block diagram of the global car-radio tuner IC.

TABLE I
RECEPTION BANDS WITH CORRESPONDING TUNING SYSTEM PARAMETERS

Band	Fant (MHz)	Fvco [151-248] (MHz)	FM DIV	AM DIV	Fref PLL (kHz)	tuning step size (kHz)
LW / MW (Eur+USA)	0.144 1.710	216.88 248.20	2	10	20	1
SW	5.85 9.99	165.5 206.9	2	5	10	1
Weather B. (USA WX)	162.40 162.55	173.10 173.25	1		25	25
FM (East Eur)	65 74	151.4 169.4	2		20	10
FM (Japan)	76 90	173.4 201.4	2		100	50
FM (Eur+USA)	87.5 108	196.4 237.4	2		100	50

II. MULTIBAND TUNER ARCHITECTURE

The block diagram of the global tuner IC with inaudible background scanning is shown in Fig. 1. The receiver and tuning system architectures have been defined such that all reception bands can be accessed with a single VCO and a single loop filter, without changes to the application. Mapping the frequency of the VCO to the different input bands is achieved by dividing its output frequency by different ratios, depending on the band to be received. The division is accomplished in the FM DIV and AM DIV dividers, which are set in between the VCO output and the RF mixers. Table I presents the VCO frequency and tuning system parameter settings for various reception bands, including the American Weather Band. By dividing the VCO output, the tuning resolution is 1 kHz in AM mode and 50 kHz in FM mode, despite the fact that reference frequencies are 20 kHz and 100 kHz, respectively.

Combining the different reception bands in one single application—the same VCO and same loop filter—complicates the design of the tuning system. A reception band with worst case

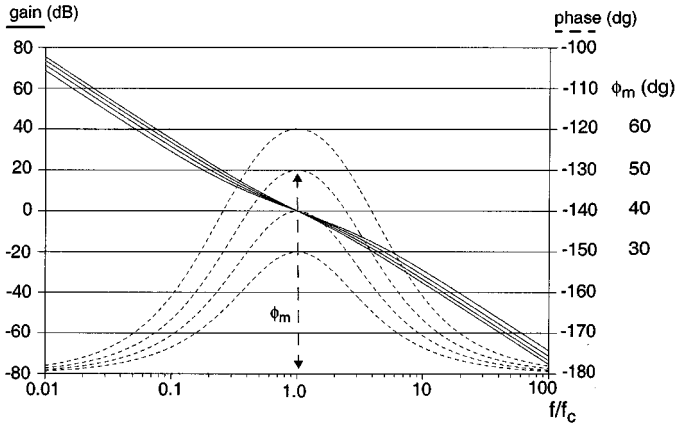


Fig. 2. Open-loop frequency response (Bode plot) of a type-2, third-order charge-pump PLL for different values of phase margin ϕ_m.

spectral purity requirements determines the loop filter design. Nonetheless, robustness for variations in tuning system parameters, for all reception bands, has to be insured. The relationships between different performance aspects on system level are discussed in the following section.

III. Settling Time and Spectral Purity Performance

The properties of a PLL are strongly related to its phase detector implementation [5]. Present-day PLL frequency synthesizers usually employ the tristate, sequential phase frequency detector (PFD), combined with a charge pump (CP) [6]. The analysis of the PLL properties presented in this paper assumes the use of a PFD/CP in the loop.

A. Settling Time, Loop Bandwidth, and Loop Phase Margin

Bode diagrams are a powerful tool for designing PLL tuning systems [7], [8] because they enable direct assessment of the loop's phase margin (ϕ_m) and open-loop bandwidth (0-dB frequency f_c). Accurate and reliable results for f_c and ϕ_m are obtained with ease to implement behavioral models [9] and with fast ac simulation runs. In spite of the advantages of the "ac method," design equations relating the settling performance of a type-2, third-order charge-pump PLL[1] [6] to its open-loop bandwidth and phase margin have, to the best of our knowledge, not yet been published in the open literature.

Fig. 2 presents Bode plots of a type-2, third-order loop for different values of phase margin ϕ_m. Fig. 3(a) displays the transient response of such a loop for three different values of phase margin. The responses are plotted as $\Delta f(f_c t)/f_{\rm step}$, normalized for $f_c t$. $\Delta f(t)$ is the remaining frequency error with respect to the final value and $f_{\rm step}$ is the amplitude of the frequency jump. Fig. 3(b) presents the responses as $\ln(|\Delta f(f_c t)|/f_{\rm step})$, so that the impact of ϕ_m on the "long-term" transient response is easily observed.

The influence of the phase margin on the settling time, obtained with transient simulations similar to those of Fig. 3, is presented in Fig. 4. The figure shows the time necessary for the value of $\ln(|\Delta f(f_c t)|/f_{\rm step})$ to reach a numerical value of -10. The settling time decreases with increasing phase margin,

[1]The most widely used configuration in synthesizer applications.

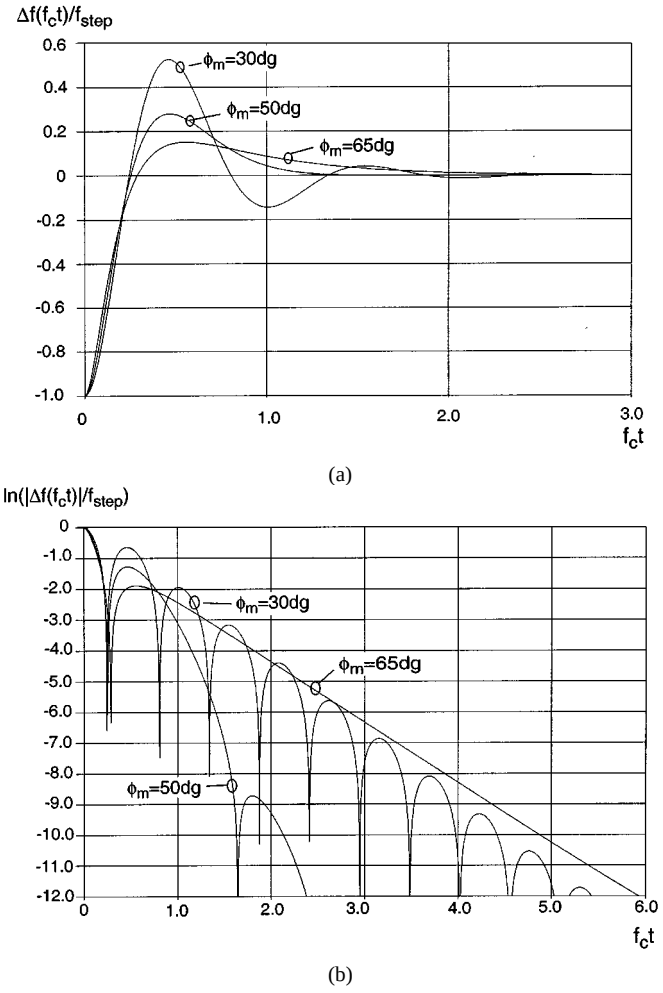


Fig. 3. Setting transient for different values of ϕ_m, normalized for $f_c t$. (a) Setting error (represented as $\Delta f(f_c t)/f_{\rm step}$) versus $f_c t$. (b) Setting error (represented as $\ln(|\Delta f(f_c t)|/f_{\rm step})$) versus $f_c t$.

reaching a minimum for ϕ_m values of around 50°. Increasing the phase margin further leads to a sharp increase in the settling time.

The relationship of settling time and phase margin, displayed in Fig. 4, can be understood with the help of Fig. 5. It presents the pole and zero locations of the closed-loop transfer function of a third-order loop with different values of phase margin (Bode plots presented in Fig. 2). The real part of the dominant (complex) poles approach $-f_c$ for values of ϕ_m of about 50°. When ϕ_m equals 53°, all three poles lie at $-f_c$. That is the location with the fastest damping of the transient error. The fastest response, however, is obtained with 51°. The complex parts of the poles "speed up" the settling transient a bit further (25%). For higher values of phase margin, the dominant real pole moves to the right on the real axis. This pole is responsible for the slowing down of the PLL response for values of $\phi_m > 53°$. Fig. 5 shows that the dominant pole, for 60° phase margin, lies at about $-0.4 f_c$. Hence, it may be concluded that the usual practice of designing critically damped loops—which have a phase margin of about 70° [5]—is not appropriate for fast-settling-time applications.

Let us consider Fig. 3(b) again. One sees that the (envelope of the) curves can be approximated by straight lines. The ap-

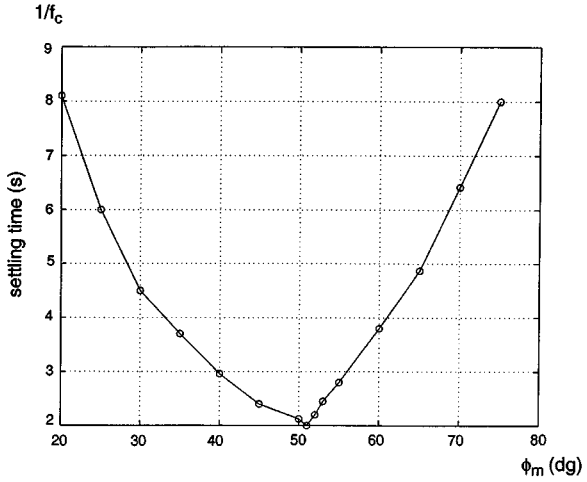


Fig. 4. Setting time as function of the phase margin for $f_{\rm error}/f_{\rm step} = e^{-10}$.

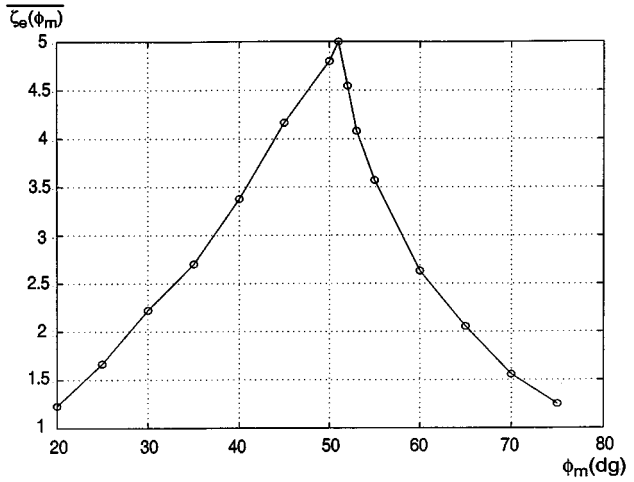


Fig. 6. Average values of $\zeta_e(\phi_m)$ for a $\Delta(\ln(\cdot))$ of ten.

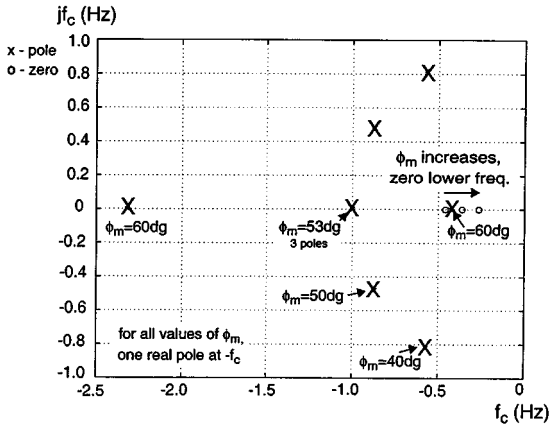


Fig. 5. Position of the *closed-loop* poles and zeros of a third-order PLL corresponding to different values of ϕ_m, as displayed in Fig. 2.

proach proposed here takes ϕ_m into account with the help of an *effective damping coefficient* $\zeta_e(\phi_m)$. By so doing, we arrive at the following approximation for the envelope of the curves of Fig. 3(b):

$$\mathrm{env}(\ln(|\Delta f(f_c t)|/f_{\rm step})) = -\zeta_e(\phi_m) \cdot f_c t. \tag{1}$$

Numerical estimations for $\zeta_e(\phi_m)$ can be obtained from transient simulations with the help of the following expression:

$$\overline{\zeta_e(\phi_m)} = \frac{-\Delta(\mathrm{env}(\ln(\Delta f(f_c t)/f_{\rm step})))}{\Delta(f_c t)}. \tag{2}$$

The settling time results presented in Fig. 4 leads to the numerical values for $\overline{\zeta_e(\phi_m)}$ displayed in Fig. 6. These values represent an average value for $\zeta_e(\phi_m)$, as they are obtained from a $\Delta(\mathrm{env}(\ln(\cdot)))$ of ten.

Manipulation of (1) results in an equation describing the minimum loop bandwidth required to achieve given settling specifications $t_{\rm lock}$, $f_{\rm error}$, and $f_{\rm step}$

$$f_c = \frac{1}{t_{\rm lock}\zeta_e(\phi_m)} \ln f_{\rm step}/f_{\rm error}. \tag{3}$$

In (3):

$t_{\rm lock}$ locking time(s);
$f_{\rm step}$ amplitude of the frequency jump (Hz);
$f_{\rm error}$ maximum frequency error (Hz) at $t_{\rm lock}$;
$\zeta_e(\phi_m)$ can be read from Fig. 6.

Two points about the present treatment of the transient response need further explanation. First, the presented results are based on a linear continuous-time model for the discrete-time charge-pump PLL. It is known in the literature [6] that the continuous-time approach is a good approximation for the discrete-time PLL if the reference (sampling) frequency $f_{\rm ref}$ of the loop is at least a factor of ten higher than its open-loop bandwidth f_c. Therefore, the value of f_c, calculated with (3), has to be checked against the loop's reference frequency $f_{\rm ref}$. If the target ratio $f_{\rm ref}/f_c$ is smaller than ten, then actual settling behavior will deviate from the calculations.

The second point is that usual implementations of the phase frequency detector have a limited linear phase error detection range, namely, from -2π to 2π [9]. When the instantaneous phase error $\phi_{\rm error}$ becomes larger than $\pm 2\pi$, the PFD interprets the error information as $(\phi_{\rm error} \mp 2\pi)$. This effect leads to a longer settling time than predicted with (3). The maximum value of $\phi_{\rm error}$, denoted $\phi_{\rm max}$, was found to obey the following relationship: $\phi_{\rm max} = \alpha(\phi_m)(f_{\rm step}/N)/f_c$, where N is the main divider ratio and $\alpha(\phi_m)$ is a fitting factor for the influence of the phase margin on $\phi_{\rm max}$. Numerical values for $\alpha(\phi_m)$, obtained from transient simulations, lie in the range [0.7,0.8]. Hence, the maximum phase error is contained in the interval $\pm 2\pi$, when $f_c > 0.8(f_{\rm step}/2\pi N)$. If this condition is satisfied, then the (discrete-time) transient response is accurately predicted by the continuous-time linear model.

Inaudible RDS background scanning requires settling times of 1 ms, defined as a residual settling error of 6 kHz for a 20-MHz frequency jump. The nominal loop phase margin is set to 50°, which corresponds to a $\zeta_e(\phi_m)$ of five. On the other hand, it is appropriate to use a lower value for $\zeta_e(\phi_m)$ in the calculations (e.g., 2.5), to provide enough margin for variations in the nominal values of loop bandwidth and phase margin. Solving (3) for these settling specifications leads to a nominal value of 3.2 kHz for the loop bandwidth f_c.

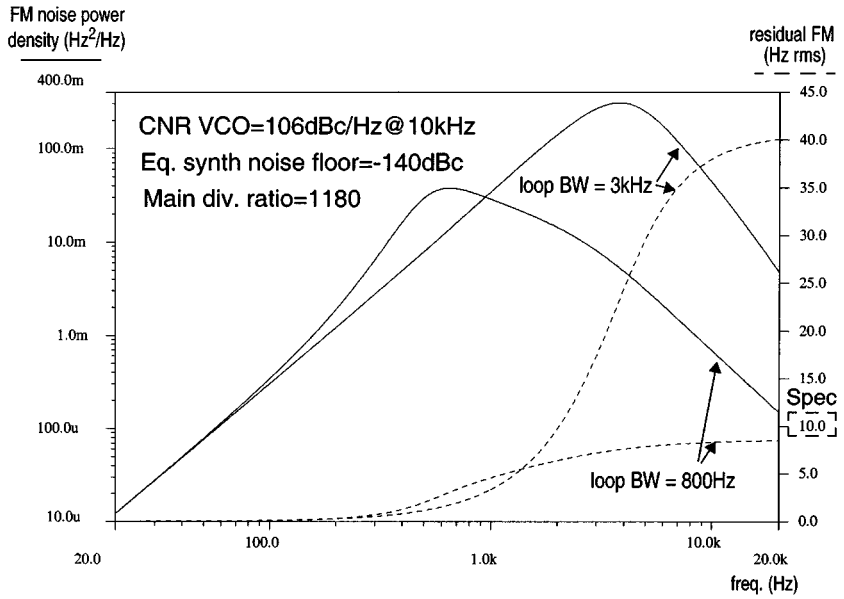


Fig. 7. FM noise density and residual FM for loop bandwidths of 800 Hz and 3 kHz.

The loop bandwidth that satisfies different settling requirements can be calculated with the help of (3). Settling specifications, however, often require loop bandwidths that are not optimal with respect to spectral purity performance, as will become clear in the next subsection.

B. Phase Noise Performance and Loop Bandwidth

The dependency of the total phase noise of a PLL tuning system on the phase noise of the loop components is well known in the literature [3], [5], [10]. The phase noise of the VCO is suppressed inside the loop bandwidth, whereas the (phase) noise from the other building blocks is transferred to the VCO output, multiplied by the closed-loop transfer function of the PLL: a low-pass function that suppresses their noise contribution outside the loop bandwidth. There is a "crossover point" for the loop bandwidth, where the noise contribution from the dividers and charge pump becomes dominant with respect to the noise from the VCO.

For terrestrial FM reception, the LO signal residual frequency noise (residual FM) determines the ultimate receiver's SNR performance. The SNR specification for the application is 64 dB, defined for a reference level of 22.5-kHz peak deviation with 50-μs deemphasis. Complying to the specification requires the residual FM in the LO signal to be less than 10 Hz rms.

The frequency (FM) noise density of the LO signal $S_{\Delta f}(f)$ is linked to its phase noise power density $S_{\Delta\theta}(f)$ by $S_{\Delta f}(f) = f_m^2 S_{\Delta\theta}(f)$ [5]. $S_{\Delta\theta}(f)$ equals $2\mathcal{L}(f)$, the single-sideband noise-to-carrier ratio, so that $S_{\Delta f}(f) = 2f_m^2\mathcal{L}(f)$. Finally, the residual FM can be calculated

$$\Delta f_{\rm res} = \sqrt{\int_{f_l}^{f_h} S_{\Delta f}(f)\,df} = \sqrt{\int_{f_l}^{f_h} 2f_m^2\mathcal{L}(f)\,df}. \quad (4)$$

The integration limits f_l and f_h in (4) depend on the signal bandwidth of the application [3]. For terrestrial FM reception, the lower limit is 20 Hz and the higher is 20 kHz. Fig. 7 presents the simulated frequency noise (FM noise) power density and the residual FM, which is plotted as function of f_h, with f_l fixed at 20 Hz. The FM noise density and the residual FM are plotted for values of loop bandwidth of 800 Hz and of 3 kHz. For 3 kHz, the residual FM amounts to 40 Hz rms, which is 12 dB higher than the specification. A loop bandwidth of 800 Hz, on the other hand, leads to a residual FM of 8 Hz rms, which satisfies the SNR requirement.

The contributions of different noise sources to the total frequency noise density, in the case of an 800-Hz loop bandwidth, are displayed in Fig. 8. The contribution of the VCO to the residual FM equals that of the other synthesizer building blocks. This is a good compromise, and 800 Hz was chosen as the nominal loop bandwidth for in-lock situations.

The settling specification requires a bandwidth of 3.2 kHz. The SNR constraint, on the other hand, asks for 800 Hz. These conflicting requirements can be combined when the loop bandwidth is made adaptive as a function of the operating mode: frequency jump or in-lock.

Adapting the value of the loop bandwidth during frequency jumps is easily accomplished by switching the nominal value of the charge-pump current [6], [13]. This method, however, often causes disturbances in the VCO tuning voltage—the so-called secondary glitch-effect—at the moment the current is switched from high to low values. These disturbances are highly undesirable, as they have to be corrected by the loop in small bandwidth mode. What is more, the "secondary glitches" may cause audible disturbances in analog systems and increase the bit error rate in digital systems.

To provide stability for a small bandwidth loop requires a transfer function zero located at low frequencies (large time constant). A low-frequency zero, however, is undesirable for operation in high bandwidth mode. It causes the phase margin to be "too" high, which increases the settling time. Note that the effective damping coefficient $\zeta_e(\phi_m)$ decreases for high values of phase margin (see Fig. 6).

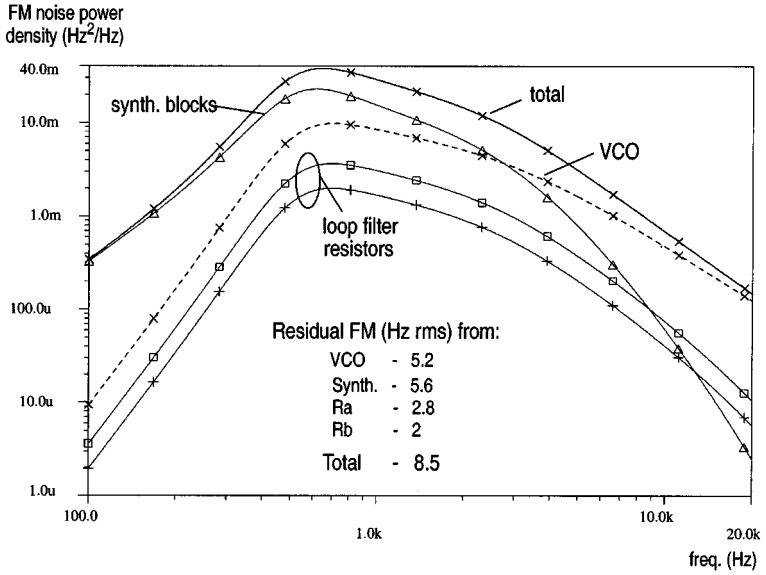


Fig. 8. Contributions from different noise sources to the total FM noise density and residual FM (20 Hz–20 kHz) with 800-Hz loop bandwidth.

Therefore, for optimal settling time *and* phase noise, one has not only to switch the value of the loop bandwidth but also to change the location of the zero in the transfer function.

C. Reference Spurious Signals and Loop Filter Attenuation

The use of phase frequency detectors yields the minimum levels of spurious breakthrough at the reference frequency [11]. The spurious signals are due to compensation of leakage currents or to imperfections in the charge pump's implementation. Standard FM modulation theory and the small angle approximation lead to the following equation for the amplitude of the spurious signal (in dBc), which is at an offset frequency f_m from the carrier:

$$\text{spurious}(f_m) = 20\log(i_{\text{sp}}(f_m) \cdot |Z(f_m)| \cdot K_{\text{vco}}/(2f_m)). \tag{5}$$

where

f_m offset frequency from the carrier (Hz);
$i_{\text{sp}}(f_m)$ amplitude of ac current component with frequency f_m (A);
$|Z(f_m)|$ impedance of the loop filter at f_m (V/A);
K_{vco} VCO gain (Hz/V).

The value of $i_{\text{sp}}(f_m)$ is twice the value of the loop-filter dc leakage current [12] in loops operating with well-designed charge pumps. In cases where the charge pump has charge-sharing problems and/or charge injection into the loop filter, $i_{\text{sp}}(f_m)$ may become dominated by these second-order effects. The imperfections can lead to spurious components with (much) higher amplitudes than would be expected based on the leakage current alone.

Rearranging the above equation leads to a formula that relates the required filter attenuation at f_m to the specified maximum level of spurious signals $(\max \text{spurious}(f_m))$, to the dc leakage current (I_{leak}), and to the VCO gain (K_{vco})

$$|Z(f_m)| < \frac{2f_m}{I_{\text{leak}}K_{\text{vco}}} 10^{\max \text{spurious}(f_m)/20}. \tag{6}$$

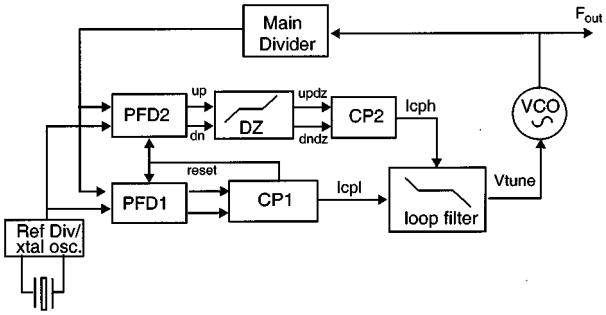
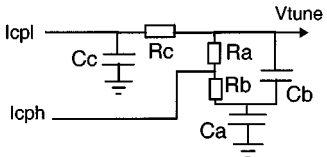


Fig. 9. Adaptive PLL tuning system architecture.



Icpl	130uA
Icph	3mA
Ca	100n
Cb	3.9n
Cc	3.3n
Ra	2.2k
Rb	1.2k
Rc	10k

Fig. 10. Loop-filter configuration, charge-pump currents, and component values used in the global car-radio tuner IC.

The relevant values of f_m equal f_{ref} and its harmonics in a standard PLL operating with a reference frequency of f_{ref} Hz. Therefore, the required loop-filter (trans)impedance for these frequencies can be readily calculated. The VCO gain, the spurious specification, and the expected (maximum) leakage current are known.

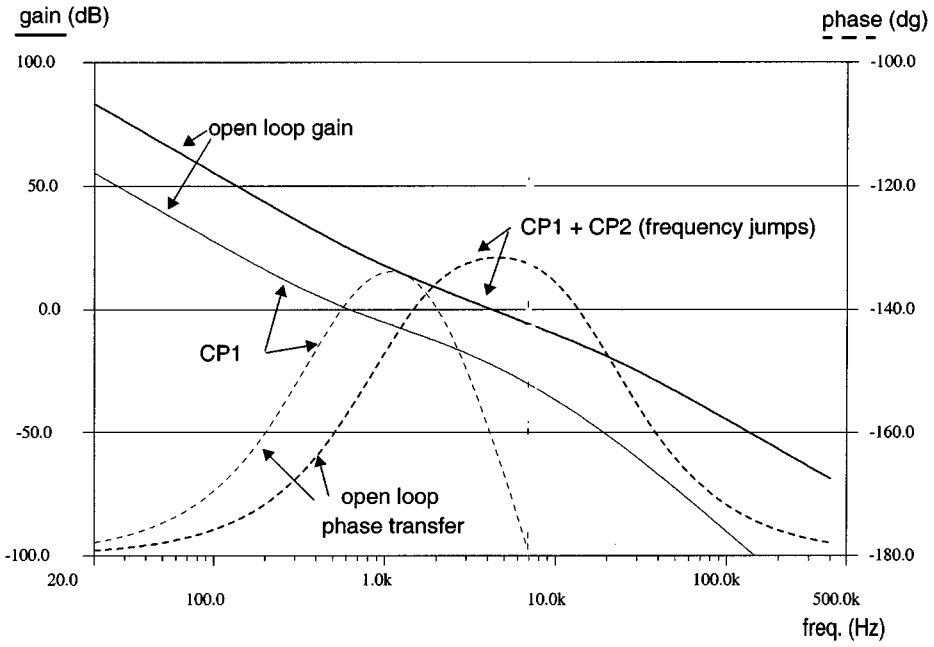


Fig. 11. Bode plots of the adaptive loop during frequency jumps and in-lock.

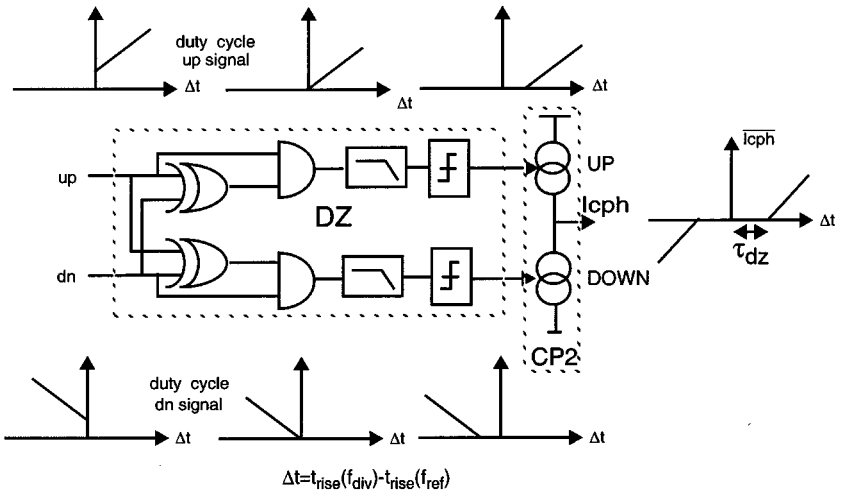


Fig. 12. Implementation of the DZ building block.

An important conclusion to be taken from the above equations is that the amplitude of the spurious signals is *not* dependent on the absolute value of loop bandwidth. Instead, it is determined by the (trans)impedance of the loop filter. This means that, at least in principle, "any" spurious specification can be achieved simply by decreasing the impedance level of the loop filter. In practice, this is not a viable option because the PLL loop bandwidth is proportional to the value of the loop-filter resistor and to the charge-pump current [6].

For a constant value of the loop bandwidth, a decrease of the loop-filter impedance level requires a proportional increase of the nominal charge-pump current. This leads to difficulties in the charge-pump design and to higher power dissipation. To avoid these difficulties, more RC sections are added to the basic loop-filter configuration, so that the filter attenuation at higher frequencies is increased. Additional RC sections, however, inevitably cause phase lag at lower frequencies. The phase lag decreases the loop phase margin and increases the settling time in high-bandwidth mode.

Therefore, to provide optimal settling, low-power dissipation, *and* good spurious performance, one has not only to switch the value of the loop bandwidth but also to bypass (some) RC sections of the loop filter. The PLL architecture presented here complies with these requirements.

IV. Adaptive PLL Architecture

A. Basic Architecture

The basic idea is to have two loops working in parallel, as depicted in Fig. 9. Loop 1, built around PFD1 and CP1, is dimensioned for in-lock operation. Loop 2, built around PFD2, DZ, and CP2, is dimensioned for fast settling time. Loop 1 operates all the time, whereas Loop 2 is only active during tuning

actions. Loop 1 and Loop 2 share the crystal oscillator, the reference divider, and the main divider.

A smooth takeover from Loop 1, after a frequency jump, avoids "secondary glitch" effects. The high-current charge pump CP2 is only active during tuning. CP2 is controlled by the dead-zone (DZ) block. DZ generates a *smooth* transition into a well-defined dead zone for CP2 when lock is achieved, so that sudden disturbances of the VCO tuning voltage are avoided.

Additional freedom for optimization of the loop parameters is obtained by using two separate charge-pump outputs and by applying the charge-pump currents to different nodes of the loop filter. In this way, the location of the zeros for frequency jumps and in-lock can be set in a continuous way, without switching of loop components—which is a source of "secondary glitch" problems. Furthermore, the path from Icpl to Vtune may contain additional filtering sections for, e.g., attenuation of spurious signals and/or fractional-N quantization noise [14]. These filter sections may be bypassed by Icph to increase the phase margin in high-bandwidth mode.

B. Loop-Filter Implementation

The ideas described above are demonstrated with the help of Figs. 10 and 11. Fig. 10 presents the loop-filter configuration and component values used in the global tuner IC (Fig. 1). Fig. 11 shows the optimized Bode diagrams of the adaptive PLL (in FM mode) with the loop filter of Fig. 10.

During frequency jumps both CP1 and CP2 are active; the loop filter zero frequency is $1/2\pi$ RbCa and lies at a high frequency, matching the 0-dB open-loop frequency. It enables stability and fast tuning to be achieved. The nominal loop bandwidth in this mode is 3.2 kHz, and the phase margin is 50°. After the frequency jump only CP1 is active. The zero of the loop filter moves to a lower frequency ($1/2\pi(\mathrm{Ra} + \mathrm{Rb})\mathrm{Ca}$), without the switching of loop-filter components. The low-frequency zero increases the phase margin in-lock.

When the loop is in-lock, an extra pole is introduced ($1/2\pi$ RcCc), which increases the 100-kHz reference suppression by about 20 dB. During frequency jumps, these elements are bypassed by CP2, increasing the phase margin in high-bandwidth mode. If the loop bandwidth were increased by simply switching the amplitude of CP1, one would end up with an unstable loop, because of a phase margin of less than 10°in high-bandwidth mode.

C. Dead-Zone Implementation

The new element in the adaptive PLL architecture is the combination of the DZ block with the high-current charge pump CP2. The function of DZ is to provide CP2 with a well-defined dead zone of $\pm\tau_{\mathrm{dz}}$ s. The dead zone is centered symmetrically around the locking position of charge pump CP1 [see Fig. 13(a)].

The logic diagram of the DZ/CP2 combination is depicted in Fig. 12. The figure shows how the different logic functions influence the duty cycle of the *up* and *dn* signals from the phase frequency detector (PFD2). At the input of DZ, the *up* and *dn* signals have a finite duty cycle, even for an in-lock situation ($\Delta t = 0$). The finite duty cycle eliminates dead-zone problems in CP1. The XOR and AND gates are used to cancel the finite

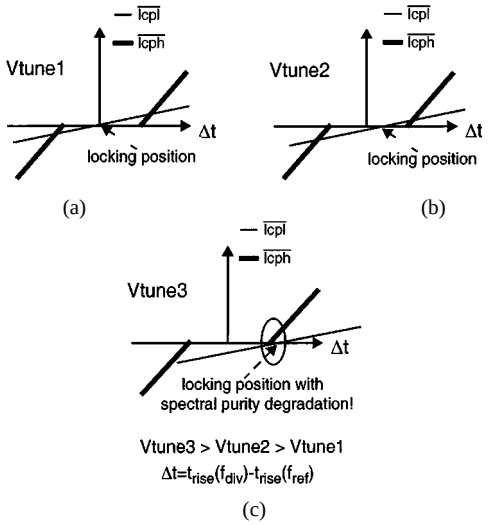


Fig. 13. Shift in locking position as function of VCO tuning voltage.

in-lock duty cycle. The processed *up* and *dn* signals are then applied to low-pass filters and slicers, whose function is to prevent pulses that have too small a duty cycle from reaching CP2. The cutoff frequency of the low-pass filters, the discrimination level of the slicers, and the turn-on time of CP2 determine the size of the dead zone around the lock position $\pm\tau_{\mathrm{dz}}$ s.

A tradeoff among settling performance, circuit implementation, and robustness arises, when the magnitude of the dead zone τ_{dz} has to be determined. Let us start discussing circuit aspects.

The dead zone of charge pump CP2 should be centered around the locking position of the loop for optimum settling and spectral purity performance. The locking position, however, is a function of the output voltage of charge pump CP1. The effect is depicted in Fig. 13. One sees that, as the tuning voltage Vtune increases, there is a shift of the locking position to positive values of Δt. The reason lies in the finite output resistance of the active element used in CP1. Different current gains in CP1's UP and DOWN branches need to be compensated by *up* and *dn* signals with different duty cycles at the locking point. Different duty cycles are accomplished by a shift in the loop's locking position.

Fig. 13 shows situations where the gain in the UP branch of the pump decreases as Vtune increases. The ideal operating situation is depicted in Fig. 13(a). Situation (b) is still allowed from the point of view of spectral purity but has asymmetrical settling performance. Finally, (c) depicts a situation that should never happen: the locking position shifts so much that the high-current charge pump CP2 becomes active and degrades the in-lock spectral purity. Therefore, increasing the size of CP2's dead zone ($\pm\tau_{\mathrm{dz}}$ s) eases the design of charge pump CP1 and increases the robustness of the system.

On the other hand, the size of CP2's dead zone influences the settling performance of the adaptive loop. The influence of τ_{dz} on the transient response was simulated with behavioral models. The results are displayed in Fig. 14, together with the settling requirements that ensure inaudible background scanning functionality. Table II presents the settling time for different settling accuracies and different values of τ_{dz}. A dead-zone value of infinity corresponds to the situation where only CP1 is active

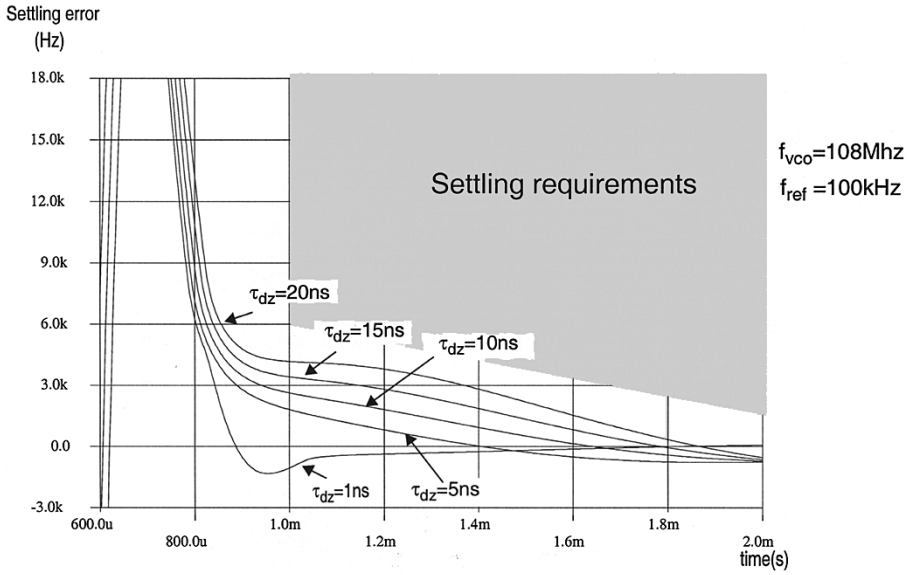


Fig. 14. Detail of settling transient for different values of τ_{dz}.

TABLE II
SIMULATED IN-LOCK SNR AND SETTLING TIME (ms) FOR A 20-MHz FREQUENCY JUMP FOR DIFFERENT VALUES OF THE DEAD ZONE AND DIFFERENT SETTLING ACCURACIES

Settling accuracy (f_{error})	Dead-zone value τ_{dz}				
	0	5 ns	15 ns	20 ns	∞
6 kHz	0.79	0.81	0.84	0.85	7.9
3 kHz	0.81	0.88	1.14	1.37	8.1
1 kHz	0.98	1.15	1.56	1.68	9.4
SNR (dB)	52	66			

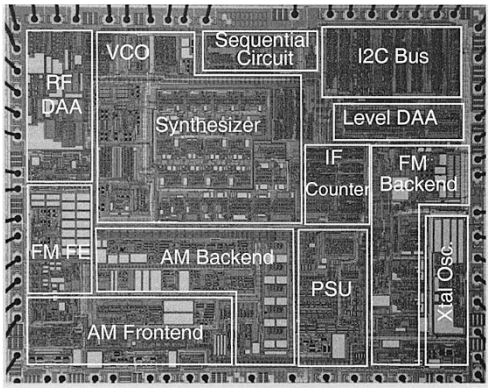


Fig. 15. Micrograph of the tuner IC.

(nonadaptive loop). Table II shows that by using the adaptive loop architecture, it is possible to combine fast settling time with good SNR in-lock. Increasing τ_{dz} leaves more "residual" phase (and frequency) error to be corrected by the small bandwidth loop. The closer one comes to the locking point in high bandwidth mode, the shorter the total settling transient will be. A dead-zone value of ± 15 ns is a good compromise for the intended application.

V. CIRCUIT IMPLEMENTATION

A die micrograph of the total tuner IC is displayed in Fig. 15. The adaptive PLL has been integrated with the other functional blocks of Fig. 1 in a 5-GHz, 2-μm bipolar technology [15].

A. Programmable Dividers

The architecture of the main divider is depicted in Fig. 16. The high-frequency part of the programmable divider is based on the programmable prescaler concept described in [12] and consists of a chain of 2/3 divider cells. The modular architecture enables easy optimization of power dissipation and robustness for process variations. The division range of the basic prescaler configuration is extended by the low-frequency programmable counter. The logic functions of the PLL were implemented with current routing logic techniques (CRL) [12], [16]. The low-frequency part of the main and reference dividers operate with low current levels to limit total power dissipation. To decrease the phase noise of the reference signal going to the phase detectors, this signal is reclocked in a high-current D-flip-flop (D-FF). The clean crystal signal is used to clock the D-FF. The total main divider current consumption is 5 mA. The first 2/3 cell consumes 2.1 mA.

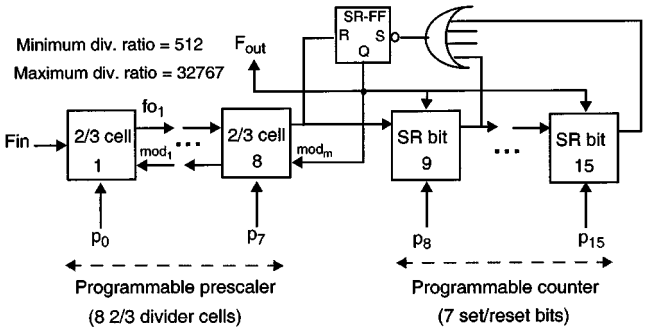


Fig. 16. Architecture of the main programmable divider.

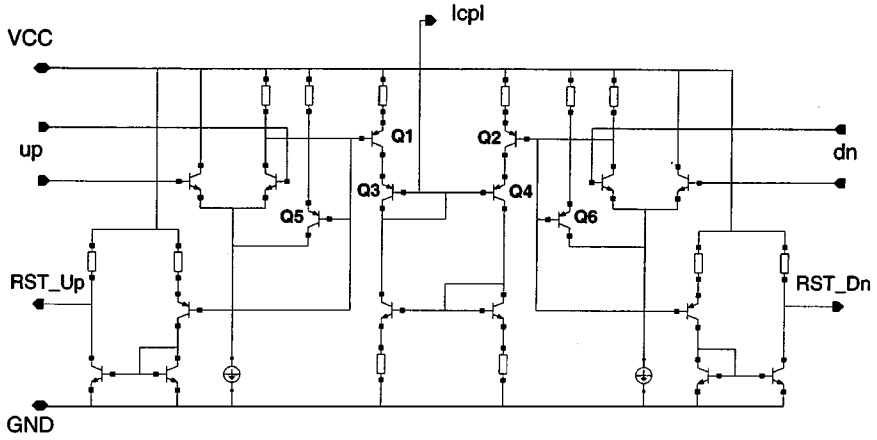


Fig. 17. Simplified circuit diagram of charge pump CP1.

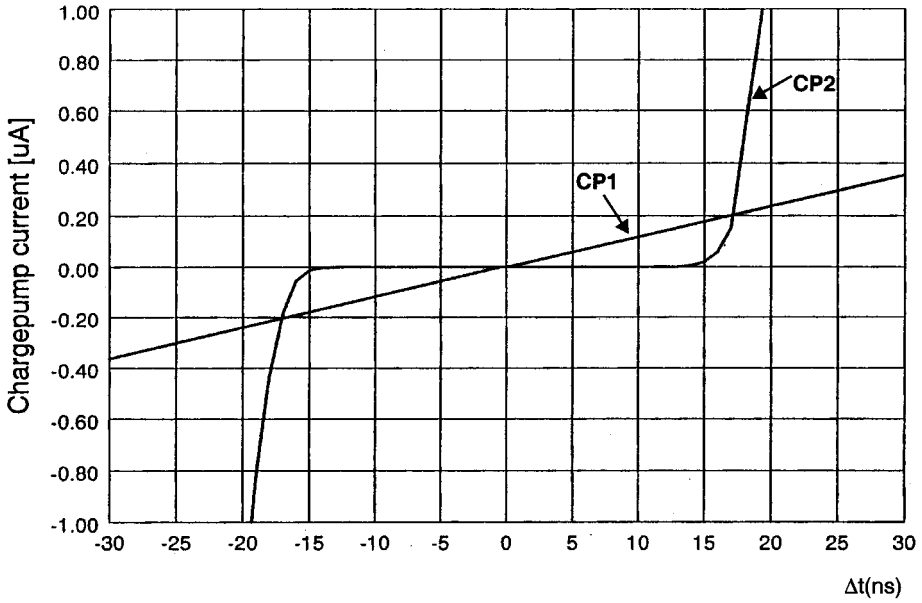


Fig. 18. CP1 and CP2 charge-pump currents as a function of Δt.

B. Oscillators

The LC VCO uses an external tank circuit. It can be tuned from 150 to 250 MHz, with a voltage tuning range from 0.5 to 8 V. The VCO phase noise is −100 dBc/Hz at 10 kHz, for a carrier frequency of 237 MHz. The VCO core consumes 1.5 mA. The 20.5-MHz reference crystal oscillator operates in linear mode, to avoid harmonics interfering in the FM reception bands. Quadrature generation for the image rejection FM mixers (see Fig. 1) is accomplished in a divider-by-two (FM DIV), with the exception of reception in the American Weather Band (WX). In that case, I/Q signals are generated with a RC-CR network directly from the VCO. This avoids the need to have the VCO operating at 346 MHz, and a change in the LC VCO tuned circuit during WX reception.

C. Charge Pumps

Fig. 17 shows the simplified circuit diagram of the low-current charge pump CP1. The *up* and *dn* signals from the phase

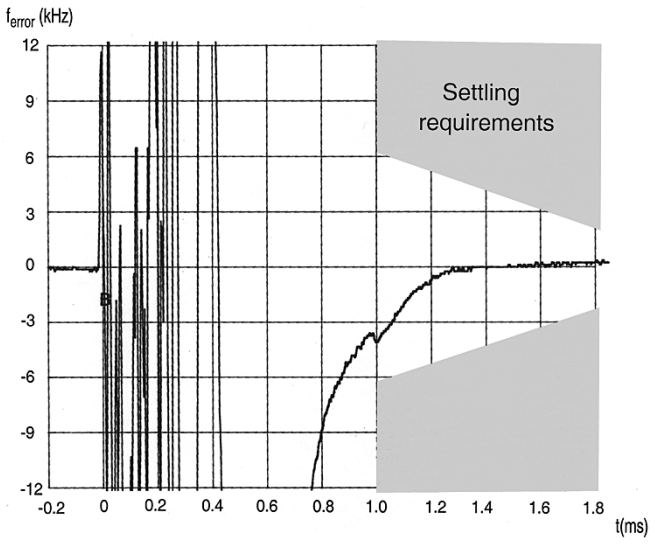
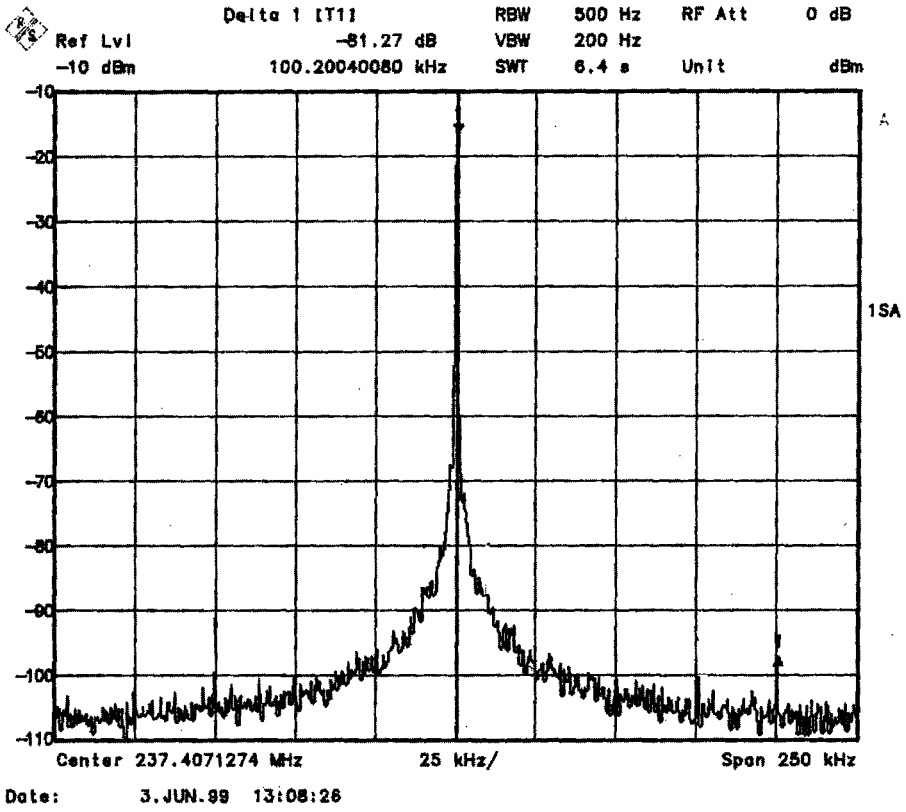
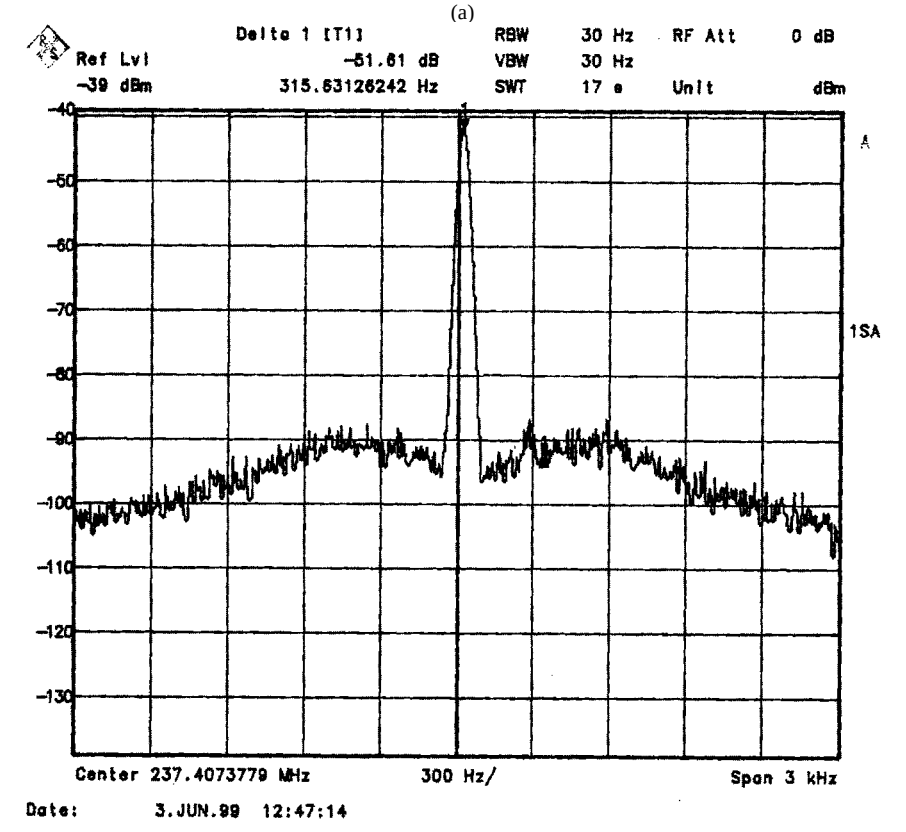


Fig. 19. Settling transient for a 20-MHz tuning step.



(a)



(b)

Fig. 20. Spectral purity measurements in FM mode: (a) reference spurious breakthrough and (b) close to the carrier.

detector drive the input differential pairs, which set the currents in the PNP current switches Q1 and Q2 on and off. The collector outputs of Q1 and Q2 are kept at equal dc levels by the dc feedback arrangement provided by Q3 and Q4. This prevents asymmetry in the source and sink currents, ensuring good centring of the charge-pump characteristics for all tuning voltages. Q5 and

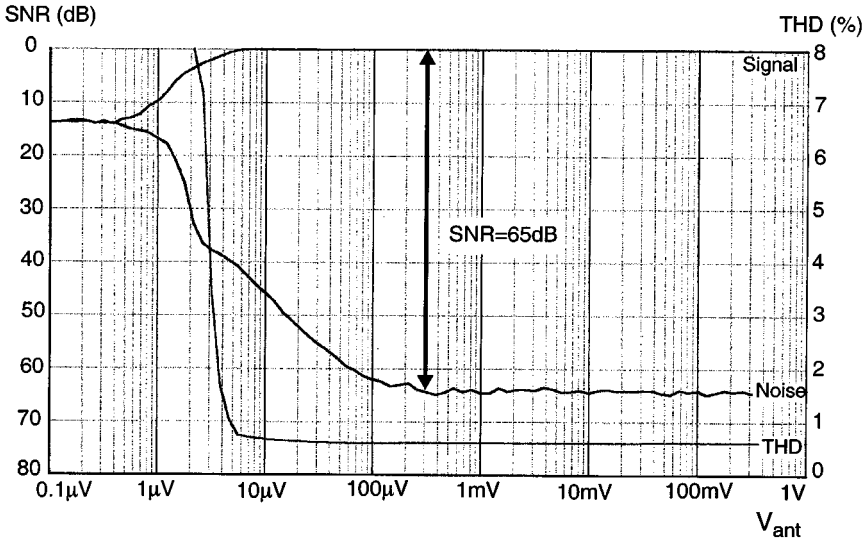


Fig. 21. Evaluation of the FM channel—VCO purity determines SNR for $V_{\rm ant} > 300\ \mu$V. Fin $= 97.1$ MHz, AF freq $= 1$ kHz. SNR meas.: FMdev $= 22.5$ kHz; 26 dB $= 2.0\,\mu$V. THD meas.: FMdev $= 75$ kHz.

Q6 provide means for stabilization of currents and for speeding up the switching of Q1 and Q2. The reset circuits monitor the currents in Q1 and Q2 and generate the reset signals RST_Up and RST_Dn. These signals are fed back to reset the phase detectors. The high-current charge pump CP2 is a scaled-up version of the CP1 circuit, without the reset circuits.

VI. Measurements

The measured charge-pump currents as a function of the time difference between the phase detector inputs are shown in Fig. 18. Good centering of the two charge-pump outputs is observed, and there is enough margin for variations in the in-lock position of CP1. The measured settling transient response is displayed in Fig. 19. The settling performance complies to the settling requirements and enables inaudible background scanning in single-tuner RDS applications.

The frequency spectrum of the VCO in FM mode is presented in Fig. 20(a) and (b). Fig. 20(a) shows the spurious reference breakthrough at 100 kHz to be under -81 dBc. There is yet a 6-dB improvement in noise and spurious breakthrough before the VCO signal reaches the FM mixers, due to the division by two in the FM DIV divider (see Fig. 1). Fig. 20(b) displays the phase noise spectrum close to the carrier. Spectrum measurements done in AM mode showed a reference spurious breakthrough of -57 dBc, at an offset of 20 kHz from the carrier. For AM, the improvement in phase noise and spurious performance amounts to 26 dB, due to the division by 20 in between the VCO and the AM mixers.

Finally, the SNR and THD of the total FM receiver chain are displayed in Fig. 21 as a function of the antenna input signal level $V_{\rm ant}$. For low values of $V_{\rm ant}$, the noise is dominated by RF input noise and by the quality of the building blocks in the signal processing chain: low-noise amplifier, mixers, and demodulator. For high values of $V_{\rm ant}$ ($>300\ \mu$V), the dominant noise source becomes the LO signal. The excellent measured FM sensitivity, 2.0 μV for 26-dB SNR, and the ultimate SNR of 65 dB verify the spectrum purity of the tuning system and of the RF channel.

VII. Conclusion

This paper described an adaptive PLL architecture for high-performance tuning systems. The relationships of performance aspects to design variables were presented. It is demonstrated that design for spectral purity performance often leads to suboptimal settling performance, because of different requirements on the loop bandwidth and on the location of the zeros and poles of the closed-loop transfer function. The adaptive architecture described here resolves these contradictory requirements, without the necessity of switching circuit elements in the loop filter. The adaptation of loop bandwidth occurs continuously, as a function of the phase error in the loop, and without interaction from outside of the tuning system. During frequency jumps, high bandwidth and high phase margin are obtained by bypassing filter sections. When the loop is locked, the architecture allows heavy filtering of spurious signals. The implementation of the dead-zone block was presented, and the basic tradeoffs of the concept were discussed. The adaptive PLL was optimized for use in a multiband (global) car-radio tuner IC, which features inaudible background scanning. Design and architecture of the PLL building blocks were discussed, and measurement results were presented. The integrated adaptive PLL tuning system achieved state-of-the-art settling and spectral purity performance in its class (integer-N PLL's). It fulfills simultaneously the speed requirements for inaudible frequency hopping and the heavy SNR specification of 64 dB.

Acknowledgment

The author wishes to thank D. Kasperkovitz for technical support during the project, K. Kianush for his tireless disposition in bringing the car-radio project to a successful end, H. Vereijken for the optimization and layout of the synthesizer building blocks, B. Egelmeers for the implementation and evaluation of the concept in a bread-board functional model, and G. van Werven for the measurements.

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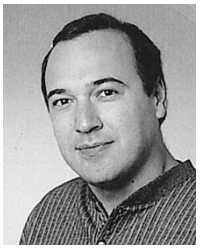

Cicero S. Vaucher (M'98) was born in São Francisco de Assis, Brazil, in 1968. He graduated in electrical engineering from the Universidade Federal do Rio Grande do Sul, Porto Alegre, Brazil, in 1989.

He joined the Integrated Transceivers group of Philips Research Laboratories, Eindhoven, The Netherlands, in 1990, where he works on implementations of low-power building blocks for frequency synthesizers, on synthesizer architectures for low-noise/high-tuning-speed applications, and on CAD modeling of PLL synthesizers.