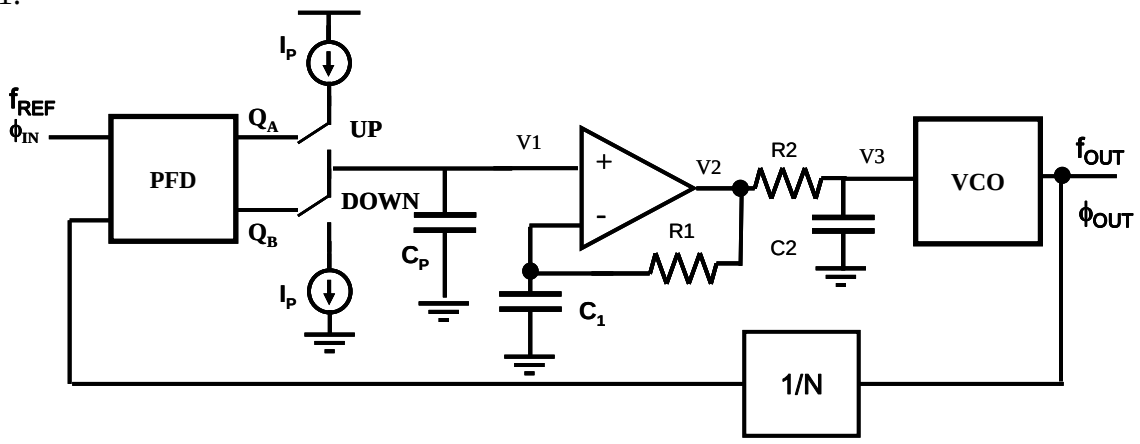
ECE145B/ECE218B Homework #5 Winter 2011
Due Monday 3/7/2011 at homework box, 3rd floor

1.



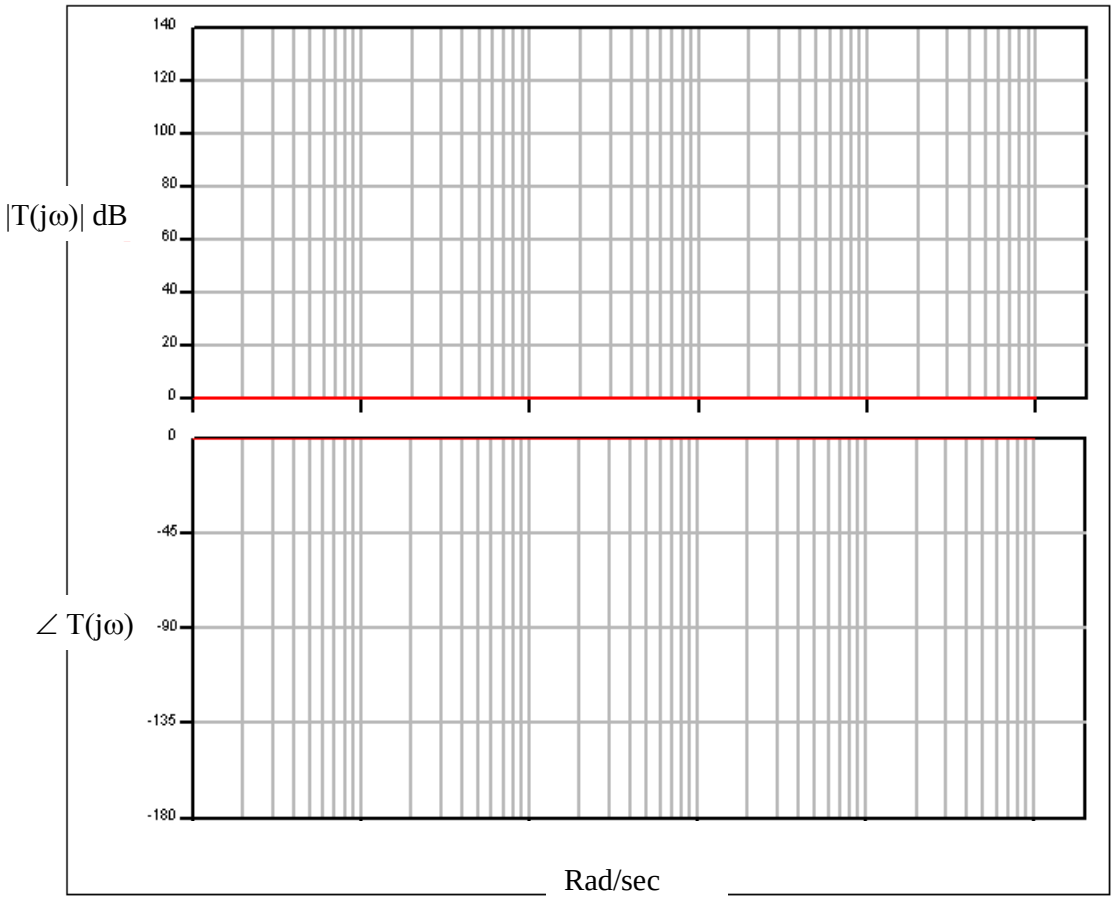
a. Derive T(s) and |T(jω)| for the PLL above. Note that: $\frac{V_1}{\Delta\phi} = \frac{I_P}{2\pi C_P s}$

b. The magnitude of T at 1 rad/sec is 120 dB. Also,

I_P	0.1 mA
K_O	6.28 x 10^5 rad/sec/V
F_{ref}	100 kHz
F_{out}	100 MHz

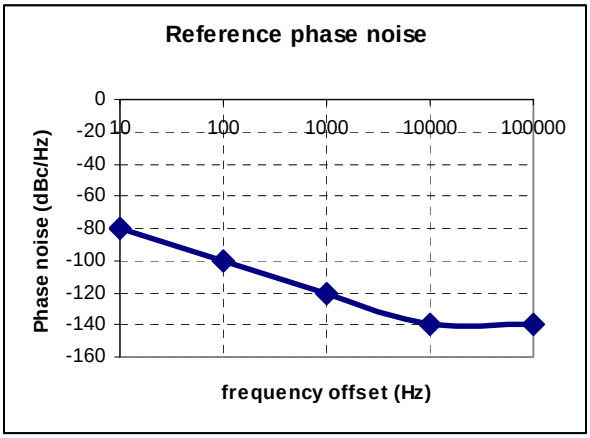
Determine C_P

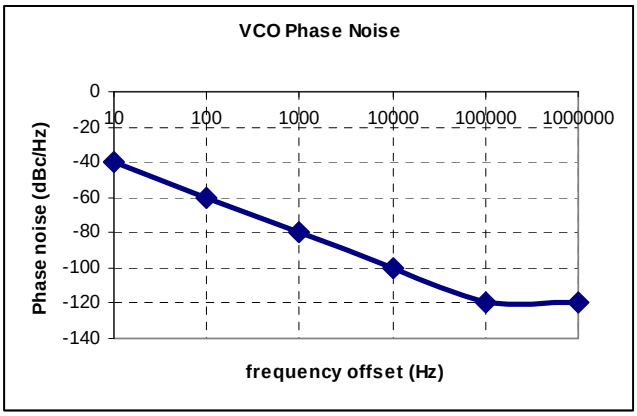
c. Assuming C2 = 0, determine the zero frequency needed to set the crossover frequency, ωc = 3000 rad/sec. If R1 = 10k, find C1.
d. Now add the third pole to make the phase margin 60 degrees. If R2 = 10k, find C2. What will be the phase margin for this crossover frequency?
e. How much spur rejection is expected for this combination?


|T(jω)| dB
140
120
100
80
60
40
20
0
∠ T(jω)
0
-45
-90
-135
-180
Rad/sec

f. The phase noise power to carrier power ratio, L(Δf), vs. offset frequency is displayed in the plots below for the reference oscillator and the VCO of the PLL in part a.

What will be the phase noise N/C ratio at the output of the VCO at a 100 Hz offset frequency (Δf)? Explain why.

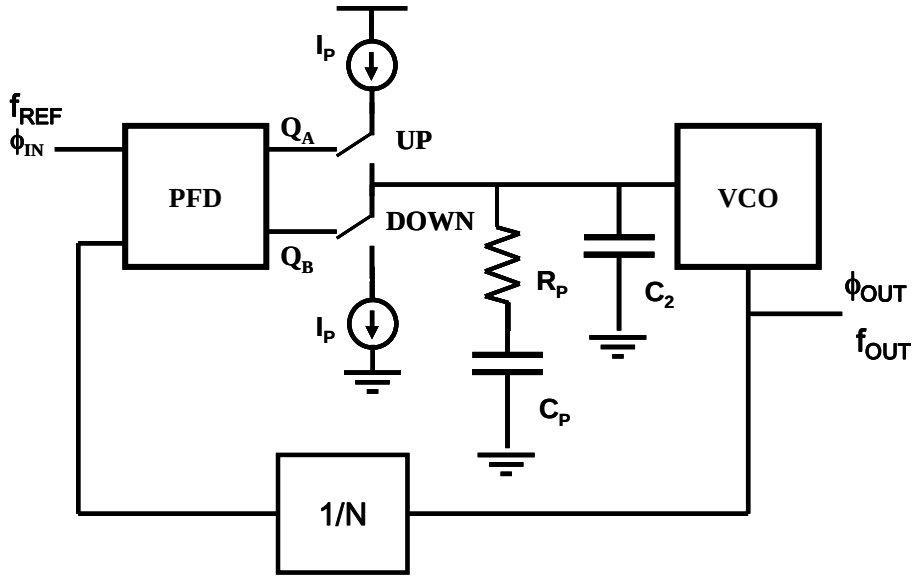


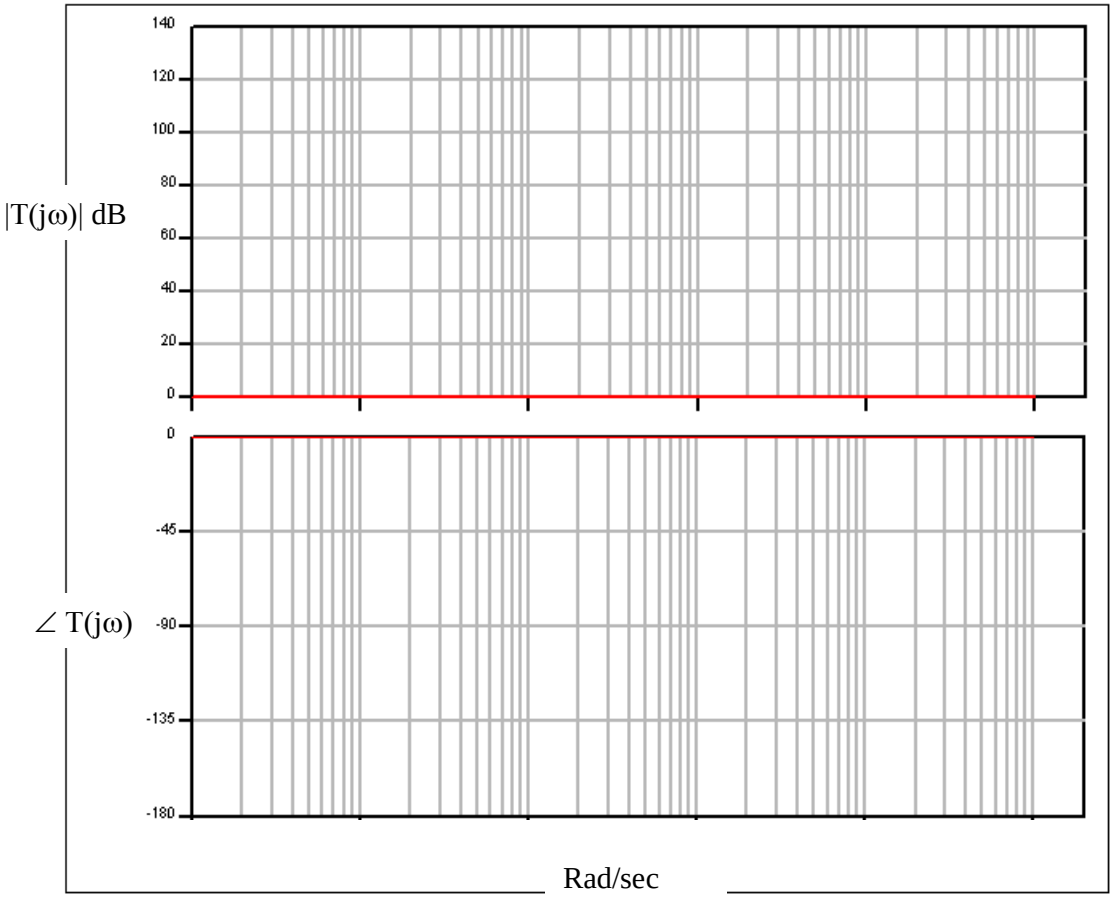


What will it be at 10 kHz offset? Explain why.

g. Explain why low phase noise is important for local oscillator PLL applications.

2. a. Using your VCO from Lab 2, design a third-order CP PLL with the required frequency step, settling time and reference spur specifications. Choose Ip to be either 1.176mA or 2.5 mA. Use the procedure from the PLL Notes 2 or Vaucher for your design.





b. Verify with ADS.