

# An 80-MHz, 80-mW, 8-b CMOS Folding A/D Converter with Distributed Track-and-Hold Preprocessing

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**Abstract**—An analog-to-digital converter incorporating a distributed track-and-hold preprocessing combined with folding and interpolation techniques has been designed in CMOS technology. The presented extension of the well known folding concept has resulted in a 75 MHz maximum full-scale input signal frequency. A signal-to-noise ratio of 44 dB is obtained for this frequency. The 8-b A/D converter achieves a clock frequency of 80 MHz with a power dissipation of 80 mW from a 3.3 V supply voltage. The active chip area is 0.3 mm<sup>2</sup> in 0.5- $\mu$ m standard digital CMOS technology.

## I. INTRODUCTION

EVOLUTION of CMOS technology into the submicron region has made possible the integration of more and more digital signal processing systems on a single VLSI chip. However, the interfaces of the system to the external world will remain in the analog signal domain. The advantages of embedding these analog-to-digital and digital-to-analog interfaces on the digital system chip are evident. This paper describes an analog-to-digital converter in standard digital CMOS technology, capable of converting full scale analog input signals with a frequency up to 75 MHz. This high analog input bandwidth is achieved due to an improved folding architecture.

Successful implementation of folding and interpolation techniques in high-speed A/D converters is demonstrated in both bipolar [1]–[4] and, more recently, CMOS technology [5]–[7]. The performance of the A/D converters described in these papers makes clear that a folding architecture realizes an optimum balance between power dissipation, clock frequency, and chip area due to the limited number of comparators in this type of A/D converters. The folding architecture can be considered as a time-continuous two-step architecture. In a two-step or pipeline A/D converter, the signal conversion is split into two or more phases in time. In a folding A/D converter, the signal conversion consists of a coarse and a fine conversion stage, but these conversions are done in parallel. This gives a folding A/D converter the same maximum clock frequency that can be achieved with full-flash A/D converters. A track-and-hold amplifier is not necessary in this type of A/D converter. However, the input signal frequency is multiplied in the analog preprocessing of the A/D converter as a result of the *folding* operation. The maximum frequency multiplication

in a folding system is determined by the folding factor of the A/D converter. A high folding factor results in a low number of comparators, but on the contrary, it lowers the maximum input signal frequency of the A/D converter. In [4], a folding architecture has been combined with an input track-and-hold amplifier, overcoming this bandwidth limitation in folding A/D converters.

The presented folding A/D converter incorporates a distributed track-and-hold operation embedded in the analog folding preprocessing. Distribution of the track-and-hold function leads to an accurate and simple overall system implementation. Maximum frequency of a full-scale analog input signal equals 75 MHz. Clock frequency is 80 MHz at a power dissipation of 80 mW from a 3.3 V supply voltage.

First the distributed track-and-hold folding architecture will be discussed. Special attention will be given to the design of the track-and-hold input gain stage. In Section IV the realized CMOS circuit implementation is described. Measurement results of the A/D converter will be given in Section V. Finally, conclusions on this design will be drawn in Section VI.

## II. DISTRIBUTED TRACK-AND-HOLD FOLDING ARCHITECTURE

In several publications, the advantages of a general folding A/D converter architecture have been demonstrated [1]–[7]. In many ways, the comparison of a folding architecture with a full-flash A/D converter architecture is justified. However, most drawbacks of a full-flash converter have been eliminated. Fig. 1(a) shows a standard implementation of a folding A/D converter. It consists of a parallel operating coarse flash converter and a fine flash converter. The coarse flash converter directly quantizes the input signal, whereas the fine flash converter is preceded by the analog folding preprocessing.

The folding preprocessing generates one or more folding signals, which are a function of the input signal. In [5] it is described that the number of folding signals needed in the A/D converter can be interchanged to the number of voltage levels that need to be distinguished per folding signal. As an example, a 5-b fine resolution can be realized by detection of 31 voltage levels in only one folding signal [Fig. 1(b)]. The same fine resolution can be achieved by detection of only one voltage level in each of 32 folding signals [Fig. 1(c)]. In a differential folding system only the zero crossings of the folding signals have to be detected. Implementation of a zero-crossing detection system is more robust than a voltage level detection system. The latter system needs an accurate matching

Manuscript received June 18, 1996; revised August 2, 1996.

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Publisher Item Identifier S 0018-9200(96)08221-2.

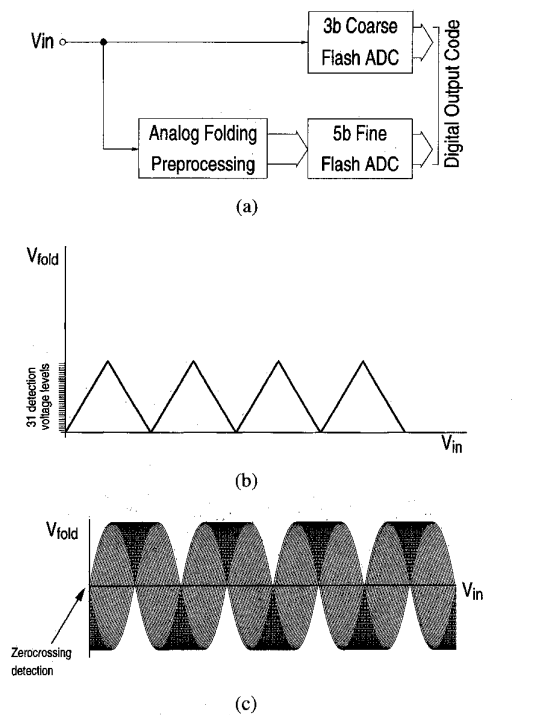


Fig. 1. (a) Block diagram of a standard folding A/D converter, (b) detection of 31 voltage levels in a single folding signal, and (c) 32 output signals of the analog folding preprocessing.

of the full scale fine reference with the different coarse levels. The interpolation operation in a zero-crossing detection system automatically adjusts the full scale fine reference to the different coarse levels. As long as the comparators can determine the sign of a folding signal, the shape of the signal is of less importance. The locations of the zero crossings in the folding signals determine the code transitions in the input range of the A/D converter.

In the presented A/D converter, 32 folding signals are generated with eight zero crossings in the input range of the A/D converter each, giving a total number of  $8 \times 32 = 256$  zero crossings. This provides an 8-b quantization of the input signal. One of the folding signals represents an analog version of the MSB-2 bit and can directly be used for the coarse encoding of the output bits. The partitioning of coarse and fine bits (three coarse bits, five fine bits in this A/D converter) is a tradeoff between the number of comparators required and the complexity of the analog folding preprocessing.

The bandwidth realized in the folding preprocessing ( $BW_{\text{fold}}$ ) will be the limiting factor with respect to the maximum input signal frequency that can be achieved. This is exacerbated by the effect that the folding preprocessing acts like an amplitude dependent frequency multiplier. For a sinusoidal input signal, it can be derived that the maximum input signal frequency  $f_{\text{in,max}}$  of the A/D converter equals

$$f_{\text{in,max}} = \frac{2BW_{\text{fold}}}{\pi F_F} \quad (1)$$

in which  $F_F$  is the folding factor. The folding factor determines the number of zero crossings in a single folding signal. In this A/D converter a folding factor of eight is used.

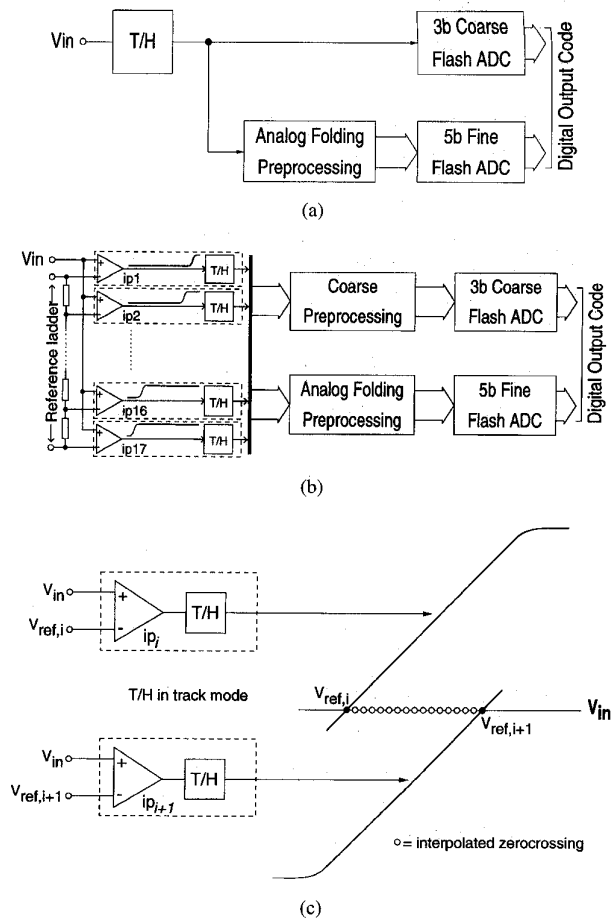


Fig. 2. (a) Standard solution of a track-and-hold amplifier in front of a folding A/D converter, (b) distribution of the track-and-hold operation in 17 parallel track-and-hold input gain stages, and (c) generation of 16 codes—zero crossings—per track-and-hold input gain stage via interpolation in the folding preprocessing.

This limitation on the analog input signal bandwidth can be overcome by the integration of a track-and-hold amplifier in front of the folding A/D converter [Fig. 2(a)]. The bandwidth of the track-and-hold amplifier now determines the overall analog bandwidth of the A/D converter. The performance of the converter and maximum clock frequency that can be achieved is then limited by the settling behavior of the analog preprocessing during the hold phase of the system. To realize a low harmonic distortion converter, a high dynamic range in the track-and-hold amplifier is required. Since the A/D converter has an input signal range of  $1.6 V_{\text{pp}}$  this can only be done at the expense of high power dissipation.

The realized A/D converter uses a distributed implementation of the track-and-hold function. In this way, an optimum overall system performance can be achieved. The demands on the individual track-and-hold circuits are relaxed compared to the previously described system [Fig. 2(a)]. In Fig. 2(b) a block diagram of a distributed track-and-hold folding architecture is shown. In front of the folding operation an additional preprocessing has been added. It consists of a set of 17 parallel track-and-hold input gain stages, realizing a partitioning of the input signal range into 16 subranges. The input signal range is

TABLE I  
COMPARISON OF SINGLE TRACK-AND-HOLD AMPLIFIER SOLUTION AND  
DISTRIBUTED TRACK-AND-HOLD OPERATION IN A FOLDING A/D CONVERTER

	Single track-and-hold amplifier	Distributed track-and-hold operation
Linear region	Linearity in entire input range (1.6 $V_{pp}$ ) of A/D converter	Linearity in 1/16 of the input range of the A/D converter
Dynamic accuracy: • Settling • Hold mode feedthrough • Clock switch charge injection	8-bit accuracy	8-bit accuracy divided by the gain in the input gain stages
Overall power dissipation	High power dissipation in buffer amplifier to ensure low distortion	No additional power dissipation apart of input gain stages
Clock distribution	Single clock switch	Multiple clock switches

defined by a resistor reference ladder, generating 17 uniformly spaced reference voltages. The sampling time differences in the distributed track-and-hold circuits must be kept small: 75-MHz full-scale input signal frequency requires a sampling time difference below 16 ps. In the layout, the sampling clock interconnect lines are shorter than 500  $\mu\text{m}$ , so this condition is easily satisfied. For 8-b resolution, each of the track-and-hold gain stages is responsible for 16 adjacent codes in the input range of the A/D converter [Fig. 2(c)]. Linearity of the transfer function of the input gain stages is therefore mainly required in 1/16 of the input range of the A/D converter.

The zero crossings required for the 32 folding signals are generated via combination and interpolation of the output signals of the input track-and-hold gain stages. Finally, each of the folding signals contains eight zero crossings in the input range of the A/D converter as shown in Fig. 1(c). Additionally, the coarse flash converter also operates from the output signals of the input track-and-hold gain stages via an analog coarse preprocessing block.

Comparing the distributed track-and-hold folding architecture to the common folding architecture with single track-and-hold amplifier in front, the improvements made are twofold.

- The demands on the distributed track-and-hold function in the input gain stages are much less severe than the demands on a single track-and-hold amplifier in front of the A/D converter. In Table I, both systems are compared on some important design parameters. Apart from the increased complexity of clock switching, the distributed track-and-hold folding architecture is favorable for all design parameters.
- Due to the gain in the track-and-hold stages, requirements to the folding preprocessing become more relaxed. Offset requirements in the folding circuitry may be relaxed by a factor equal to the gain in the input stages. Furthermore, the analog coarse preprocessing will show (the same) settling behavior. Therefore, synchronization problems between coarse and fine flash converters will not occur.

By addition of a set of track-and-hold input gain stages, a costly single track-and-hold amplifier is no longer required

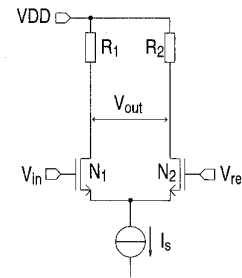


Fig. 3. Implementation of input gain stages with a NMOS differential pair.

and the folding preprocessing circuitry can be implemented more simply. The major limitation to the overall performance of the A/D converter is now found in the performance of the set of input track-and-hold gain stages. In the next section, an analysis of the influence of the behavior of the track-and-hold gain stages on the A/D converter performance will be given.

### III. DESIGN CONSIDERATIONS FOR THE TRACK-AND-HOLD GAIN STAGES

The influence of the performance of the input gain stages will be analyzed with respect to two topics. First, the influence of feedthrough on the reference ladder will be discussed. Second, the relation between gain stage nonlinearity and A/D converter performance will be derived.

In Fig. 3 a standard implementation for the input gain stage is given. As shown in Fig. 2(b), one of the inputs of the gain stage is connected to the input voltage while the other input is connected to a tap of the resistor reference ladder. The gate-source capacitances of the NMOS transistors in the input gain stage couple the input signal to the reference ladder, which results in deterioration of the reference voltages [Fig. 4(a)]. Since the reference voltage determines the location of the zero crossing generated by the input gain stage, this will result in distortion in the A/D converter. In Fig. 4(b) a model is given to calculate the maximum allowed reference ladder resistance for a given shift in the reference voltages [6]. In this model the total ladder resistance  $R$  has been divided into four sections of  $R/4$  each. The total coupling capacitance of the set of input gain stages is given by  $C$ , and has been divided into five capacitors in this model. Capacitance  $C$  is formed by the sum of the capacitances [Fig. 4(a)] of all input gain stages. Since the number of active input gain stages is input voltage dependent, this also accounts for  $C$ .

It is assumed that the feedthrough at nodes  $ref,low$  and  $ref,high$  is negligible due to proper decoupling. Maximum feedthrough will occur on the  $mid$  node, with a feedthrough from the input voltage  $V_{in}$  with frequency  $f_{in}$  given by

$$\frac{V_{mid}}{V_{in}} = \frac{\alpha(\alpha + 32)}{\alpha^2 + 32\alpha + 128}, \quad \text{with } \alpha = \pi f_{in} RC. \quad (2)$$

If it is assumed that  $\alpha \ll 1$ , (2) can be simplified to

$$\frac{V_{mid}}{V_{in}} = \frac{\pi}{4} f_{in} RC. \quad (3)$$

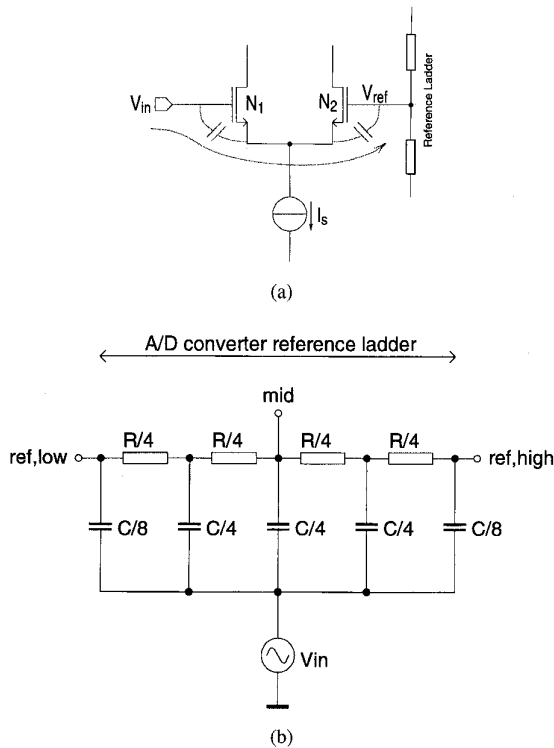


Fig. 4. (a) Reference ladder feedthrough of the input signal via the series capacitive combination in the differential pairs of the input gain stages. (b) Calculation model to derive the maximum resistance of the reference ladder in the A/D converter input circuit for a given shift in the reference voltages.

The required reference ladder resistance for given feedthrough is now defined by

$$R = \frac{4 \frac{V_{mid}}{V_{in}}}{\pi f_{in} C} = \frac{4\phi}{\pi 2^n f_{in} C} \quad (4)$$

in which  $\phi$  is the feedthrough in LSB and  $n$  the resolution of the A/D converter in number of bits. As an example, if a coupling capacitance  $C = 1$  pF is assumed, a maximum feedthrough of 1 LSB in an 8-b converter at 10 MHz input signal frequency requires a reference ladder resistance of 500  $\Omega$ . External decoupling of the middle tap of the reference ladder will reduce the requirement for the ladder resistance by a factor four.

As a second topic related to the input gain stages, the influence of the nonlinear transfer function of the gain stages on the integral nonlinearity of the A/D converter will be discussed. In Fig. 2(c) it has been shown that each of the input gain stages is responsible for 16 code transitions of the A/D converter. Between the output signals of adjacent gain stages, 15 codes (zero crossings) will be generated via interpolation in the folding preprocessing. Therefore, the linearity of the transfer function of the input gain stages has to be guaranteed over 1/16 of the input range. However, zero crossings generated by interpolation will shift due to the nonlinear transfer function of the input gain stages as shown in Fig. 5(a). For the gain stage shown in Fig. 3 in the active region of the differential pair, the output voltage can

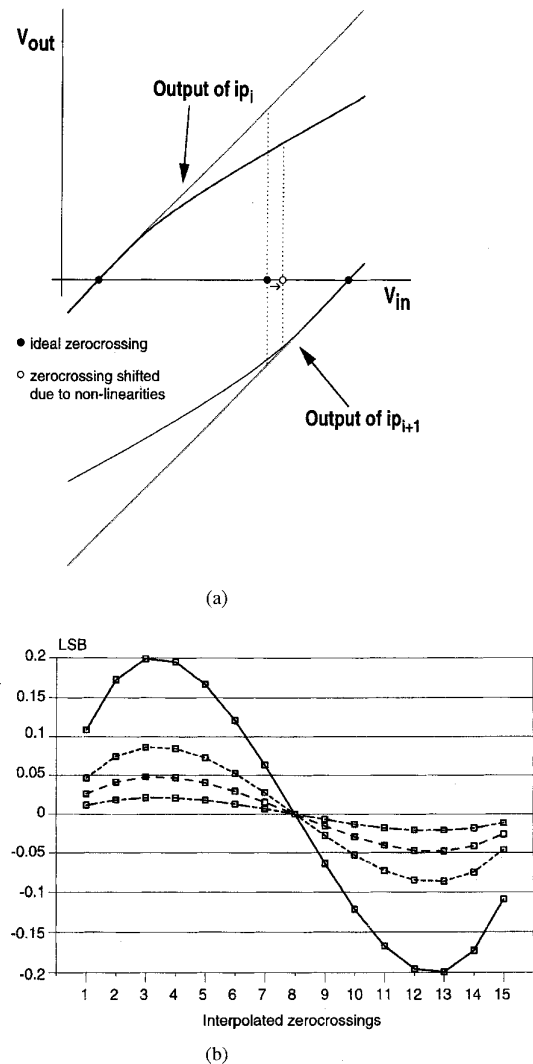


Fig. 5. (a) Interpolation errors due to nonlinearities in the transfer curves of the input gain stages and (b) interpolation errors for different  $V_{GT}$  of the input gain stage transistors.

be represented by

$$V_{out} = \frac{A}{2V_{GT}} (V_{in} - V_{ref}) \sqrt{4V_{GT}^2 - (V_{in} - V_{ref})^2} \quad (5)$$

in which  $A = g_m R$  is the gain of the circuit, with  $g_m$  the transconductance of transistors  $N_1$  and  $N_2$  and

$$V_{GT} = V_{GS} - V_T = \frac{I_s}{g_m}. \quad (6)$$

$I_s$  is the tail current of the differential pair. Two adjacent input gain stages are considered with  $V_{ref1} = 0$  and  $V_{ref2} = V_{range}/16$ .  $V_{range}$  is the input range of the A/D converter. In order to determine the integral nonlinearity error of the A/D converter due to the nonlinearity of the input gain stages, interpolation between transfer functions according to (5) has to be considered. The difference between a linearly interpolated zero crossing and a zero crossing which is generated via nonlinear interpolation has to be analyzed. It can be derived that the integral nonlinearity error  $\delta_{INL}$  due to the nonlinear

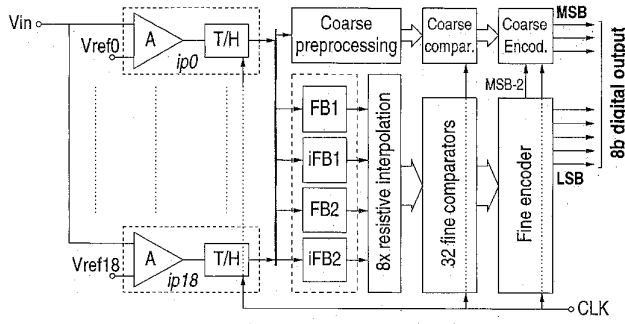


Fig. 6. Block diagram of the entire distributed track-and-hold folding A/D converter.

interpolation yields

$$\delta_{\text{INL}} = V_{\text{in}} \left( 1 - \frac{16V_{\text{in}}}{V_{\text{range}}} \right) \cdot \left[ \sqrt{1 - \left( \frac{V_{\text{in}}}{2V_{\text{GT}}} \right)^2} - \sqrt{1 - \left( \frac{V_{\text{in}} - \frac{V_{\text{range}}}{16}}{2V_{\text{GT}}} \right)^2} \right] \quad (7)$$

With linear interpolation, the zero crossings between both input gain stages are located at the positions

$$V_{\text{in}} = i \frac{V_{\text{range}}}{256}, \quad \text{with } i = 1, 2, \dots, 15. \quad (8)$$

In Fig. 5(b)  $\delta_{\text{INL}}$  has been plotted for various values of parameter  $V_{\text{GT}}$ . From this figure it becomes clear that realization of an interpolation error less than 0.1 LSB requires parameter  $V_{\text{GT}}$  of the input gain stages to be more than 0.15 V. In the above derivation, additional interpolation errors generated in the folding preprocessing are not taken into account. It can be assumed that the interpolation errors due to the nonlinearity of the input gain stages are dominant.

#### IV. A/D CONVERTER IMPLEMENTATION

In Fig. 6 a block diagram is given of the actual implementation of the distributed track-and-hold folding A/D converter. The input circuit of the A/D converter is constructed with 19 track-and-hold gain stages. Seventeen stages  $ip1 \dots ip17$  realize the partitioning of the input range into the 16 subranges as described in Section II. With the additional gain stages  $ip0$  and  $ip18$ , two additional subranges are created beyond and below the input range. These subranges are necessary to ensure the similarity of the 16 subranges within the input range of the A/D converter. Reference voltages  $V_{\text{ref}0} \dots V_{\text{ref}18}$  defining the  $1.6 V_{\text{pp}}$  input range are generated by the resistor reference ladder. Since offsets in the reference voltages directly result in nonlinearity errors of the A/D converter, in layout wide resistors are used and a perfect symmetry has been taken into account. A circuit implementation of the track-and-hold gain stages  $ip$  is given in Fig. 7(a). The gain in the input stage  $g_m R$  equals four, with  $g_m$  the transconductance of the transistors ( $N_1, N_2$ ). Parameters  $V_{\text{GT}}$  of these transistors are 0.3 V to ensure the linearity of the A/D converter as derived in the previous section. Furthermore, transistors  $N_1$  and  $N_2$  have a

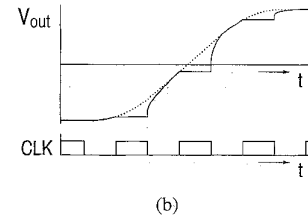
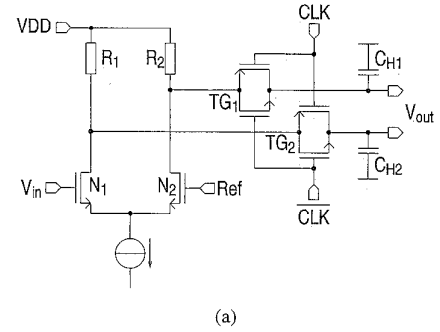


Fig. 7. (a) Implementation of track-and-hold input gain stage and (b) control of the track and hold phases with the CLK signal.

large gate area of  $120 \mu\text{m}^2$  to reduce the offset voltage in the gain stage [9] below 0.25 LSB. Diffusion-type resistors are used for  $R_1$  and  $R_2$  to ensure a small resistor mismatch. Analog bandwidth of the input gain stages will determine the overall analog input bandwidth and high frequency performance of the A/D converter and therefore has to be large (600 MHz). The differential track-and-hold function is implemented with transmission gates  $TG_1$  and  $TG_2$  and hold capacitors  $C_{H1}$  and  $C_{H2}$ . These hold capacitors are implemented by using gate capacitances of transistors. As shown in Fig. 7(b), when the CLK signal level is low, the circuit operates in track mode. At the rising edge of CLK, the hold mode is initiated. Since the folding preprocessing is a zero-crossing detection system, at any moment only two input gain stages contain relevant information about the signal level to be converted. Furthermore, all 19 output signals of the gain stages have the same common mode level. Effects such as input dependent charge injection and on-resistance of the transmission gates are of minor importance to the system performance. An overview of the advantages of the distribution of the track-and-hold operation compared to a single track-and-hold circuit is given in Table I. Due to these advantages, the individual track-and-hold circuits can have this straightforward implementation.

The output signals of  $ip0 \dots ip18$  (Fig. 6) are connected with a parallel operating coarse converter and an eight-times folding, 16-times interpolating fine converter. The circuit implementation of folding blocks FB1 and FB2 is given in Fig. 8(a). The cross-coupled differential pair structure is comparable to the implementation given in [5]. The folding blocks consist of nine NMOS differential pairs with the drains of the even and odd differential pairs cross coupled and are loaded with resistors  $R_1$  and  $R_2$ . The input zero crossing voltages  $in1 \dots in9$  are output signals of nine input track-and-hold gain stages and are shown in Fig. 8(b) versus the input voltage  $V_{\text{in}}$  of the A/D converter. In case of FB1, these input signals

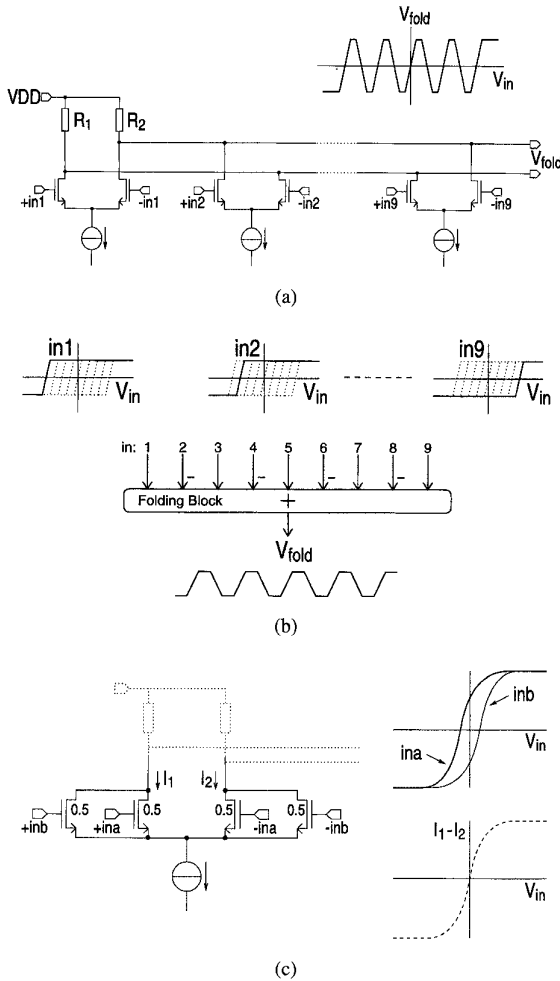


Fig. 8. (a) Implementation of standard folding block with cross-coupled NMOS differential pairs, (b) combination of input signals  $in_1 \dots in_9$  into a single folding signal, and (c) active interpolating differential pair structure with four NMOS transistors.

are the output signals of  $ip_0, ip_2, ip_4, \dots, ip_{16}$  and in case of FB2 these input signals are the output signals of  $ip_1, ip_3, ip_5, \dots, ip_{17}$ . The folding block performs a combination of the nine separate input edges into a single folding signal. Due to the gain in the input stages, offsets in the differential pairs of the folding blocks have only limited impact. Small transistors can be used, so total capacitance at the output nodes of the folding preprocessing is limited. A large bandwidth in the folding preprocessing is ensured. This results in a fast settling of the folding preprocessing when switched into the hold mode.

Two interpolating folding blocks  $iFB1$  and  $iFB2$  (Fig. 6) generate a third and fourth folding signal. Comparing these interpolating folding blocks to FB1 and FB2, the differential pairs are replaced by active interpolating differential pair circuits, as shown in Fig. 8(c). The output current  $I_1 - I_2$  of this four NMOS structure is a function of both input signals  $ina$  and  $inb$ . The devices are scaled to have an equal current density compared to the differential pairs in folding blocks FB1 and FB2. In the output current, a zero crossing is realized in between the zero crossings of the two input signals. Compared to resistive interpolation, this active

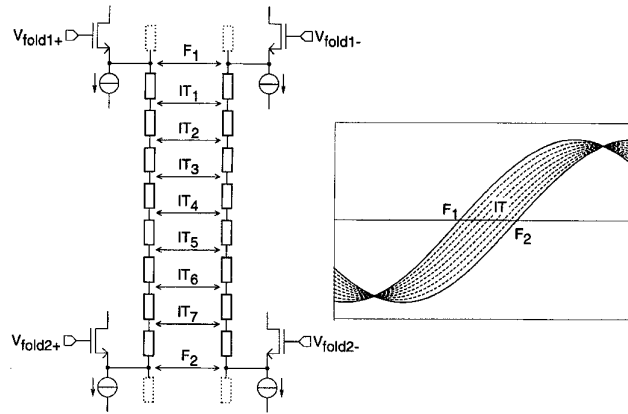


Fig. 9. Differential implementation of resistive interpolation.

interpolation has the advantage that the gain of the input cells is maintained, in contrast to interpolation with a resistive interpolation network [10]. Due to the implementation of the two interpolating folding blocks, the number of input track-and-hold stages  $ip$  could be limited to only 19. Clearly, this yields a power saving, but additionally it results in a low input capacitance of the A/D converter (2 pF). Folding blocks FB1, FB2 and  $iFB1, iFB2$  have an additional two-times gain and this gives a large LSB voltage of 50 mV at the outputs of the (interpolating) folding blocks.

In an 8-b eight-times folding system, 32 folding signals are necessary for the fine conversion. From the folding signals generated in the four folding blocks, an additional 28 folding signals are generated by eight-times resistive interpolation. In Fig. 9 a differential implementation of resistive interpolation is shown. NMOS source followers are used to drive the resistor ladder. Between the differential output voltages of two adjacent folding blocks ( $V_{fold1}, V_{fold2}$ ), the additional folding signals  $IT_1 \dots IT_7$  are generated. An advantage of resistive interpolation over current interpolation is that it is more power efficient. Each of the 32 folding signals has eight zero crossings over the input range of the A/D converter, resulting in a total number of 256 zero crossings, providing an 8-b quantization of the input signal. This is in accordance with Fig. 1(c), showing the transfer of an analog folding preprocessing circuit. The analog coarse preprocessing circuit generates analog versions of the MSB bit, MSB-1 bit and signals to detect overflow and underflow conditions. All of these signals are generated by means of combination of output signals of the track-and-hold input gain stages. The output signal of  $ip_9$  represents the analog MSB signal. The analog MSB-1 signal combines the output signals of  $ip_5, ip_9$ , and  $ip_{13}$ . One of the folding signals represents an analog version of the MSB-2 bit, which completes the required information for coarse quantization of the input signal.

The folding signals and coarse bit information are both digitized by master-slave comparators. An implementation of the master part of the comparator is given in Fig. 10. With a high CLK signal level, the master comparator is in its preamplification phase. The gain of the comparator in this clock phase,  $V_q/V_{comp}$ , is determined by the transconductance

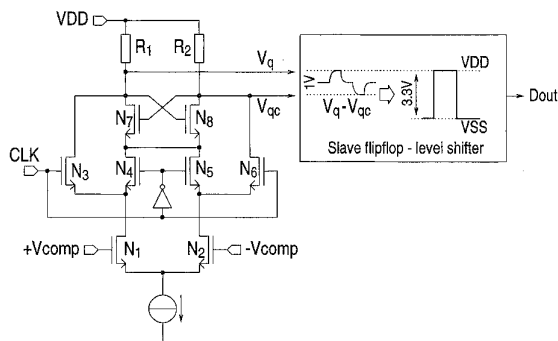


Fig. 10. Implementation of master-slave comparator, optimized for a low bit error rate.

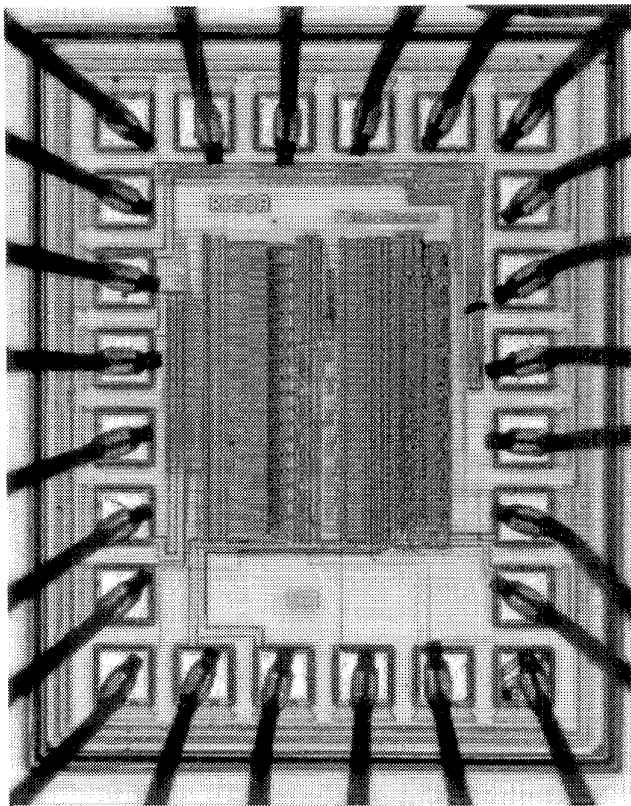


Fig. 11. Chip micrograph of the A/D converter in 0.5- $\mu\text{m}$  standard digital CMOS technology.

of transistors  $N_1$ ,  $N_2$  and resistors  $R_1$ ,  $R_2$ . At the falling edge of CLK, the latch phase is initiated.

A major performance issue of a comparator is the bit error rate (BER), the possibility of a metastable state during the latch phase [8]. The BER is favored by a large comparator unity gain bandwidth and so a large transconductance of latch pair transistors  $N_7$ ,  $N_8$ . Due to the gain in the comparator during the preamplification phase and the large gain in the input track-and-hold gain stages and folding preprocessing, offsets in transistors  $N_7$  and  $N_8$  are not critical. Therefore, small transistors with minimum gate length can be used. The low metastability probability in the comparators has resulted in

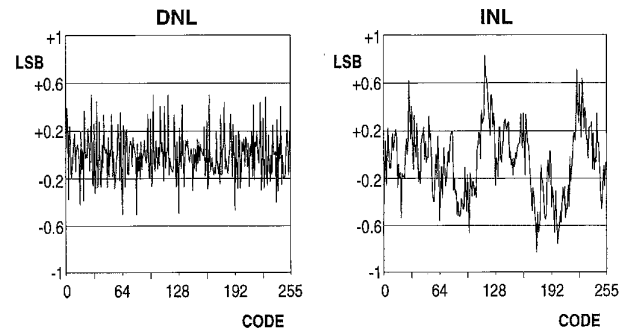


Fig. 12. Differential nonlinearity (DNL) and integral nonlinearity (INL) at maximum clock frequency.

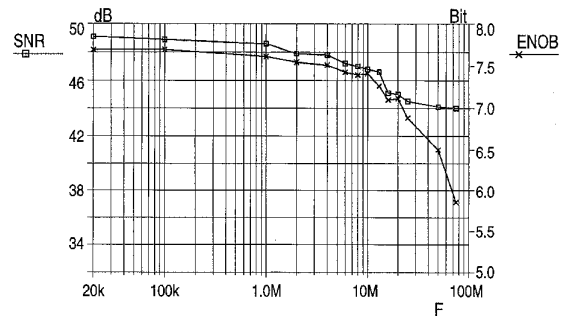


Fig. 13. Dynamic performance of the A/D converter: signal-to-noise ratio (SNR) and effective number of bits (ENOB). Maximum input signal frequency is 75 MHz.

the 80 MHz maximum clock frequency of the A/D converter with low BER. The slave flipflop delivers standard CMOS logic levels for direct interfacing with digital error correction circuitry and coarse and fine encoders. The encoders make use of standard CMOS logic and ROM circuits and generate the output code in a binary format. Additional pipelining in the digital encoding logic is not necessary, resulting in a one-clock-cycle latency of the A/D converter.

## V. MEASUREMENT RESULTS

The A/D converter has been designed in a 0.5- $\mu\text{m}$  single-poly, triple-metal standard digital CMOS technology. A micrograph of the chip is shown in Fig. 11. Active chip area is 0.3 mm<sup>2</sup>. This chip size can be realized, since the critical parts of the A/D converter with respect to transistor mismatch are the 19 input gain stages only. Small transistors can be used in the rest of the analog part of the A/D converter. Supply voltage of the chip is 3.3 V. At the maximum clock frequency of 80 MHz, power dissipation is 80 mW. This includes the digital circuitry and the reference ladder power dissipation. Linearity measurements and dynamic measurements are done with a digital test setup. In Fig. 12 both the integral and differential nonlinearity of the A/D converter are given for a low frequency input signal. Fig. 13 shows the signal-to-noise ratio (SNR) and effective number of bits (ENOB). Measurements were done at the maximum clock frequency of 80 MHz. The BER was measured by applying a low amplitude input signal around the MSB transition. The occurrences of bit errors can be identified with an exnor operation on the MSB and MSB-1 bit. The

TABLE II  
SPECIFICATIONS OF THE DISTRIBUTED  
TRACK-AND-HOLD FOLDING A/D CONVERTER

Technology	0.5 $\mu\text{m}$ CMOS, single poly, triple metal
Resolution	8-bit
Effective number of bits	7.5 bit
SNR ( $f_m = 75$ MHz)	44 dB
Large signal analog bandwidth	75 MHz
Maximum clock frequency	80 MHz
BER at maximum clock frequency	$<10^{-12}$
Active chip area	0.3 mm <sup>2</sup>
Supply voltage	3.3 V
Power dissipation (including digital and reference ladder)	80 mW
Analog input voltage range	1.6 V
Input capacitance	2 pF
Integral non-linearity (INL)	0.8 LSB
Differential non-linearity (DNL)	0.45 LSB

measured BER can be found in Table II, giving an overview of the specifications of the A/D converter.

## VI. CONCLUSIONS

An extension of the folding A/D converter architecture with a distributed track-and-hold input preprocessing has been designed. It has been shown that this extension leads to an improved system architecture. The analog bandwidth limitation generally encountered in folding A/D converters has been conquered. Furthermore, it has been made clear that distribution of the track-and-hold operation instead of a single track-and-hold amplifier at the input of the A/D converter is advantageous for realization of a high-performance track-and-hold function. Additionally, this distributed track-and-hold input processing relaxes the constraints to the implementation of the analog folding preprocessing and coarse preprocessing.

The A/D converter achieves a maximum full-scale analog input signal bandwidth of 75 MHz, with a small signal  $-3$  dB bandwidth of 600 MHz. Limiting factor to the dynamic performance is harmonic distortion. Maximum clock frequency is 80 MHz. From a 3.3-V supply voltage, power dissipation equals 80 mW. Active chip area is limited to 0.3 mm<sup>2</sup>.

## ACKNOWLEDGMENT

The authors wish to acknowledge L. Giry of Philips Semiconductors, Caen, France, for his cooperation and support during the evaluation of the A/D converter.

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